Surge Components, Inc

APPROVAL DRAWING

Surge Components product name
SES5VT553-5 TR (RoHS compliant)

CONTENTS

Surge Components, Inc.

Customer Acknowledgement	Manufacturer Surge Components, Inc. 2009-05-06

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Deer Park, NY
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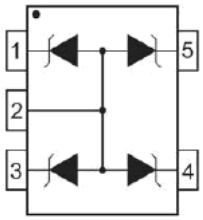
(631)595-1818

1.FEATURE

- 100 Watts Peak Power per Line(tp=8/20us)
- SOT-553 package
- Protects three bidirectional lines and four Unidirectional lines
- Monolithic structure
- Working woltage: 5V
- Low clamping voltage
- ESD protection > 40KV
- Low leakage current
- RoHS compliant
- Transient protection for data lines to IEC 61000-4-2(ESD) ± 15KV (air), ± 8KV (contact); IEC 61000-4-4 (EFT) 40A (5/50ns)



2. APPLICATION

- Communication Systems
- Printers
- Notebooks and hand hold computers
- PDAs
- Video Equipment

3. ELECTRICAL CHARACTERISTICS PER LINE@25℃(UNLESS OTHERWISE SPECIFIED) note 1

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Reverse stand-off voltage	V_{RWM}				5	V
Reverse Breakdown voltage	V_{BR}	I_t=1mA	6			V
Reverse Leakage Current	I_R	V_{RWM}=5V T=25℃			5	uA
Clamping Voltage	V_C	I_{PP}=1A T_P=8/20uS			8.8	V
Clamping voltage	V_C	I_{PP}=10A T_P=8/20uS			10.0	V
Junction Capacitance	C_J	V_R=0V f=1MHz		40		pF

- Note 1: Pin 1,3,4,5 to Pin 2

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4. ABSOLUTE MAXIMUM RATING @25℃ note 1

Rating	Symbol	Value	Units
Peak Pulse Power(t_p=8/20μs)	P_{PP}	100	W
Forward voltage@1 0mA	V_F	1.5	V
Operating Temperature	T_j	-55 to +150	℃
Storage Temperature	T_{STG}	-55 to +150	℃

- Note 1: Pin 1,3,4,5 to Pin 2

5.TYPICAL CHARACTERISTICS

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

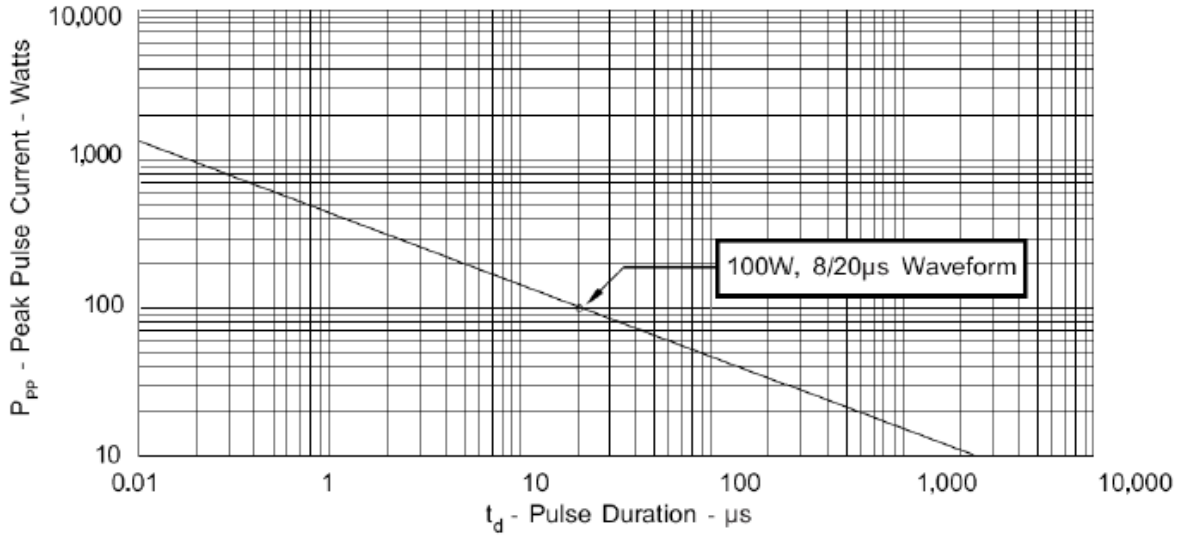

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FIGURE 2
PULSE WAVE FORM

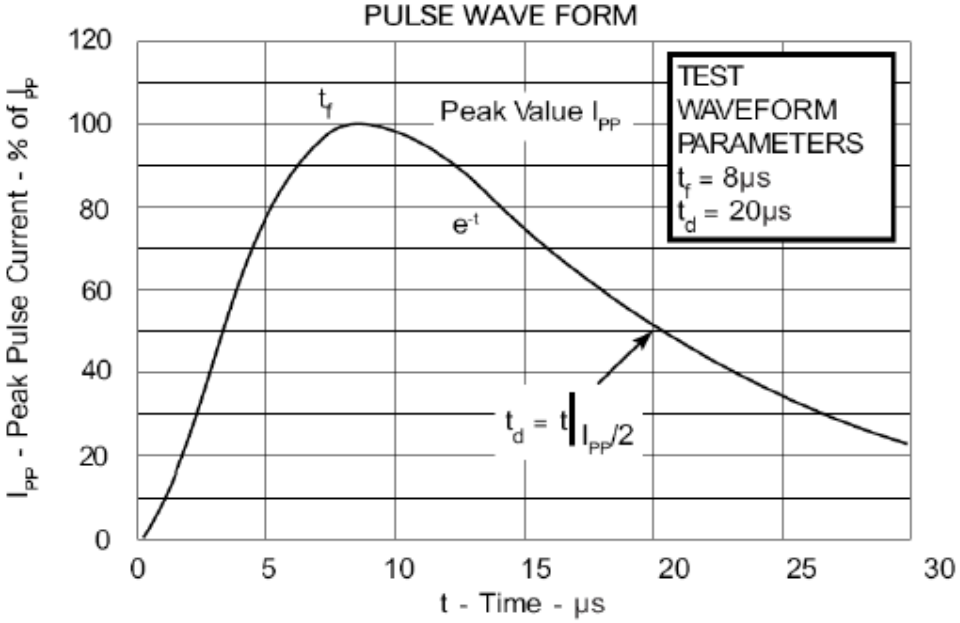
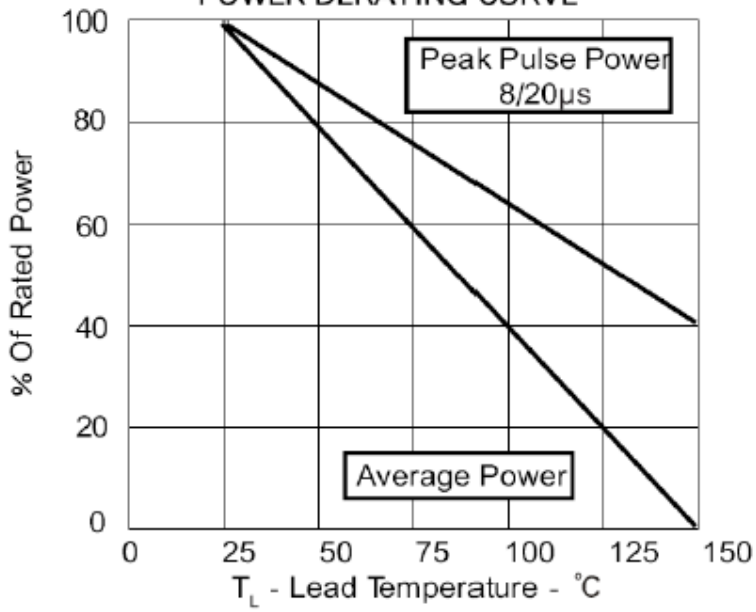


FIGURE 3
POWER DERATING CURVE



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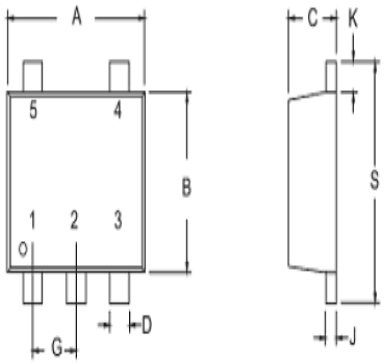
6. PRODUCT DIMENSION AND PAD SIZE.

PACKAGE OUTLINE



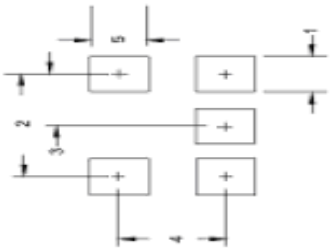
SOT-553

PACKAGE DIMENSION

DIM	MILIMETER		INCHES	
	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.1	1.3	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC	-	0.020 BSC	-
J	0.06	0.16	0.003	0.006
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

Mounting Pad

TYPICAL		
DIM	MILIMETER	INCHES
1	0.30	0.012
2	1.02	0.040
3	0.51	0.020
4	1.40	0.055
5	0.51	0.020



NOTES:
1. Controlling Dimension Inches
2. Pin 3 is the cathode (Unidirectional only).
3. Dimensions are exclusive of mold lash and metal burrs

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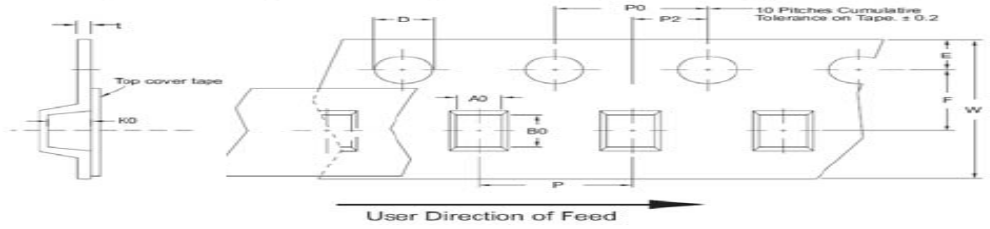
7.PACKING INFORMATION

Reel Dia	Tape Width	AO	BO	KO	D	E	F	W	PO	P2	P	Imax
178mm(7")	8mm	1.78±0.05	1.78±0.05	0.69±0.05	1.50±0.10	1.75±0.10	3.50±0.10	8.00±0.30	4.00±0.10	2.00±0.005	4.00±0.10	0.25



8. APPLICATION NOTE

The SES5VT553-5 is TVS arrays designed to protect I/O or data lines from the damaging effects of ESD or EFT. This product provides both unidirectional and bidirectional protection, with a surage capability of 100 watts Ppp line for an 8/20μs wave shape and ESD protection > 25kv.

Common-mode unidirectional configuration(Figure 1)
The SES5VT553-5 provides up to 4 lines of protection in a common-mode unidirectional configuration as depicted in Figure 1.

Circuit connectivity is as follows:

- Line 1 is connected to Pin1.
- Line 2 is connected to Pin3.
- Line 3 is connected to Pin4.
- Line 4 is connected to Pin5.
- Pin2 is connected to ground.

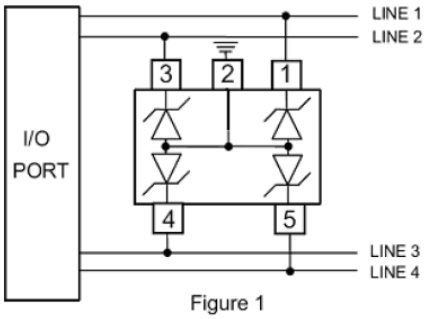


Figure 1

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Common-mode unidirectional configuration(Figure 2)

The SES5VT553-5 provides up to 3 lines of protection in a common-mode bidirectional configuration as depicted in Figure 2.

Circuit connectivity is as follows:

- Line 1 is connected to Pin1.
- Line 2 is connected to Pin3.
- Line 3 is connected to Pin4.
- Pin5 is connected to ground.
- Pin2 is not connected.

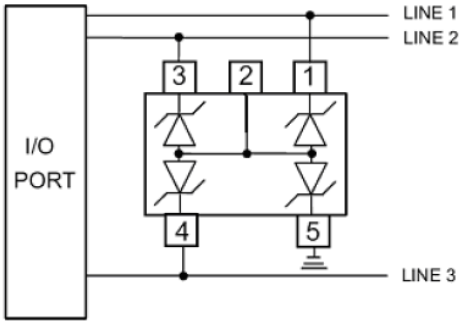

Figure 2

Differential-mode bidirectional configuration (Figure 3)

The SES5VT553-5 provides up to 4 lines of protection in a Differential-mode bidirectional configuration as depicted in Figure 3.

Circuit connectivity is as follows:

- Line 1 is connected to Pin1.
- Line 2 is connected to Pin3.
- Line 3 is connected to Pin4.
- Line 4 is connected to Pin5.
- Pin2 is not connected.

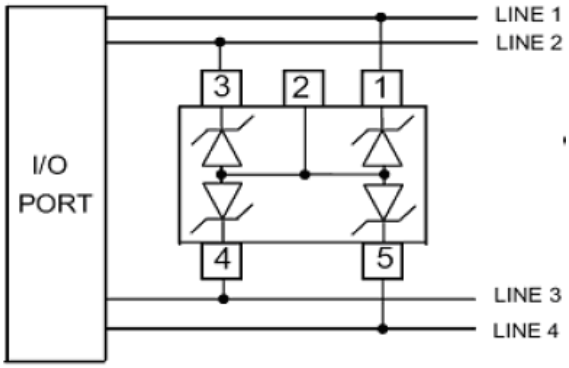

Figure 3

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Circuit board layout and protection device placement:

Circuit board layout is critical for suppression of ESD transients.
The following guidelines are recommended:

1. Place the protection devices as close to the input terminal or connector as possible.
2. The path length between the protection device and protected line should be minimized.
3. Keep parallel signal pats to a minimum.
4. Avoid running protection conductors in parallel with unprotected conductor.
5. Minimize all printed-circuit board conductive loops including power and ground loops.
6. minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to common ground point.
8. Ground planes should be used whenever possible. For multilayer printed-circuit boards, use ground vias.

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