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April 1st, 2010 Renesas Electronics Corporation

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MOS FIELD EFFECT TRANSISTOR $\mu PA2704GR$

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA2704GR is N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

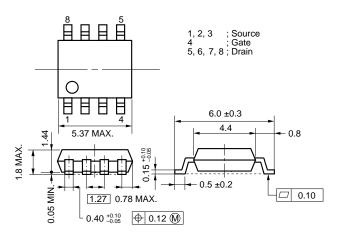
FEATURES

- Low on-state resistance $R_{DS(on)1} = 7.2 \text{ m}\Omega$ MAX. (Vgs = 10 V, ID = 7.0 A) $R_{DS(on)2} = 11.2 \text{ m}\Omega$ MAX. (Vgs = 4.5 V, ID = 7.0 A)
- Low Ciss: Ciss = 1200 pF TYP. (VDS = 10 V, VGS = 0 V)
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2704GR	Power SOP8

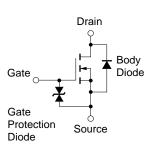
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	30	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20	V
Drain Current (DC)	I _{D(DC)}	±14	Α
Drain Current (pulse) Note1	ID(pulse)	±56	Α
Total Power Dissipation (T _A = 25°C) Note2	Рт	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note3	las	14	Α
Single Avalanche Energy Note3	Eas	19.6	mJ

EQUIVALENT CIRCUIT



- **Notes 1.** PW \leq 10 μ s, Duty Cycle \leq 1%
 - 2. Mounted on ceramic substrate of 1200 mm² x 2.2 mm
 - 3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω , L = 100 μ H, V_{GS} = 20 \rightarrow 0 V

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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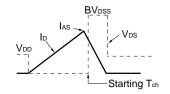


ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

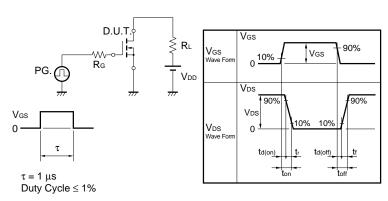
	•					
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 30 V, V _{GS} = 0 V			10	μΑ
Gate Leakage Current	lgss	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		2.5	V
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 7.0 A	7	14		S
Drain to Source On-state Resistance	RDS(on)1	V _G S = 10 V, I _D = 7.0 A		5.8	7.2	mΩ
	R _{DS(on)2}	Vgs = 4.5 V, ID = 7.0 A		8.5	11.2	mΩ
	R _{DS(on)3}	Vgs = 4.0 V, Ib = 7.0 A		9.8	13.0	mΩ
Input Capacitance	Ciss	V _{DS} = 10 V		1200		pF
Output Capacitance	Coss	V _G S = 0 V		500		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		160		pF
Turn-on Delay Time	t d(on)	V _{DD} = 15 V, I _D = 7.0 A		10		ns
Rise Time	tr	Vgs = 10 V		13		ns
Turn-off Delay Time	t d(off)	$R_G = 10 \Omega$		44		ns
Fall Time	t _f			11		ns
Total Gate Charge	Q _G	V _{DD} = 15 V		12		nC
Gate to Source Charge	Qgs	Vgs = 5 V		4		nC
Gate to Drain Charge	Q _{GD}	ID = 14 A		6		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 14 A, VGS = 0 V		0.8	1.2	V
Reverse Recovery Time	trr	IF = 14 A, VGS = 0 V		32		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/ μs		27		nC

TEST CIRCUIT 1 AVALANCHE CAPABILITY

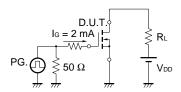
$\begin{array}{c} \text{D.U.T} \\ \text{Rg} = 25 \, \Omega \\ \text{VGS} = 20 \rightarrow 0 \, \text{V} \end{array} \begin{array}{c} \text{PG.} \\ \text{PG.} \\ \text{My.} \end{array} \begin{array}{c} \text{D.U.T} \\ \text{VDD} \end{array}$



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



NEC μ PA2704GR

[MEMO]

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