



Pb Free Plating Product

## CS48N78

70V,80A N-Channel Trench Process Power MOSFET

### General Description

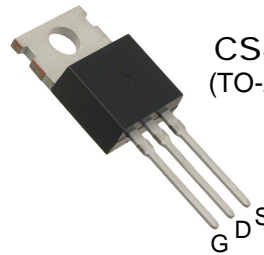
The CS48N78 is N-channel MOS Field Effect Transistor designed for high current switching applications. Rugged EAS capability and ultra low  $R_{DS(ON)}$  is suitable for PWM, load switching especially for E-Bike controller applications.

### Features

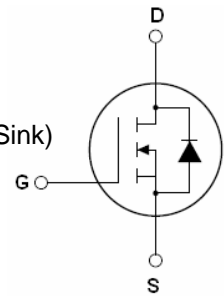
- $V_{DS}=70V$ ;  $I_D=80A@V_{GS}=10V$ ;  
 $R_{DS(ON)} < 7.2m\Omega @ V_{GS}=10V$
- Special Designed for E-Bike Controller Application
- Ultra Low On-Resistance
- High UIS and UIS 100% Test

### Application

- 48V E-Bike Controller Applications
- Hard Switched and High Frequency Circuits
- Uninterruptible Power Supply



CS48N78  
(TO-220 HeatSink)



Schematic Diagram

$V_{DS} = 70 V$

$I_D = 80 A$

$R_{DS(ON)} = 5.9 m\Omega$

Table 1. Absolute Maximum Ratings (TA=25°C)

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-Source Voltage ( $V_{GS}=0V$ )	70	V
$V_{GS}$	Gate-Source Voltage ( $V_{DS}=0V$ )	$\pm 25$	V
$I_{D(DC)}$	Drain Current (DC) at $T_c=25^\circ C$	80	A
$I_{D(DC)}$	Drain Current (DC) at $T_c=100^\circ C$	56	A
$I_{DM(pluse)}$	Drain Current-Continuous@ Current-Pulsed (Note 1)	320	A
dv/dt	Peak Diode Recovery Voltage	30	V/ns
$P_D$	Maximum Power Dissipation( $T_c=25^\circ C$ )	100	W
	Derating Factor	0.66	W/°C
$E_{AS}$	Single Pulse Avalanche Energy (Note 2)	410	mJ
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 To 175	°C

Notes 1.Repetitive Rating: Pulse width limited by maximum junction temperature

2.EAS condition: $T_J=25^\circ C, V_{DD}=33V, V_G=10V, I_D=40.5A$

Table 2. Thermal Characteristic

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.5	$^{\circ}C/W$

Table 3. Electrical Characteristics ( $T_A=25^{\circ}C$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>On/Off States</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	70			V
$I_{DSS}$	Zero Gate Voltage Drain Current( $T_c=25^{\circ}C$ )	$V_{DS}=68V, V_{GS}=0V$			1	$\mu A$
$I_{DSS}$	Zero Gate Voltage Drain Current( $T_c=125^{\circ}C$ )	$V_{DS}=68V, V_{GS}=0V$			10	$\mu A$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS}=\pm 25V, V_{DS}=0V$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=40A$		5.9	7.2	m $\Omega$
<b>Dynamic Characteristics</b>						
$g_{FS}$	Forward Transconductance	$V_{DS}=10V, I_D=15A$	20			S
$C_{iss}$	Input Capacitance	$V_{DS}=25V, V_{GS}=0V,$ $f=1.0MHz$		3483		pF
$C_{oss}$	Output Capacitance			459		pF
$C_{rss}$	Reverse Transfer Capacitance			214		pF
$Q_g$	Total Gate Charge	$V_{DS}=50V, I_D=40A,$ $V_{GS}=10V$		82		nC
$Q_{gs}$	Gate-Source Charge			16.2		nC
$Q_{gd}$	Gate-Drain Charge			36.7		nC
<b>Switching Times</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=30V, I_D=2A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$		11		nS
$t_r$	Turn-on Rise Time			13		nS
$t_{d(off)}$	Turn-Off Delay Time			22		nS
$t_f$	Turn-Off Fall Time			27		nS
<b>Source-Drain Diode Characteristics</b>						
$I_{SD}$	Source-Drain Current(Body Diode)			80		A
$I_{SDM}$	Pulsed Source-Drain Current(Body Diode)			320		A
$V_{SD}$	Forward On Voltage <sup>(Note 1)</sup>	$T_J=25^{\circ}C, I_{SD}=40A, V_{GS}=0V$		0.69	0.95	V
$t_{rr}$	Reverse Recovery Time <sup>(Note 1)</sup>	$T_J=25^{\circ}C, I_F=75A$ $di/dt=100A/\mu s$		40		nS
$Q_{rr}$	Reverse Recovery Charge <sup>(Note 1)</sup>			81		nC
$t_{on}$	Forward Turn-on Time	Intrinsic turn-on time is negligible(turn-on is dominated by $L_S+L_D$ )				

Notes 1. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 1.5\%$ ,  $R_G=25\Omega$ , Starting  $T_J=25^{\circ}C$



## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

Figure1. Safe Operating Area

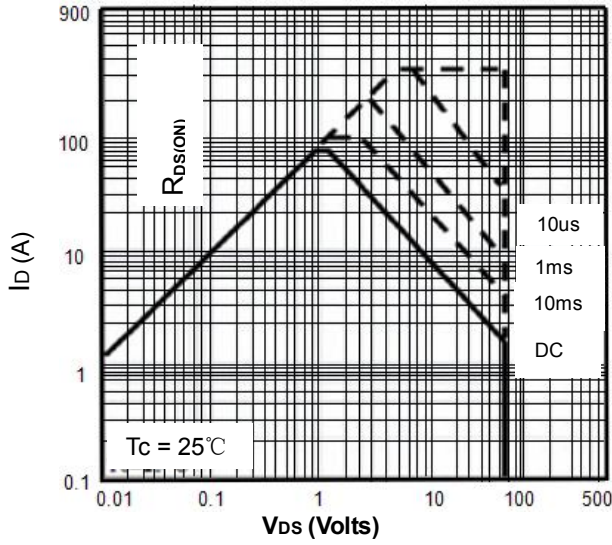


Figure2. Source-Drain Diode Forward Voltage

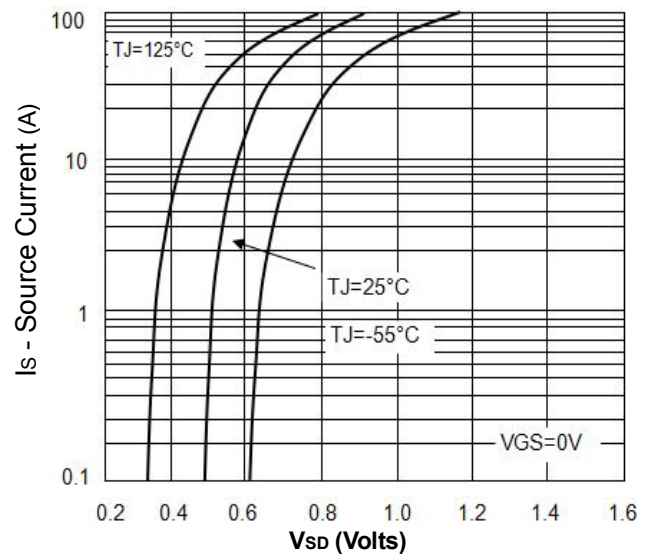


Figure3. Output Characteristics

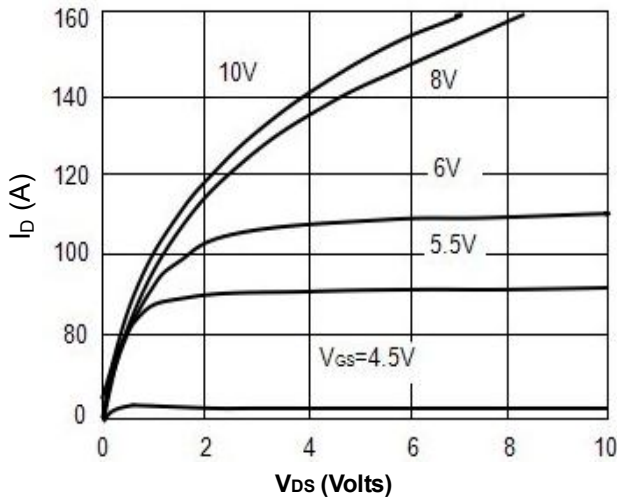


Figure4. Transfer Characteristics

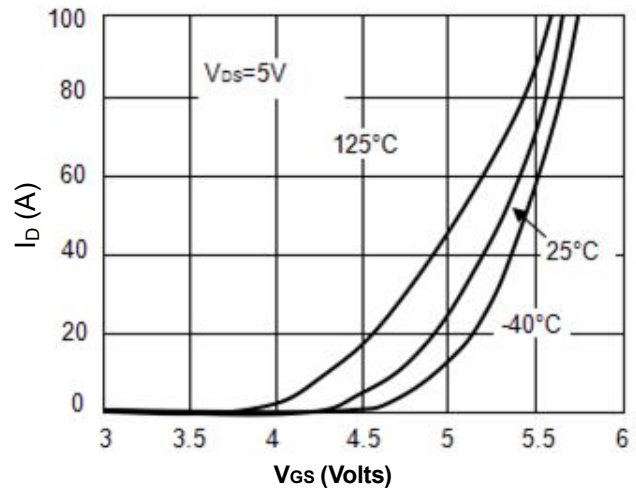


Figure5. Static Drain-Source On Resistance

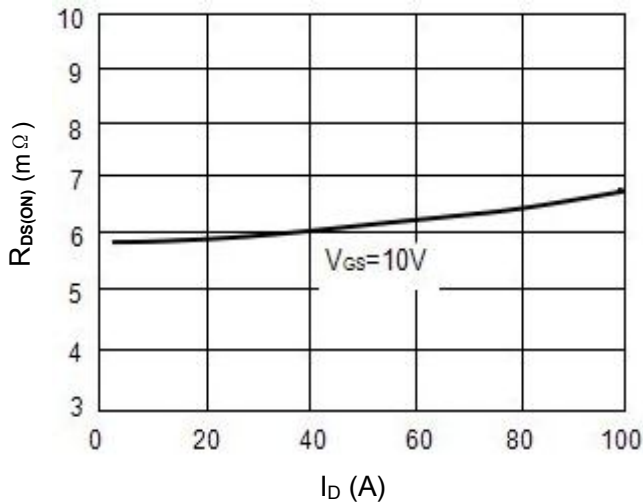
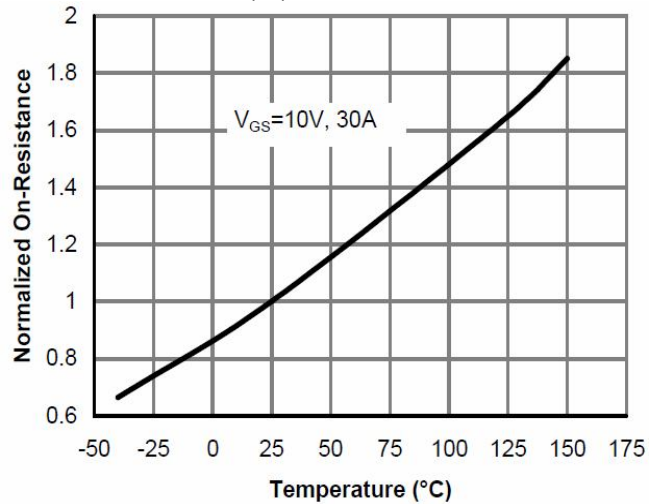
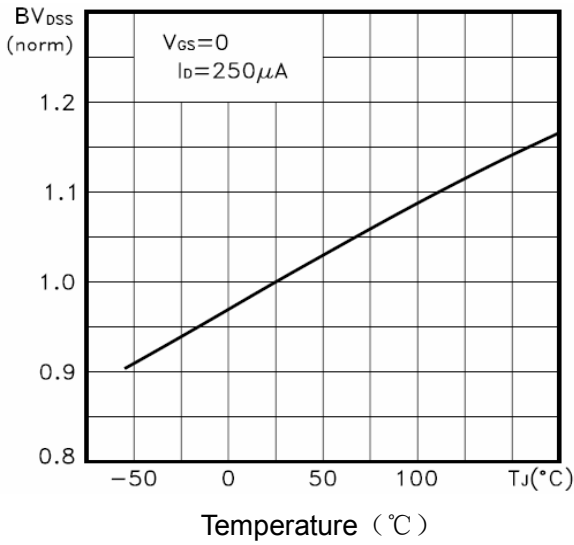


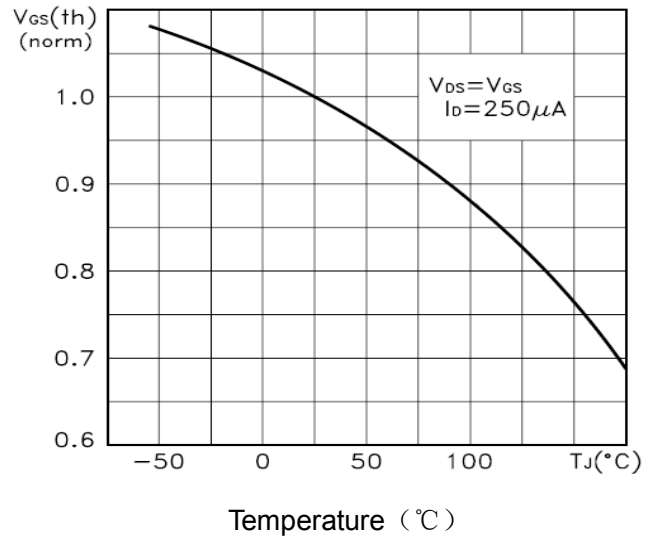
Figure6. R<sub>DS(ON)</sub> vs Junction Temperature



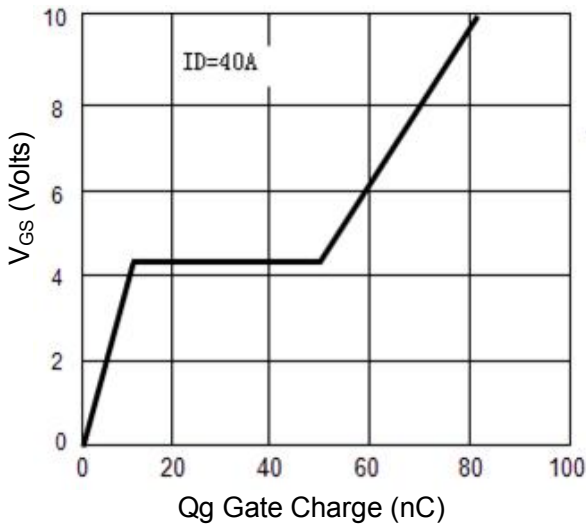
**Figure7.  $BV_{DSS}$  vs Junction Temperature**



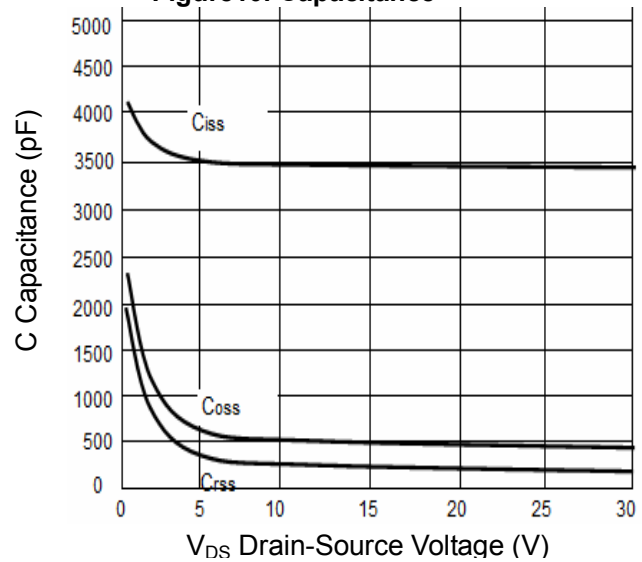
**Figure8.  $V_{GS(th)}$  vs Junction Temperature**



**Figure9. Gate Charge Waveforms**



**Figure10. Capacitance**



**Figure11. Normalized Maximum Transient Thermal Impedance**

