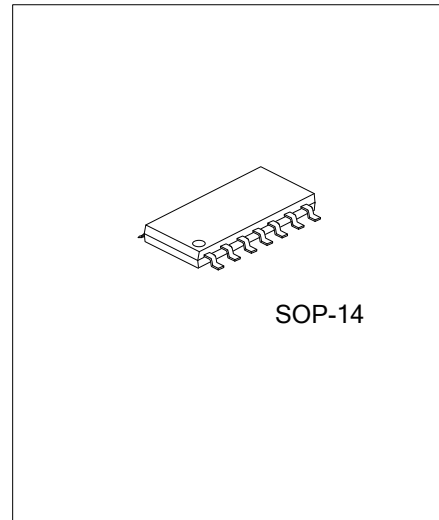




# U74ACT125

**CMOS IC**

## QUAD BUFFER WITH 3-STATE OUTPUTS



■ DESCRIPTION

The **U74ACT125** contains four independent non-inverting buffers with 3-STATE outputs.

■ FEATURES

- \* Outputs source/sink 24mA
- \*ACT125 has TTL-compatible outputs

■ ORDERING INFORMATION

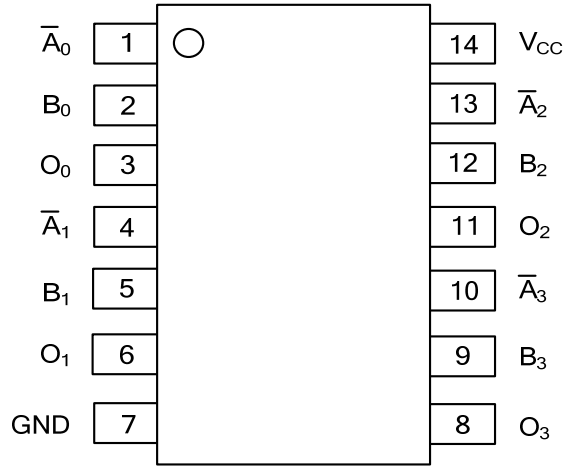
Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74ACT125L-S14-R	U74ACT125G-S14-R	SOP-14	Tape Reel

<p>U74ACT125L-S14-R</p> <p>(1)Packing Type (2)Package Type (3)Lead Plating</p>	<p>(1) R: Tape Reel (2) S14: SOP-14 (3) L: Lead Free, G: Halogen Free</p>
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# U74ACT125

CMOS IC

■ PIN CONFIGURATION

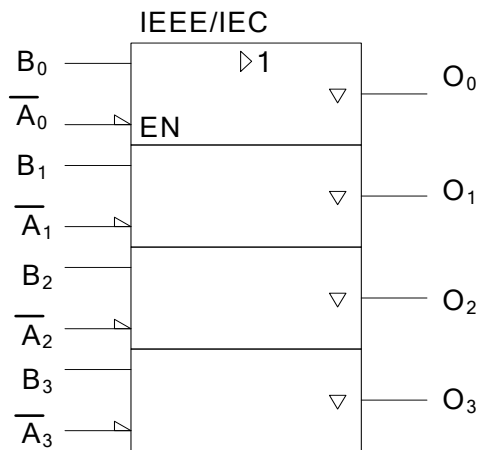
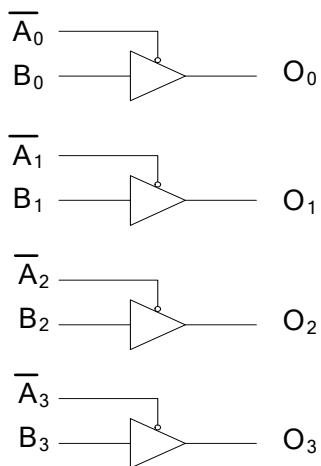


■ FUNCTION TABLE (each gate)

INPUTS		OUTPUT
A <sub>n</sub>	B <sub>n</sub>	O <sub>n</sub>
L	L	L
L	H	H
H	X	Z

H=HIGH Voltage Level; L=LOW Voltage Level  
Z=HIGH Impedance; X=Immaterial

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{CC}$	-0.5~7	V
Input Voltage	$V_{IN}$	-0.5~ $V_{CC}+0.5$	V
Output Voltage(active mode)	$V_{OUT}$	-0.5~ $V_{CC}+0.5$	V
Input Diode Current( $V_{IN}=-0.5V$ )	$I_{IK}$	-20	mA
Input Diode Current( $V_{IN}=V_{CC}+0.5V$ )	$I_{IK}$	+20	mA
Output Diode Current( $V_{IN}=-0.5V$ )	$I_{OK}$	-20	mA
Output Diode Current( $V_{IN}=V_{CC}+0.5V$ )	$I_{OK}$	+20	mA
Output Current	$I_{OUT}$	±50	mA
$V_{CC}$ or GND Current	$I_{CC}$	±100	mA
Storage Temperature	$T_{STG}$	-65 ~ +150	°C

Notes: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.  
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	$V_{CC}$		4.5		5.5	V
Input Voltage	$V_{IN}$		0		$V_{CC}$	V
Output Voltage	$V_{OUT}$		0		$V_{CC}$	V
Minimum Input Edge Rate	$\Delta v/\Delta t$	$V_{IN}$ from 0.8V to 2.0V $V_{CC}$ @ 4.5V, 5.5V			125	mV/ns
Operating Temperature	$T_A$		-40		+85	°C

■ STATIC CHARACTERISTICS ( $T_A=25^\circ C$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
HIGH Level Input Voltage	$V_{IH}$	$V_{CC}=4.5V$	2	1.5		V	
		$V_{CC}=5.5V$	2	1.5			
LOW Level Input Voltage	$V_{IL}$	$V_{CC}=4.5V$		1.5	0.8	V	
		$V_{CC}=5.5V$		1.5	0.8		
High-Level Output Voltage	$V_{OH}$	$I_{OH}=-50\mu A$	$V_{CC}=4.5V$	4.4	4.49	V	
			$V_{CC}=5.5V$	5.4	5.49		
		$I_{OH}=-24mA$	$V_{CC}=4.5V$	3.86			
			$V_{CC}=5.5V$	4.86			
Low-Level Output Voltage	$V_{OL}$	$I_{OL}=50\mu A$	$V_{CC}=4.5V$		0.001	0.1	V
			$V_{CC}=5.5V$		0.001	0.1	
		$I_{OL}=24mA$	$V_{CC}=4.5V$			0.36	
			$V_{CC}=5.5V$			0.36	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC} = 5.5V, V_{IN}=V_{CC}$ or GND			±0.1	μA	
Quiescent Supply Current	$I_{CC}$	$V_{CC} = 5.5V, V_{IN}=5.5V$ or GND $I_{OUT}=0$			4	μA	
Maximum $I_{CC}$ /Input	$I_{CCT}$	$V_{CC} = 5.5V, V_I=V_{CC}-2.1V$		0.6		mA	
Input Capacitance	$C_{IN}$	$V_{CC} = OPEN$		4.5		pF	
3-STATE Current	$I_{OZ}$	$V_{CC}=5.5V, V_I=V_{IL}, V_{IH}$ $V_O=V_{CC}, GND$			±0.5	μA	

■ DYNAMIC CHARACTERISTICS (T<sub>A</sub>=25°C, unless otherwise specified)

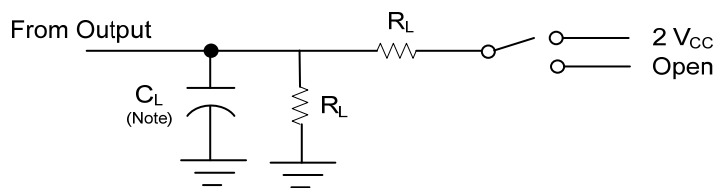
See Fig. 1 and Fig. 2 for test circuit and waveforms.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay Data to Output	t <sub>PLH</sub>	V <sub>CC</sub> =5V, t <sub>r</sub> = t <sub>f</sub> =3ns, C <sub>L</sub> =50pF, R <sub>L</sub> =500Ω, f=1MHz	1	6.5	9	ns
	t <sub>PHL</sub>		1	7	9	
Output Enable Time	t <sub>PZH</sub>		1	6.0	8.5	ns
	t <sub>PZL</sub>		1	7.0	9.5	ns
Output disable Time	t <sub>PHZ</sub>		1	7.0	9.5	ns
	t <sub>PLZ</sub>		1	7.5	10	ns

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C <sub>PD</sub>	V <sub>CC</sub> =5V		45		pF

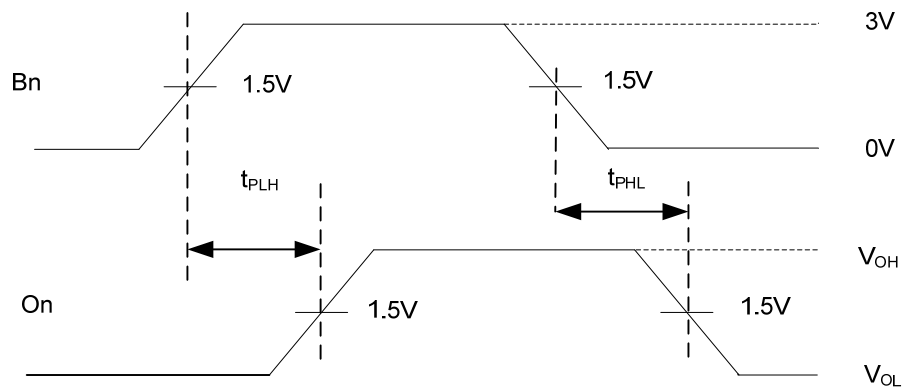
■ TEST CIRCUIT AND WAVEFORMS



Note:  $C_L$  includes probe and jig capacitance.

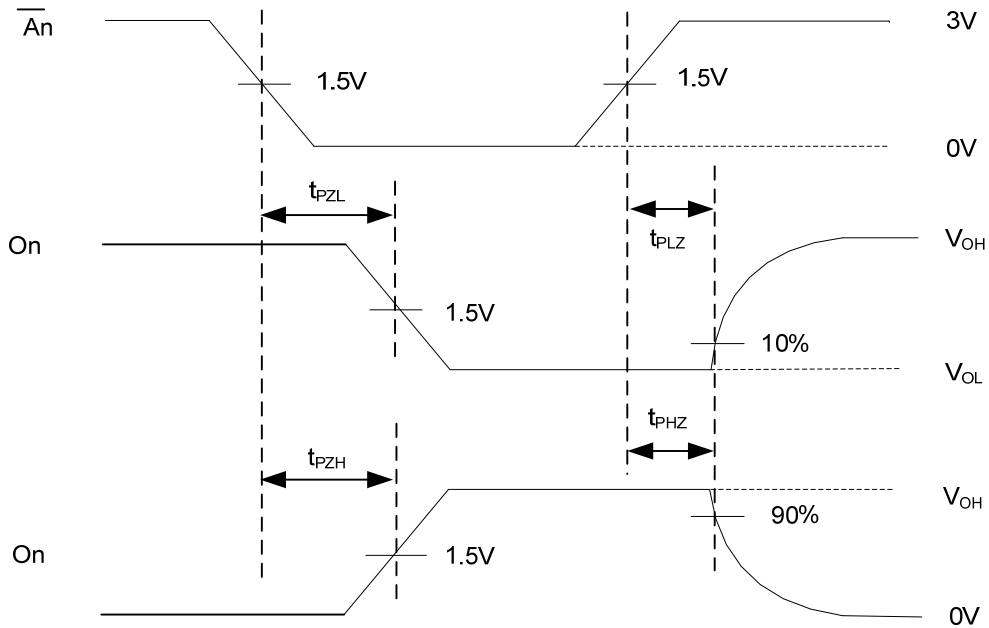
TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PLZ}$ , $t_{PZL}$	$2V_{CC}$
$t_{PZH}$ , $t_{PHZ}$	Open

Fig. 1 Load circuitry for switching times.



PROPAGATION DELAY TIMES

■ TEST CIRCUIT AND WAVEFORMS (Cont.)



**ENABLE AND DISABLE TIMES**

**Fig. 2 Propagation delay from input to output and Output transition time**

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