SY88403BL

3.3V 4.25Gbps CML Low-Power Limiting Post Amplifier with TTL LOS

General Description

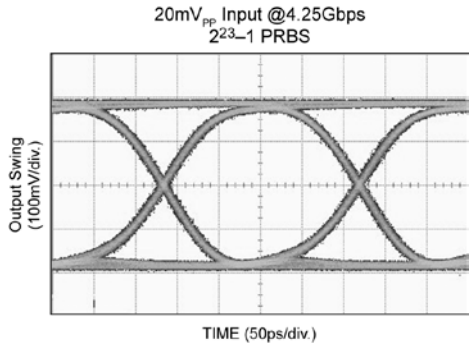
The SY88403BL is a low-power limiting post amplifier optimized for copper applications. The device connects to typical transimpedance amplifiers (TIAs). The linear signal output from TIAs can contain significant amounts of noise and may vary in amplitude over time. The SY88403BL quantizes these signals and outputs typically 800mV$_{PP}$ voltage-limited waveforms.

The SY88403BL operates from a single +3.3V ±10% power supply, over an industrial temperature range of –40°C to +85°C. With its wide bandwidth and high gain, signals with data rates up to 4.25Gbps and as small as 5mV$_{PP}$ can be amplified to drive devices with CML inputs or AC-coupled PECL inputs.

The SY88403BL incorporates a loss-of-signal (LOS) open-collector TTL output with internal 4.75kΩ pull-up resistor. A programmable loss-of-signal level set pin (LOSLVL) sets the sensitivity of the input amplitude detection. LOS asserts high if the input amplitude falls below the threshold set by LOSLVL and de-asserts low otherwise. LOS can be fed back to the enable bar (/EN) input to maintain output stability under a loss of signal condition. /EN de-asserts the true output signal without removing the input signal. Typically, 3.5dB LOS hysteresis is provided to prevent chattering.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Typical Performance



Features

- Multi-rate up to 4.25Gbps operation
- 5mV$_{PP}$ input sensitivity
- Low noise 50Ω CML data outputs
  - 800mV$_{pp}$ output swing
  - 60ps edge rates
  - 1ps$_{RMS}$ typ. random jitter
  - 10ps$_{PP}$ typ. deterministic jitter
- Chatter-free Loss-of-Signal (LOS) output
  - 3.5dB electrical hysteresis
  - OC-TTL output with internal 4.75kΩ pull-up resistor
- Programmable LOS sensitivity using single external resistor
- Internal 50Ω data input termination
- TTL /EN input allows feedback from LOS
- Wide operating range:
  - Single 3.3V ±10% power supply
  - Industrial temperature range: –40°C to +85°C
- Available in a 10-pin EPAD-MSOP and 16-pin QFN package

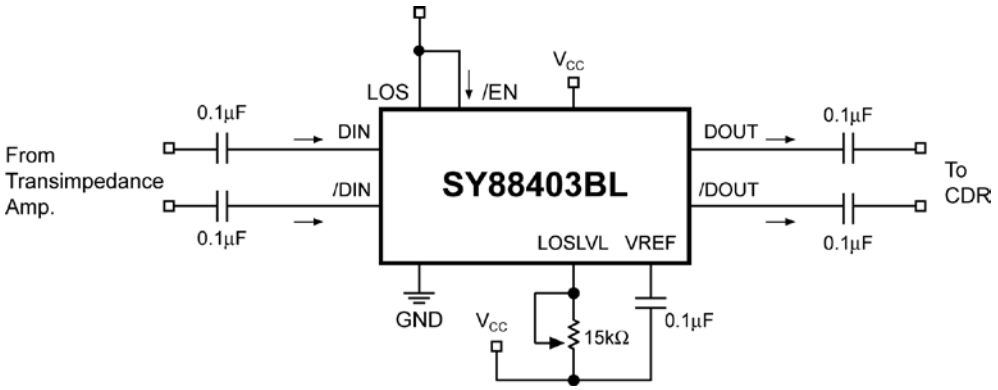
Applications

- 1.062Gbps, 2.125Gbps and 4.25Gbps Fibre Channel
- Cable driver
- Small form factor (SFF) and small form factor pluggable (SFP) transceivers
- High-gain line driver and line receiver

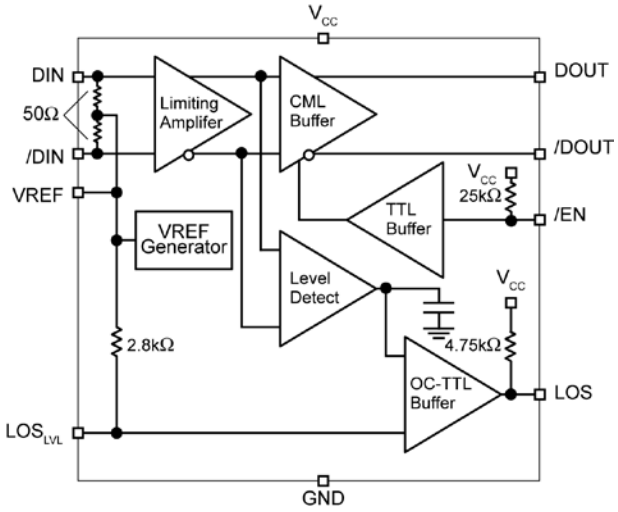
Markets

- Copper interconnect
- Datacom and telecom
- Storage area network (SAN)

Typical Application



Functional Block Diagram



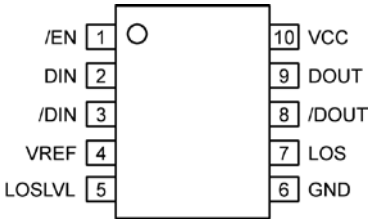
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88403BLEY	K10-2	Industrial	403B with Pb-Free bar-line indicator	Matte-Sn
SY88403BLEYTR[2]	K10-2	Industrial	403B with Pb-Free bar-line indicator	Matte-Sn
SY88403BLMG	QFN-16	Industrial	403B with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY88403BLMGTR[2]	QFN-16	Industrial	403B with Pb-Free bar-line indicator	NiPdAu Pb-Free

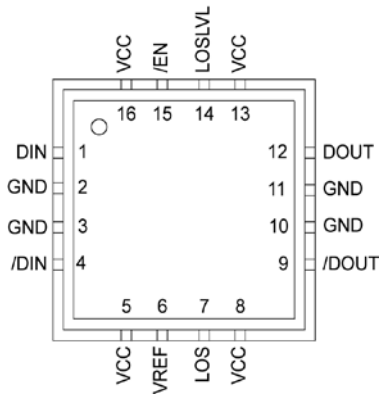
Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.

Pin Configuration



10-Pin EPAD-MSOP (K10-2)



16-Pin QFN

Pin Description

QFN Pin Number	EPAD-MSOP Pin Number	Pin Name	Type	Pin Function
1, 4	2, 3	DIN, /DIN	Differential data input	Differential data input. Each pin internally terminates to REF through 50Ω.
2, 3, 10, 11 Exposed Pad	6 Exposed Pad	GND	Ground	Device ground. Exposed pad must be soldered (or equivalent) to the same potential as the ground pins.
5, 8, 13, 16	10	VCC	Power supply	Positive power supply. Bypass with 0.1µF||0.01µF low ESR capacitors. 0.01µF capacitors should be as close as possible to VCC pin.
6	4	VREF		Reference Voltage. Bypass with 0.01µF low ESR capacitor from V_{REF} to V_{CC} to stabilize LOS_{LVL} and V_{REF}.
7	7	LOS	Open Collector TTL output with internal 4.75kΩ pull-up resistor	Loss-of-Signal: Asserts high when the data input amplitude falls below the threshold set by LOSLVL.
9, 12	9, 8	DOUT, /DOUT	Differential CML output	Differential data output.
14	5	LOSLVL	Input: Default is maximum sensitivity.	Loss-of-Signal level set: A resistor from this pin to VCC sets the threshold for the data input amplitude at which the LOS output will be asserted.
15	1	/EN	TTL input: Default is high.	Enable bar: De-asserts true data output when high. Incorporates 25kΩ pull-up to V_{CC}.

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... 0V to +7.0V
/EN, LOSLVL Voltage..... 0 to V_{CC}
REF Current .....±1mA
LOS Current .....±5mA
DOUT, /DOUT Current.....±25mA
DIN, /DIN Current.....±10mA
Lead Temperature (soldering, 20sec.)..... 260°C
Storage Temperature (T_s) .....–65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}).....+3.0V to +3.6V
Ambient Temperature (T_A)..... –40°C to +85°C
Junction Temperature (T_A)..... –40°C to +120°C
Package Thermal Resistance[3]
QFN
θ_{JA} (Still-Air) ..... 61°C/W
ψ_{JB} ..... 38°C/W
EPAD-MSOP
θ_{JA} (Still-Air) ..... 38°C/W
ψ_{JB} ..... 22°C/W

DC Electrical Characteristics

V_{CC} = +3.0V to +3.6V; T_A = –40°C to +85°C; typical values at V_{CC} = +3.3V, T_A = 25°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	3.3V, Note 4		25	42	mA
		3.3V, Note 5		41	62	mA
V_{REF}	REF Voltage			V_{CC} –1.3		V
V_{LOSLVL}	LOSLVL Voltage Range		V_{REF}		V_{CC}	V
V_{OH}	DOUT, /DOUT HIGH Voltage	Note 6	V_{CC} –0.020	V_{CC} –0.005	V_{CC}	V
V_{OL}	DOUT, /DOUT LOW Voltage	3.3V, Note 6	V_{CC} –0.475	V_{CC} –0.400	V_{CC} –0.350	V
V_{OD_DC}	DC Differential Output Voltage	Note 6	700	800	950	mV
V_{OFFSET}	Differential Output Offset				±80	mV
Z_O	Single-Ended Output Impedance		40	50	60	Ω
Z_I	Single-Ended Input Impedance		40	50	60	Ω

TTL DC Electrical Characteristics

V_{CC} = +3.0V to +3.6V; T_A = –40°C to +85°C.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	LOS Output HIGH Level	Sourcing 100µA	2.4		V_{CC}	V
V_{OL}	LOS Output LOW Level	Sinking 2mA			0.5	V
V_{IH}	/EN Input HIGH Voltage		2.0			V
V_{IL}	/EN Input LOW Voltage				0.8	V
I_{IH}	/EN Input HIGH Current	V_{IN} = 2.7V V_{IN} = V_{CC}			20 100	µA µA
I_{IL}	/EN Input LOW Current	V_{IN} = 0.5V	–0.3			mA

Notes:

1. Permanent device damage may occur if ratings in the absolute maximum ratings section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes are of 4-layer PCB. Exposed pad must be soldered (or equivalent) to the device's most negative potential on the PCB.
4. Excludes current of CML output stage. See “Detailed Description.”
5. Total device current with no output load.
6. Output levels are based on a 50Ω to V_{CC} load impedance. If the load impedance is different, the output level will be changed. Amplifier is in limiting mode. Measured at 155Mbps with 20mVpp input and PRBS-23 data pattern and 50Ω load.

AC Electrical Characteristics

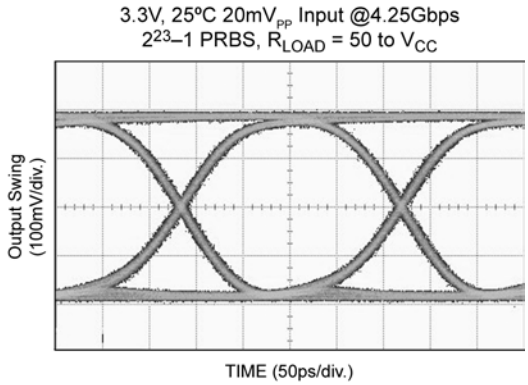
V_{CC} = +3.0V to +3.6V; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC}; typical values at V_{CC} = +3.3V, T_A = 25°C.

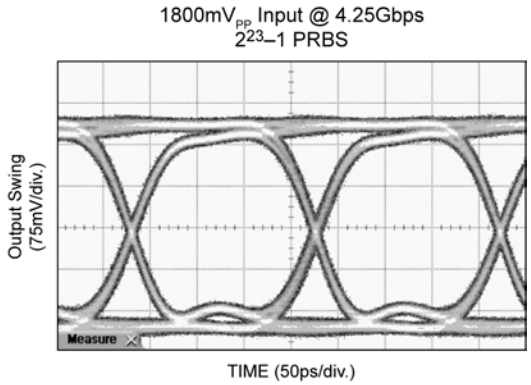
Symbol	Parameter	Condition	Min	Typ	Max	Units
t_r, t_f	Output Rise/Fall Time (20% to 80%)	Note 7		60	120	ps
t_{JITTER}	Deterministic Random	Note 8 Note 9		10 1		ps_{PP} ps_{RMS}
V_{ID}	Differential Input Voltage Swing	See Figure 1	5		1800	mV_{pp}
V_{OD_AC}	AC Differential Output Voltage	Note 10	600	800	950	mV_{pp}
t_{OFF}	LOS Release Time			2	10	µs
t_{ON}	LOS Assert Time			2	10	µs
LOS_{AL}	Low LOS Assert Level	R_{LOSLVL} = 15kΩ, Note 11		8		mV_{PP}
LOS_{DL}	Low LOS De-assert Level	R_{LOSLVL} = 15kΩ, Note 11		12		mV_{PP}
HSY_L	Low LOS Hysteresis	R_{LOSLVL} = 15kΩ, Note 12	2	3.5	4.5	dB
LOS_{AM}	Medium LOS Assert Level	R_{LOSLVL} = 5kΩ, Note 11	12	17		mV_{PP}
LOS_{DM}	Medium LOS De-assert Level	R_{LOSLVL} = 5kΩ, Note 11		25	33	mV_{PP}
HSY_M	Medium LOS Hysteresis	R_{LOSLVL} = 5kΩ, Note 12	2	3.5	4.5	dB
LOS_{AH}	High LOS Assert Level	R_{LOSLVL} = 100Ω, Note 11	34	47		mV_{PP}
LOS_{DH}	High LOS De-assert Level	R_{LOSLVL} = 100Ω, Note 11		70	83	mV_{PP}
HSY_H	High LOS Hysteresis	R_{LOSLVL} = 100Ω, Note 12	2	3.5	4.5	dB
V_{SR}	LOS Sensitivity Range		20		35	mV_{PP}
$A_{V(Diff)}$	Differential Voltage Gain		32	38		dB
S_{21}	Single-Ended Small-Signal Gain		26	32		dB

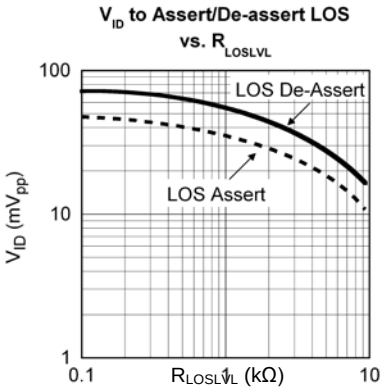
Notes:

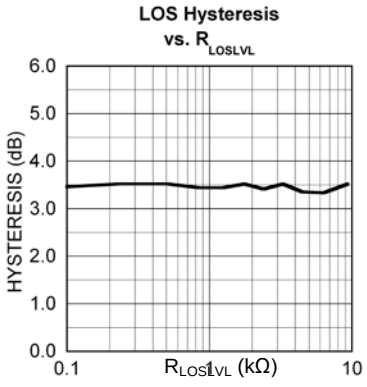
7. Amplifier in limiting mode. Input is a 200MHz square wave.
8. Deterministic jitter measured using 4.25Gbps K28.5 pattern, V_{ID} = 20mV_{PP}.
9. Random jitter measured using 4.25Gbps K28.7 pattern, V_{ID} = 20mV_{PP}.
10. Differential output swing measured at 4.25Gbps with 20mVpp input and PRBS-23 data pattern and 50Ω load.
11. See “Typical Operating Characteristics” for a graph showing how to choose a particular R_{LOSLVL} for a particular LOS assert and its associated de-assert amplitude.
12. This specification defines electrical hysteresis as 20log(LOS De-assert/LOS Assert). The ratio between optical hysteresis and electrical hysteresis is found to vary between 1.5 and 2 depending on the level of received optical power and ROSA characteristics. Based on that ratio, the optical hysteresis corresponding to the electrical hysteresis range 2dB-4.5 dB shown in the AC characteristics table will be 0.5dB-3dB Optical Hysteresis.

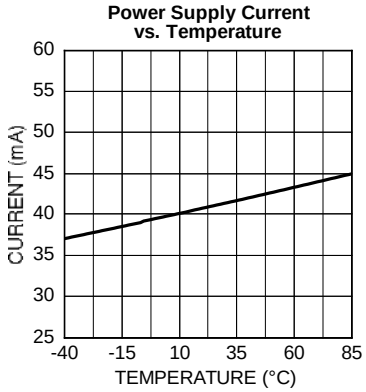
Typical Operating Characteristics

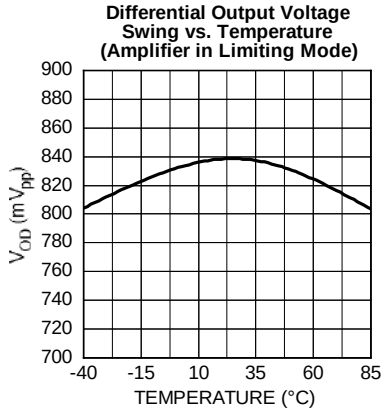


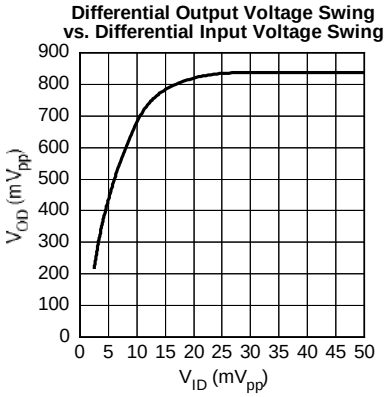












Detailed Description

The SY88403BL low-power limiting post amplifier operates from a single +3.3V power supply, over temperatures from –40°C to +85°C. Signals with data rates up to 4.25Gbps and as small as $5mV_{PP}$ can be amplified. Figure 1 shows the allowed input voltage swing. The SY88403BL generates an LOS output, allowing feedback to /EN for output stability. LOSLVL sets the sensitivity of the input amplitude detection.

Input Amplifier/Buffer

The SY88403BL's inputs are internally terminated with 50Ω to REF. If not affected by this internal termination scheme, upstream devices need to be AC-coupled to the SY88403BL's inputs. Figure 2 shows a simplified schematic of the input stage.

The high-sensitivity of the input amplifier allows signals as small as $5mV_{PP}$ to be detected and amplified. The input amplifier allows input signals as large as $1800mV_{PP}$. Input signals are linearly amplified with a typically 38dB differential voltage gain. Since it is a limiting amplifier, the SY88403BL outputs typically $800mV_{PP}$ voltage-limited waveforms for input signals that are greater than $20mV_{PP}$. Applications requiring the SY88403BL to operate with high-gain should have the upstream TIA placed as close as possible to the SY88403BL's input pins to ensure the best performance of the device.

Output Buffer

The SY88403BL's CML output buffer is designed to drive 50Ω lines. The output buffer requires appropriate termination for proper operation. An external 50Ω resistor to V_{CC} or equivalent for each output pin provides this. Figure 3 shows a simplified schematic of the output stage and includes an appropriate termination method. Of course, driving a downstream device with a CML input that is internally terminated with 50Ω to V_{CC} eliminates the need for external termination. As noted in the previous section, the amplifier outputs typically $800mV_{PP}$ waveforms across 25Ω total loads. The output buffer thus switches typically 16mA tail-current. Figure 4 shows the power supply current measurement, which excludes the 16mA tail-current.

Loss-of-Signal

The SY88403BL incorporates a chatter-free loss-of-signal (LOS) open-collector TTL output with internal 4.75kΩ pull-up resistor as shown in Figure 5. LOS is used to determine that the input amplitude is too small to be considered a valid input. LOS asserts high if the input amplitude falls below the threshold set by LOSLVL and de-asserts low otherwise. LOS can be fed back to the enable (/EN) input to maintain output stability under a loss of signal condition. /EN de-asserts low the true output signal without removing the input signals. Typically 3.5dB LOS hysteresis is provided to prevent chattering.

Loss-of-Signal Level Set

A programmable loss-of-signal level set pin (LOSLVL) sets the threshold of the input amplitude detection. Connecting an external resistor between V_{CC} and LOSLVL sets the voltage at LOSLVL. This voltage ranges from V_{CC} to V_{REF}. The external resistor creates a voltage divider between V_{CC} and VREF as shown in Figure 6. If desired, an appropriate external voltage may be applied rather than using a resistor. The relationship between V_{LOSLVL} and R_{LOSLVL} is given by:

$$V_{LOSLVL} = V_{CC} - \left(1.3\frac{R_{LOSLVL}}{R_{LOSLVL} + 2.8}\right)$$

where voltages are in volts and resistances are in kΩ.

The smaller the external resistor, implying a smaller voltage difference from LOSLVL to VCC, lowers the LOS sensitivity. Hence, larger input amplitude is required to de-assert LOS. "Typical Operating Characteristics" contains graphs showing the relationship between the input amplitude detection sensitivity and R_{LOSLVL}.

Hysteresis

The SY88403BL provides typically 3.5dB LOS electrical hysteresis. By definition, a power ratio measured in dB is 10log (power ratio). Power is calculated as V_{IN}^2/R for an electrical signal. Hence the same ratio can be stated as 20log (voltage ratio). While in linear mode, the electrical voltage input changes linearly with the optical power and hence the ratios change linearly. Therefore, the optical hysteresis in dB is half the electrical hysteresis in dB given in the datasheet. The SY88403BL provides typically 1.75dB LOS optical hysteresis. As the SY88403BL is an electrical device, this datasheet refers to hysteresis in electrical terms. With 3.5dB LOS hysteresis, a voltage factor of 1.5 is required to de-assert LOS.

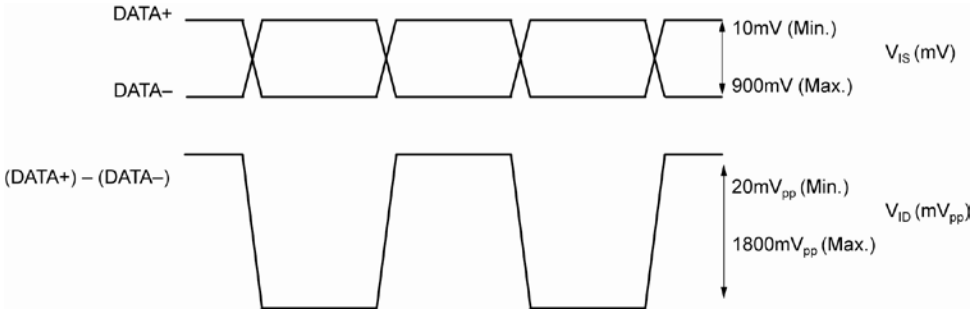


Figure 1. V_{IS} and V_{ID} Definition

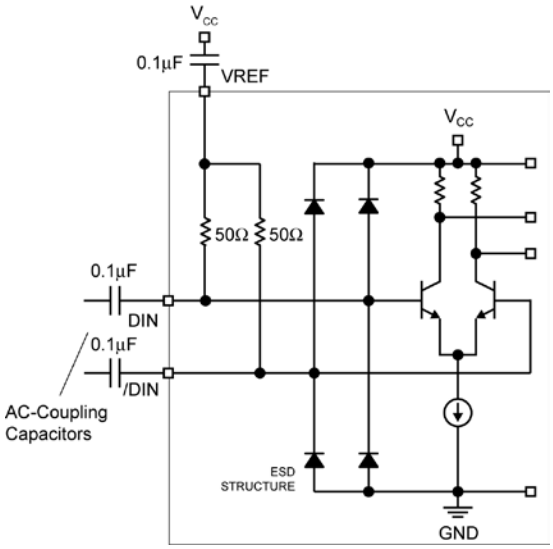


Figure 2. Input Structure

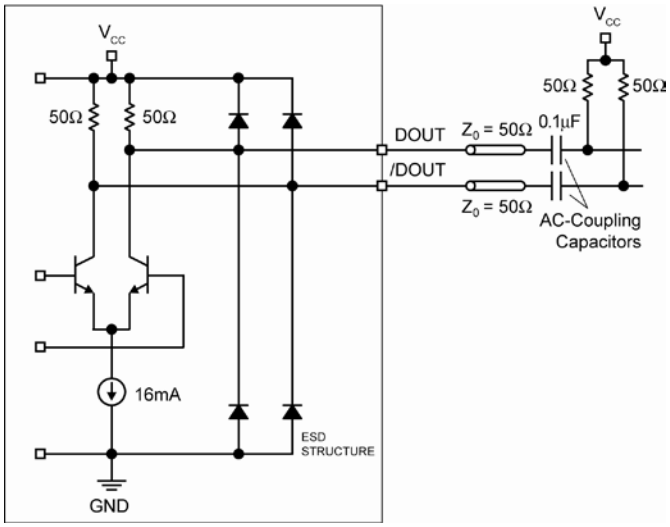


Figure 3. Output Structure

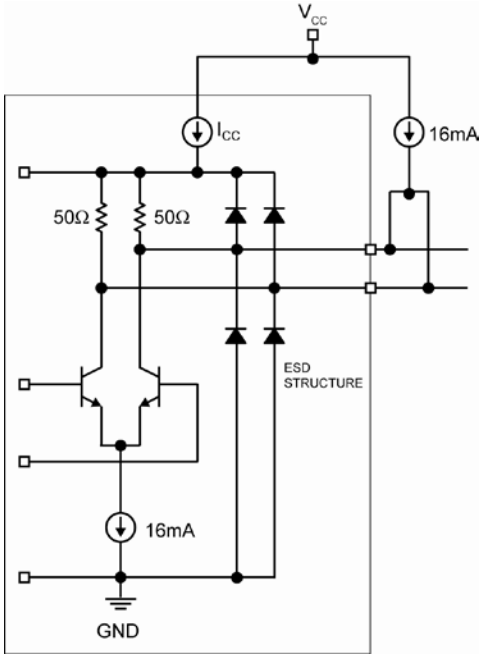


Figure 4. Power Supply Current Measurement

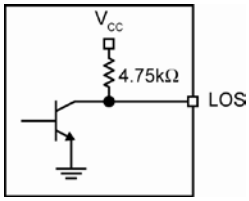


Figure 5. LOS Output Structure

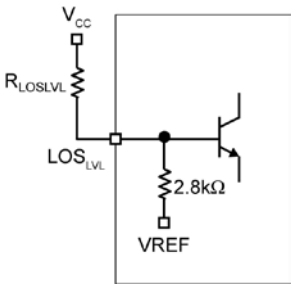
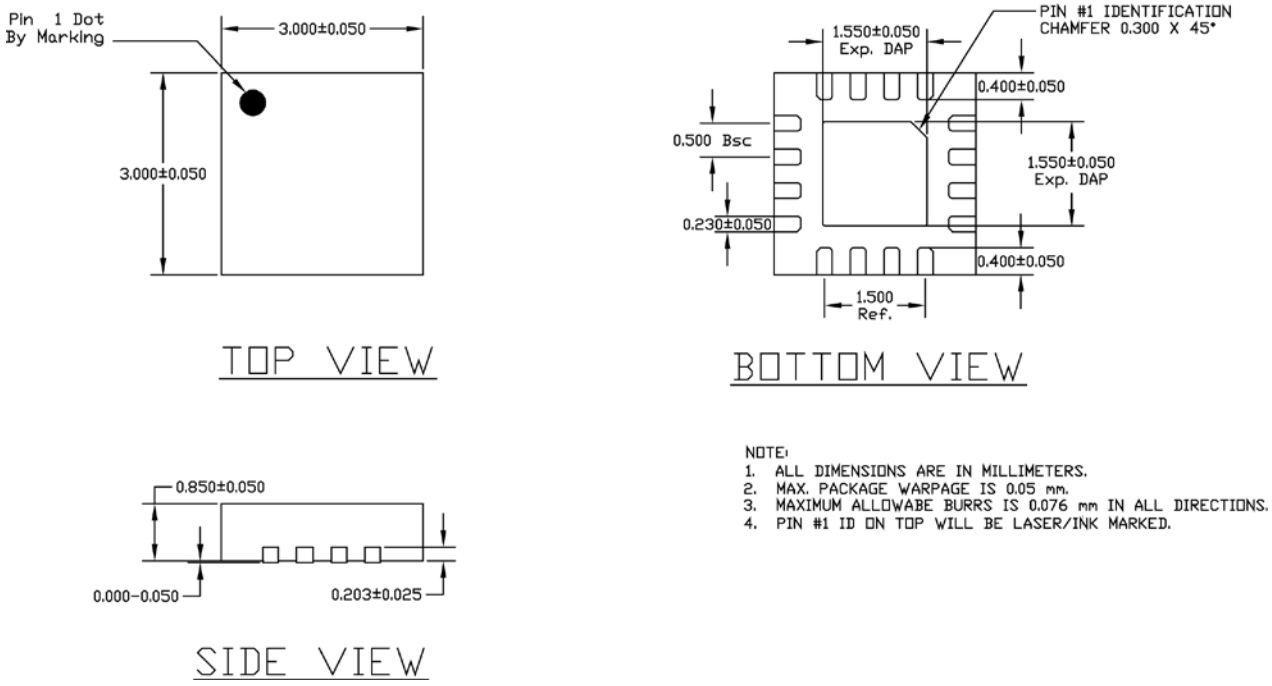


Figure 6. LOSLVL Setting Circuit

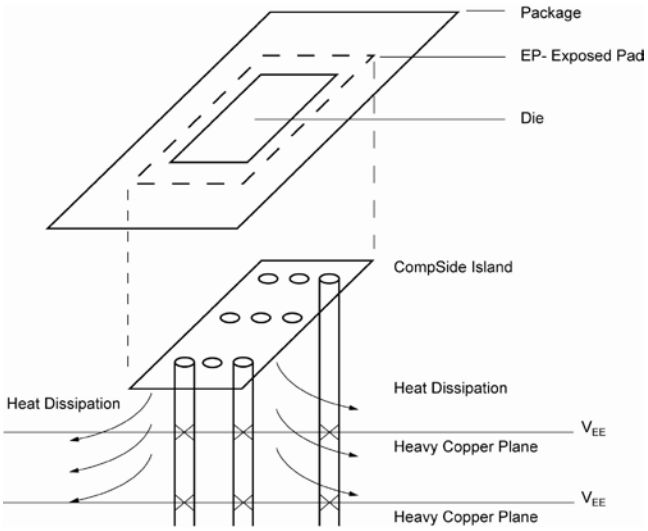
Related Product and Support Documentation

Part Number	Function	Data Sheet Link
Application Notes	Notes on Sensitivity and Hysteresis in Micrel Post Amplifier	www.micrel.com/product-info/app_hints+notes.shtml

Package Information



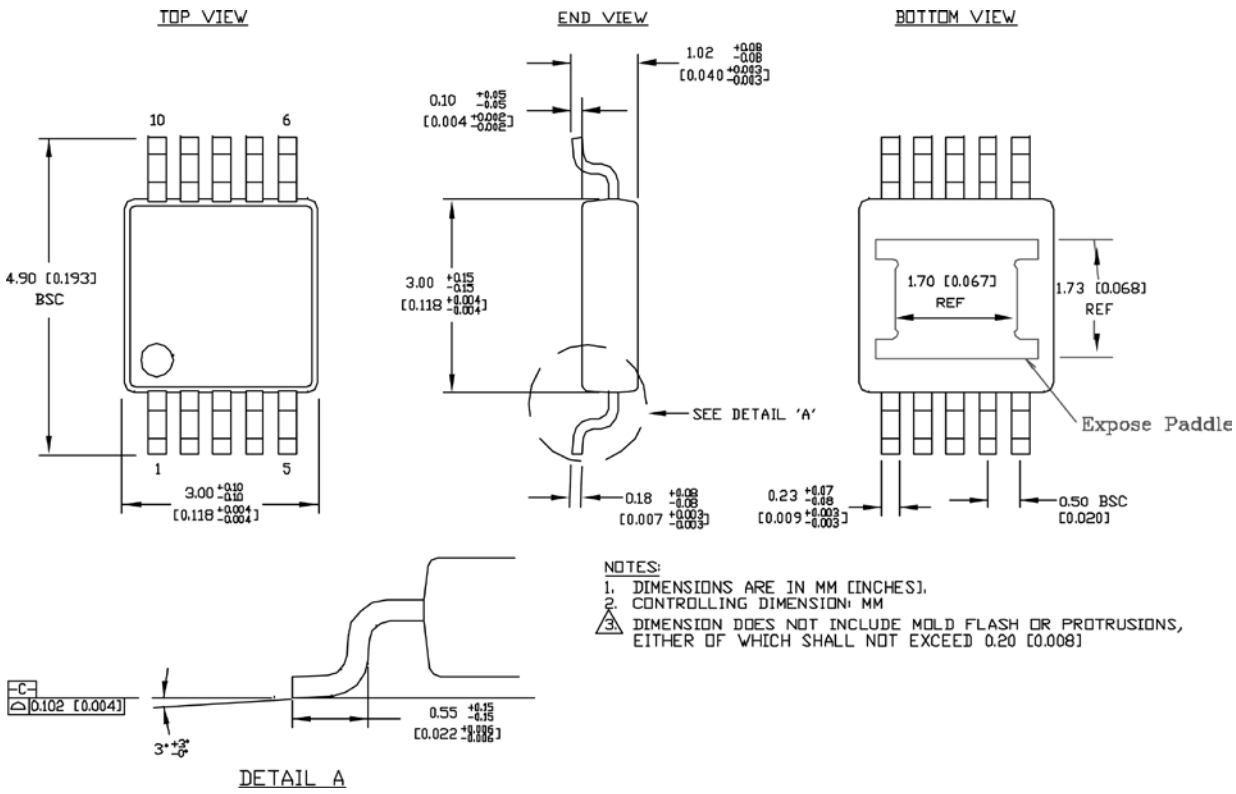
16-Pin QFN



PCB Thermal Consideration for 16-Pin QFN Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.



10-Pin EPAD-MSOP (K10-2)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com