# PI6C4911505-07

## High Performance 1:5 LVPECL Fanout Buffer

## Features

- 5 LVPECL outputs
- Up to 1.5GHz output frequency
- Ultra low additive phase jitter: < 0.03 ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Two selectable inputs
- Low delay from input to output (Tpd typ. 1.2ns)
- Separate Input output supply voltage for level shifting
- 2.5V / 3.3V power supply
- Industrial temperature support
- TSSOP-20 package

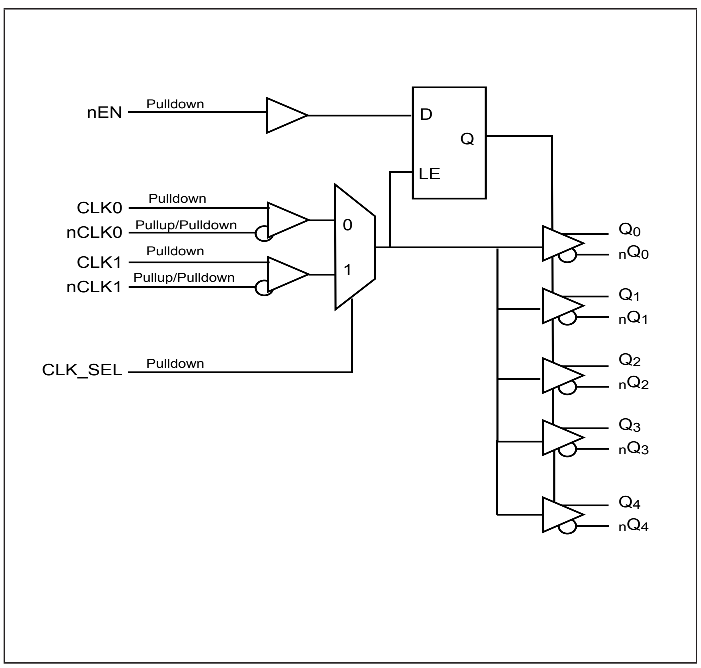
## Description

The PI6C4911505-07 is a high performance fanout buffer device-which supports up to 1.5GHz frequency. The device has 2 selectable clock inputs that can accept most differential clock sources. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

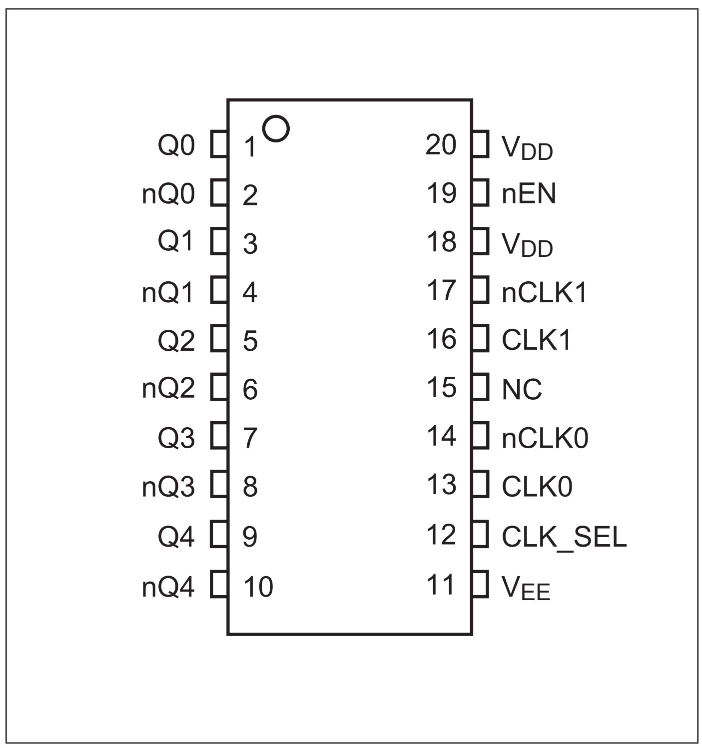
## Applications

- Networking systems including switches and Routers
- High frequency backplane based computing and telecom platforms

## Block Diagram




## Pin Configuration (20-Pin TSSOP)



## Pinout Table

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 1, 2 | Q0<br>nQ0 | Output | LVPECL output clock |
| 3, 4 | Q1<br>nQ1 | Output | LVPECL output clock |
| 5, 6 | Q2<br>nQ2 | Output | LVPECL output clock |
| 7, 8 | Q3<br>nQ3 | Output | LVPECL output clock |
| 9, 10 | Q4<br>nQ4 | Output | LVPECL output clock |
| 11 | $V_{EE}$ | Power | Negative power supply |
| 12 | CLK_SEL | Input | Clock input source selection pin |
| 13, 14 | CLK0<br>nCLK0 | Input | Differential clock input. LVPECL, LVECL, LVDS, CML, HSTL, HCSL |
| 15 | NC | - | No Connect |
| 16, 17 | CLK1<br>nCLK1 | Input | Differential clock input. LVPECL, LVECL, LVDS, CML, HSTL, HCSL |
| 18, 20 | $V_{DD}$ | Power | Power supply |
| 19 | nEN | Input | Synchronizing clock enable. When LOW, clock outputs enabled. When HIGH, Q outputs are forced low, nQ outputs forced high. |

## Function Table

Table 1: Input select function

| CLK_SEL | Function |
|---|---|
| 0 | CLK0, nCLK0 |
| 1 | CLK1, nCLK1 |

Table 2: Output Mode select function

| nEN | Outputs | |
|---|---|---|
| | Q0:Q4 | nQ0:nQ4 |
| 1 | Disabled; LOW | Disabled; HIGH |
| 0 | Enabled | Enabled |

Table 3: Input select function

| Input | | Output | | Device Mode |
|---|---|---|---|---|
| CLK0 / CLK1 | nCLK0 / nCLK1 | Q0:Q4 | nQ0:nQ4 | |
| LOW | HIGH | LOW | HIGH | Diff. -> Diff., Non-Inverting |
| HIGH | LOW | HIGH | LOW | Diff. -> Diff., Non-Inverting |
| LOW | Biased, Figure 1 | LOW | HIGH | S-E -> Diff., Non-Inverting |
| HIGH | Biased, Figure 1 | HIGH | LOW | S-E -> Diff., Non-Inverting |
| Biased, Figure 1 | LOW | HIGH | LOW | S-E -> Diff., Inverting |
| Biased, Figure 1 | HIGH | LOW | HIGH | S-E -> Diff., Inverting |

## Maximum Ratings (Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature....................................................-55 to +150°C
Supply Voltage $V_{DD}$ (Referenced to $V_{EE}$)................ -0.5 to +4.6V
Inputs (Referenced to $V_{EE}$)................................ -0.5 to $V_{DD}$+0.5V
Clock Output (Referenced to $V_{EE}$).................... -0.5 to $V_{DD}$+0.5V

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Power Supply Characteristics and Operating Conditions

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | | 3.0 | 3.3 | 3.6 | V |
| | | | 2.375 | 2.5 | 2.625 | |
| $V_{EE}$ | Negative supply voltage | | -0.5 | | | |
| $I_{DD}$ | Power Supply Current | Outputs unloaded | | | 120 | mA |
| $T_A$ | Ambient Operating Temperature | | -40 | | 85 | °C |

## DC Electrical Specifications - Differential Inputs

| Symbol | Parameter | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High current: CLK0, CLK1 | Input = $V_{DD}$ | | | 150 | uA |
| | Input High current: nCLK0, nCLK1 | Input = $V_{DD}$ | | | 150 | uA |
| $I_{IL}$ | Input Low current: CLK0, CLK1 | Input = GND | -5 | | | uA |
| | Input Low current: nCLK0, nCLK1 | Input = GND | -150 | | | uA |
| $C_{IN}$ | Input capacitance | | | 4 | | PF |
| $V_{IH}$ | Input high voltage | | | | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input low voltage | | -0.3 | | | V |
| $V_{ID}$ | Input Differential Amplitude PK-PK | | 0.15 | | $V_{DD}$-0.85 | V |
| $V_{CM}$ | Common model input voltage | | $V_{EE}$+0.5 | | $V_{DD}$-0.85 | V |

## DC Electrical Specifications - LVCMOS Inputs

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $I_{IH}$ | Input High current | Input = $V_{DD}$ | | | 150 | uA |
| $I_{IL}$ | Input Low current | Input = GND | -150 | | | uA |
| $V_{IH}$ | Input high voltage | $V_{DD}$=3.3V | 2.0 | | 3.765 | V |
| $V_{IL}$ | Input low voltage | $V_{DD}$=3.3V | -0.3 | | 0.8 | V |
| $V_{IH}$ | Input high voltage | $V_{DD}$=2.5V | 1.7 | | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input low voltage | $V_{DD}$=2.5V | -0.3 | | 0.7 | V |

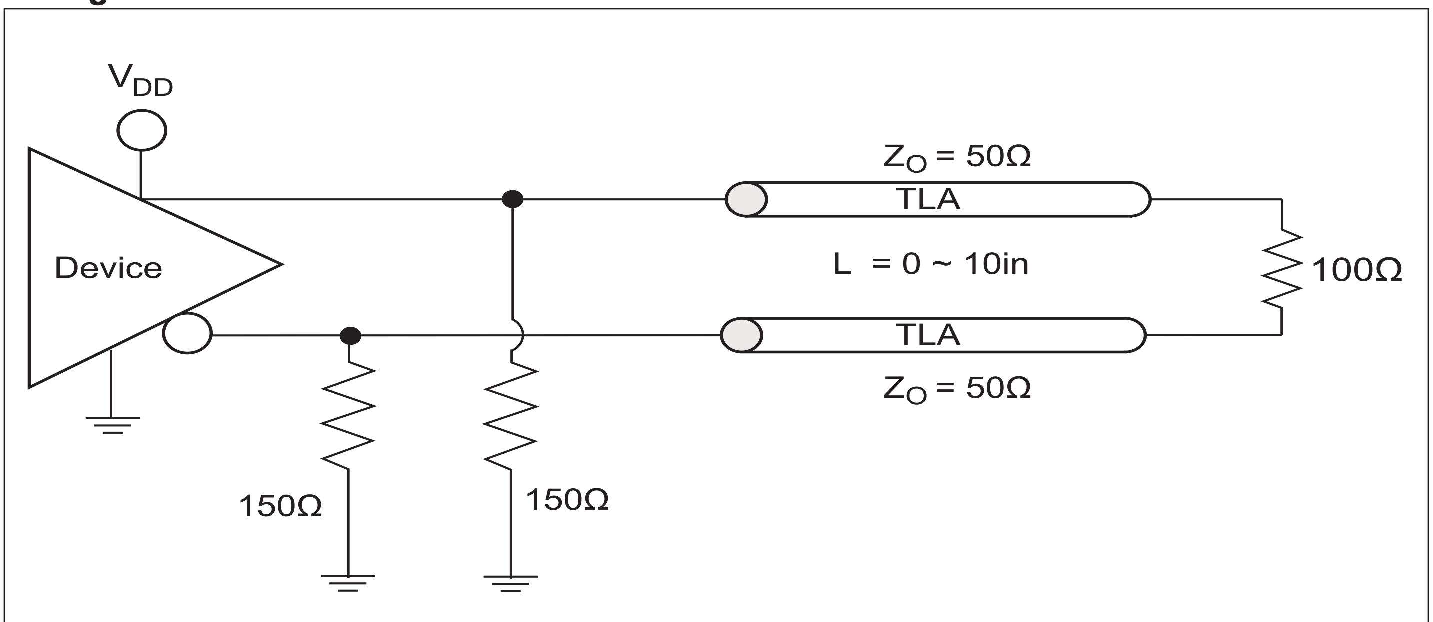
## DC Electrical Specifications- LVPECL Outputs

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High voltage | $V_{DD}$=3.3V | 2.1 | | 2.6 | V |
| | | $V_{DD}$=2.5V | 1.3 | | 1.6 | |
| $V_{OL}$ | Output Low voltage | $V_{DD}$=3.3V | 1.3 | | 1.8 | V |
| | | $V_{DD}$=2.5V | 0.5 | | 1.0 | |

## AC Electrical Specifications

| Parameter | Description | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $F_{OUT}$ | Clock output frequency | LVPECL | | | 1500 | MHz |
| $T_r$ | Output rise time | From 20% to 80% | | 150 | | ps |
| $T_f$ | Output fall time | From 80% to 20% | | 150 | | ps |
| $T_{ODC}$ | Output duty cycle | Frequency<650MHz, LVPECL input used | 48 | | 52 | % |
| $V_{PP}$ | Output swing Single-ended | Frequency<650MHz | 400 | | | mV |
| $T_j$ | Buffer additive jitter RMS | Differential clock input | | 0.03 | | ps |
| $T_{SK}$ | Output Skew | | | | 70 | ps |
| $T_{PD}$ | Propagation Delay | | | 1200 | | ps |
| $T_{P2P\ Skew}$ | Part to Part Skew | | | | 150 | ps |

## Configuration Test Load Board Termination for LVPECL



# Application information

## Suggest for Unused Inputs and Outputs

**LVCMOS Input Control Pins**

It is suggested to add pull-up=4.7k and pull-down=1k for LVCMOS pins even though they have internal pull-up/down but with much higher value (>=50k) for higher reliability design.

**Differential +IN/-IN Input Pins**

They can be left floating if not used. Connect them 1k to GND is optional for the additional protection.

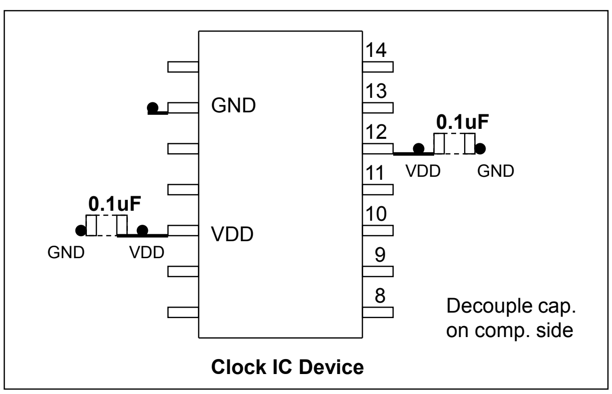
**Outputs**

All unused outputs are suggested to be left open and not connected to any trace. This can lower the IC power supply power.

## Power Decoupling & Routing

**VDD Pin Decoupling**

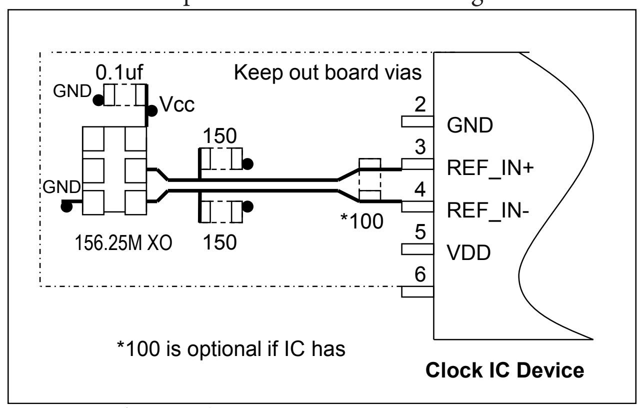
As general design rule, each VDD pin must have a 0.1uF decoupling capacitor. For better decoupling, 1uF can be used. Locating the decoupling capacitor on the component side has better decoupling filter result as shown below.




Placement of Decoupling caps

**Differential Clock Trace Routing**

Always route differential signals symmetrically, make sure there is enough keep-out space to the adjacent trace (>20mil.). In 156.25MHz XO drives IC example, it is better routing differential trace on component side as the following.



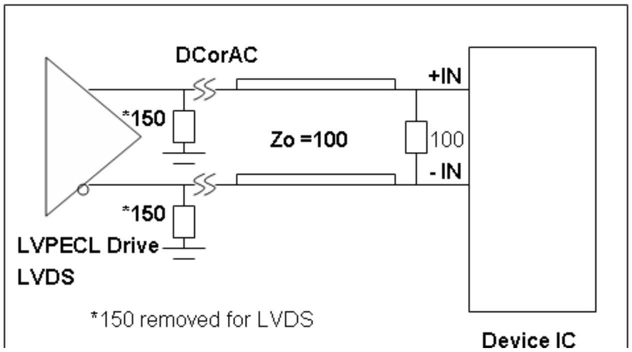

IC routing for XO drive

Clock timing is the most important component in PCB design, so its trace routing must be planned and routed as a first priority in manual routing. Some good practices are to use minimum vias (total trace vias count <4), use independent layers with good reference plane and keep other signal traces away from clock traces (>20mil.) etc.

## LVPECL and LVDS Input Interface

### LVPECL and LVDS DC/ AC Input

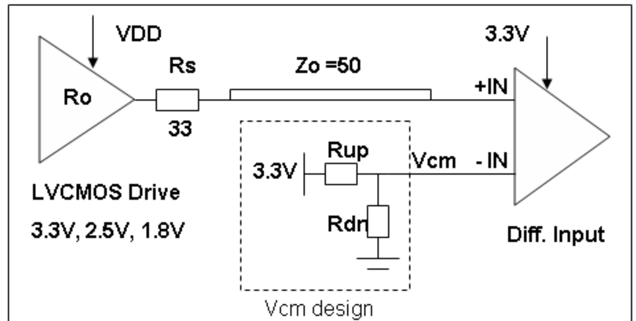
LVPECL and LVDS clock input to this IC is connected as shown below.




LVPECL/ LVDS Input

### CMOS Clock DC Drive Input

LVCMOS clock has voltage Voh levels such as 3.3V, 2.5V, 1.8V. CMOS drive requires a Vcm design at the input: Vcm= ½ (CMOS V) as shown below 7. Rs =22 ~33ohm typically.



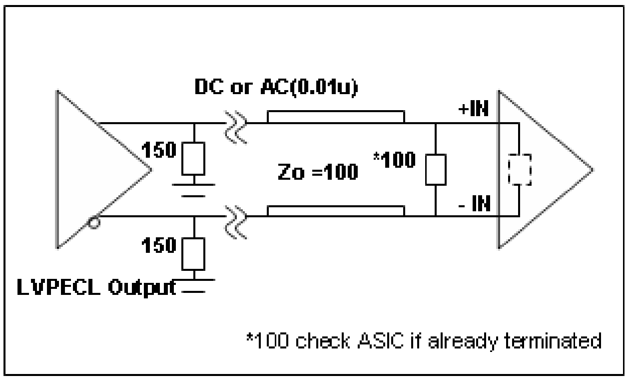

| VDD V | Rup | Rdn | Vcm |
|---|---|---|---|
| 3.3V | 1k | 1k | 1.65V |
| 2.5V | 1k | 610 | 1.25V |
| 1.8V | 1k | 380 | 0.9V |

CMOS DC Input Vcm Design

## Device LVPECL Output Terminations

### LVPECL Output Popular Termination

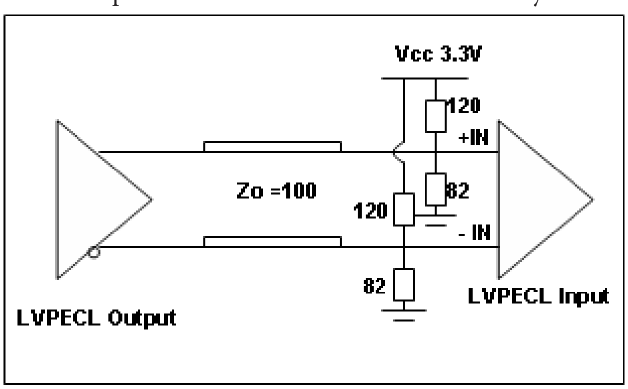
The most popular LVPECL termination is 150ohm pull-down bias and 100ohm across at RX side. Please consult ASIC datasheet if it already has 100ohm or equivalent internal termination. If so, do not connect external 100ohm across as shown in below. This popular termination's advantage is that it does not allow any bias through from Vcc. This prevents Vcc system noise coupling onto clock trace.




LVPECL Output Popular Termination

### LVPECL Output Thevenin Termination

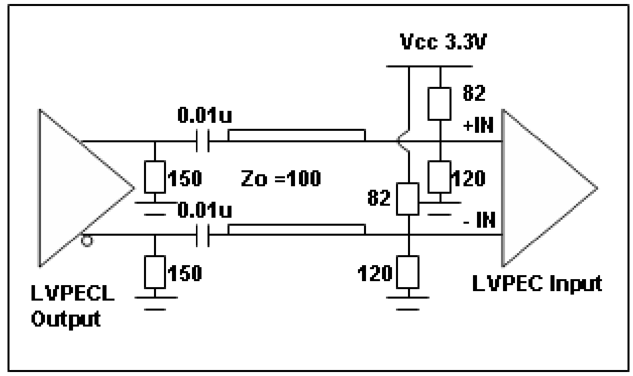
Figure below shows LVPECL output Thevenin termination which is used for shorter trace drive (<5in.), but it takes Vcc bias current and Vcc noise can get onto clock trace. It also requires more component count. So it is seldom used today.




LVPECL Thevenin Output Termination

### LVPECL Output AC Thevenin Termination

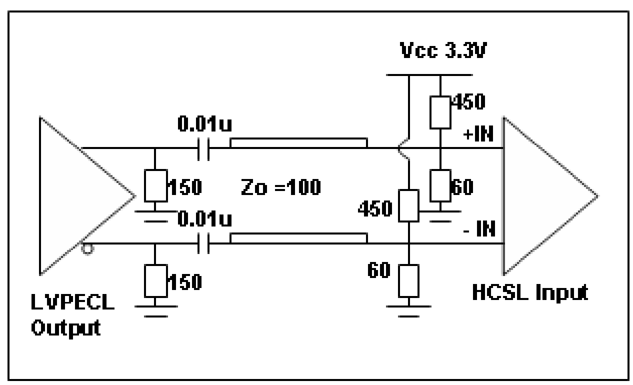
LVPECL AC Thevenin terminations require a 150ohm pull-down before the AC coupling capacitor at the source as shown below. Note that pull-up/down resistor value is swapped compared to previous figure.  This circuit is good for short trace (<5in.) application only.




LVPECL Output AC Thenvenin Termination

### LVPECL Output Drive HCSL Input

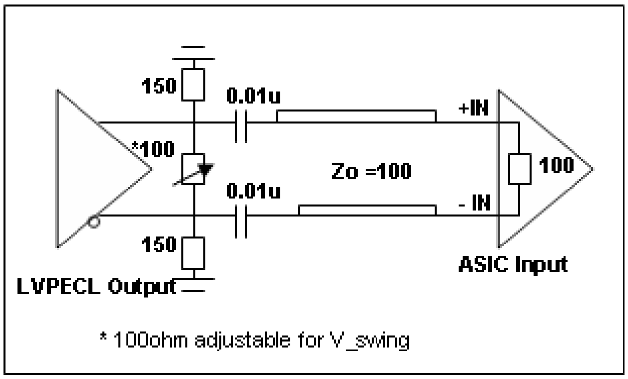
Using the LVPECL output to drive a HCSL input can be done using a typical  LVPECL AC Thenvenin termination scheme. Use pull-up/down 450/60ohm to generate Vcm=0.4V for the HCSL input  clock. This termination is equivalent to 50Ohm load as shown.




LVPECL Output Drive HCSL Termination

**LVPECL Output V_swing Adjustment**

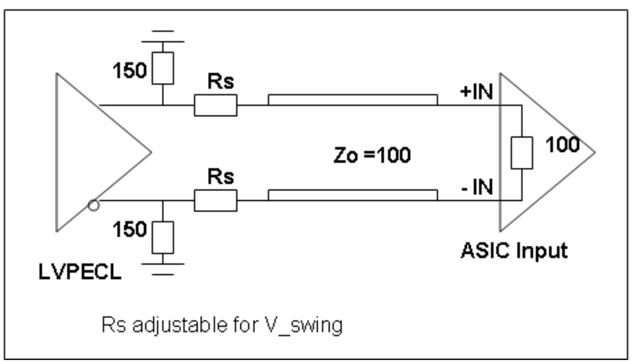
It is suggested to add another cross 100ohm at TX side to tune the LVPECL output V_swing without changing the optimal 150ohm pull-down bias. This form of double termination can reduce the V_swing in ½ of the original at the RX side. By fine tuning the 100ohm resistor at the TX side with larger values like 150 to 200ohm, one can increase the V_swing by > 1/2 ratio.




LVPECL Output V_swing Adjustment

**LVPECL V_swing Adjustment using Rs**

Another way to control V_swing is by adding serial Rs. Rs value is tunable between 22 to 33 ohm depending on application. This method may reduce the clock drive PCB trace in slower Tr/Tf .




LVPECL V_swing Adjustment using Rs

## Clock Jitter Definitions

**Total jitter= RJ + DJ**

Random Jitter (RJ) is unpredictable and unbounded timing noise that can fit in a Gaussian math distribution in RMS. RJ test values are directly related with how long or how many test samples are available. Deterministic Jitter (DJ) is timing jitter that is predictable and periodic in fixed interference frequency. Total Jitter (TJ) is the combination of random jitter and deterministic jitter: , where is a factor based on total test sample count. JEDEC std. specifies digital clock TJ in 10k random samples.

**Phase Jitter**

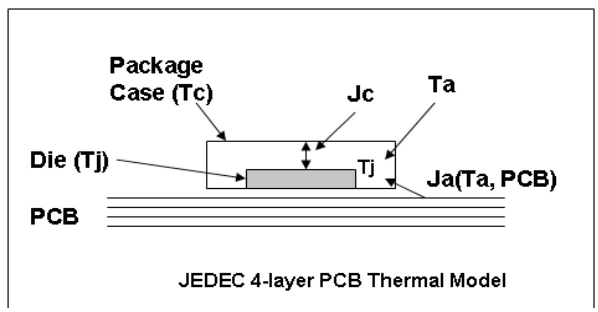
Phase noise is short-term random noise attached on the clock carrier and it is a function of the clock offset from the carrier, for example dBc/Hz@10kHz which is phase noise power in 1-Hz normalized bandwidth vs. the carrier power @10kHz offset. Integration of phase noise in plot over a given frequency band yields RMS phase jitter, for example, to specify phase jitter <=1ps at 12k to 20MHz offset band as SONET standard specification.

**PCIe Ref_CLK Jitter**

PCIe reference clock jitter specification requires testing via the PCI-SIG jitter tool, which is regulated by US PCI-SIG organization. The jitter tool has PCIe Serdes embedded filter to calculate the equivalent jitter that relates to data link eye closure. Direct peak-peak jitter or phase jitter test data, normally is higher than jitter measure using PCI-SIG jitter tool. It has high-frequency jitter and low-frequency jitter spec. limit. For more information, please refer to the PCI-SIG website: http://www.pcisig.com/specifications/pciexpress/

## Device Thermal Calculation

Figure below shows the JEDEC thermal model in a 4-layer PCB.




JEDEC IC Thermal Model

Important factors to influence device operating temperature are:

1) The power dissipation from the chip (P_chip) is after subtracting power dissipation from external loads. Generally it can be the no-load device Idd

2) Package type and PCB stack-up structure, for example, 1oz 4 layer board. PCB with more layers and are thicker has better heat dissipation

3) Chassis air flow and cooling mechanism. More air flow M/s and adding heat sink on device can reduce device final die junction temperature Tj

The individual device thermal calculation formula:

**Tj =Ta + Pchip x Ja**

**Tc = Tj - Pchip x Jc**

Ja ___ Package thermal resistance from die to the ambient air in C/W unit; This data is provided in JEDEC model simulation. An air flow of 1m/s will reduce Ja (still air) by 20~30%

Jc ___ Package thermal resistance from die to the package case in C/W unit

Tj ___ Die junction temperature in C (industry limit <125C max.)

Ta ___ Ambiant air température in C

Tc ___ Package case temperature in C

Pchip___ IC actually consumes power through Iee/GND current

**Thermal calculation example**
To calculate Tj and Tc of PI6CV304 in an SOIC-8 package:
Step 1: Go to Pericom web to find Ja=157 C/W, Jc=42 C/W
http://www.pericom.com/support/packaging/packaging-mechanicals-and-thermal-characteristics/

Step 2: Go to device datasheet to find Idd=40mA max.

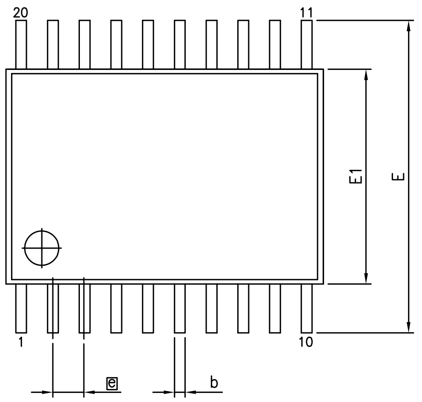
| | | | | | | |
|---|---|---|---|---|---|---|
| $I_{DD}$ | Supply Current | $C_L$ = 33pF/33MHz | | 20 | | mA |
| | | $C_L$ = 33pF/66MHz | | 40 | | |
| | | $C_L$ = 22pF/80MHz | | 35 | | |
| | | $C_L$ = 15pF/100MHz | | 32 | | |
| | | $C_L$ = 10pF/125MHz | | 28 | | |
| | | $C_L$ = 10pF/155MHz | | 41 | | |

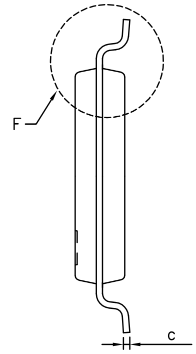
Step 3: P_total= 3.3Vx40mA=0.132W
Step 4: If Ta=85C
Tj= 85 + Ja xP_total= 85+25.9 = 105.7C
Tc= Tj + Jc xP_total= 105.7- 5.54 = 100.1C
Note:
The above calculation is directly using Idd current without subtracting the load power, so it is a conservative estimation. For more precise thermal calculation, use P_unload or P_chip from device Iee or GND current to calculate Tj, especially for LVPECL buffer ICs that have a 150ohm pull-down and equivalent 100ohm differential RX load.

## Thermal Information

| Symbol | Description | Condition | |
|---|---|---|---|
| $\Theta_{JA}$ | Junction-to-ambient thermal resistance | Still air | 84.0 $^{O}$C/W |
| $\Theta_{JC}$ | Junction-to-case thermal resistance | | 17.0 $^{O}$C/W |

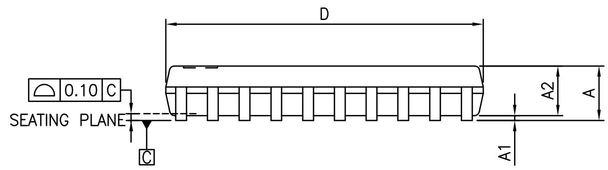
## Packaging Mechanical: 20-Pin TSSOP (L)

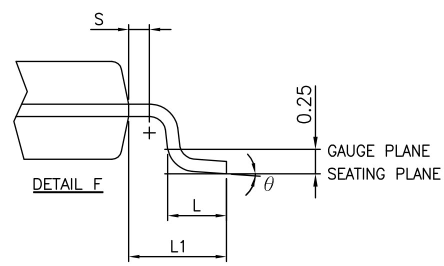



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | – | – | 1.20 |
| A1 | 0.05 | – | 0.15 |
| A2 | 0.80 | – | 1.05 |
| b | 0.19 | – | 0.30 |
| C | 0.09 | – | 0.20 |
| D | 6.40 | 6.50 | 6.60 |
| E1 | 4.30 | 4.40 | 4.50 |
| E | 6.40 BSC | | |
| e | 0.65 BSC | | |
| L1 | 1.00 REF | | |
| L | 0.45 | 0.60 | 0.75 |
| S | 0.20 | – | – |
| θ | 0° | – | 8° |




lotes:
. Refer JEDEC MO-153F/AC
. Controlling dimensions in millimeters
. Package outline exclusive of mold flash and metal burr

PERICOM® Enabling Serial Connectivity

**DATE: 05/03/12**

**DESCRIPTION: 20-pin, 173mil Wide TSSOP**

**PACKAGE CODE: L**

**DOCUMENT CONTROL #: PD-1311** **REVISION: F**

## Ordering Information(1-3)

| Ordering Code | Package Code | Package Description |
|---|---|---|
| PI6C4911505-07LIE | L | 20-pin, TSSOP, Pb-Free and Green |
| PI6C4911505-07LIEX | L | 20-pin, TSSOP, Pb-Free and Green, Tape & Reel |

**Notes:**

1. 1Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free and Green
3. Adding an X suffix = Tape/Reel