MX98741

XRC
100 BASE-TX/FX
REPEATER CONTROLLER

1.0 FEATURES

- Eight 100 BASE-TX/FX ports; each port individually configurable to TX or FX
- Direct interface with analog clock generation/recovery chips
- Three Media Independent Interface (MII)
- Expandable to increase number of repeater ports
- Low latency design simplified high port number Class II repeater implementation
- Management features accessible through MII or serial ports
- All ports can be separately isolated or partitioned in reponse to fault conditions
- Conforms to IEEE 802.3u Repeater Unit Specification
- LED display for TX/FX port activities and collisions
- 208-pin, CMOS device in PQFP package

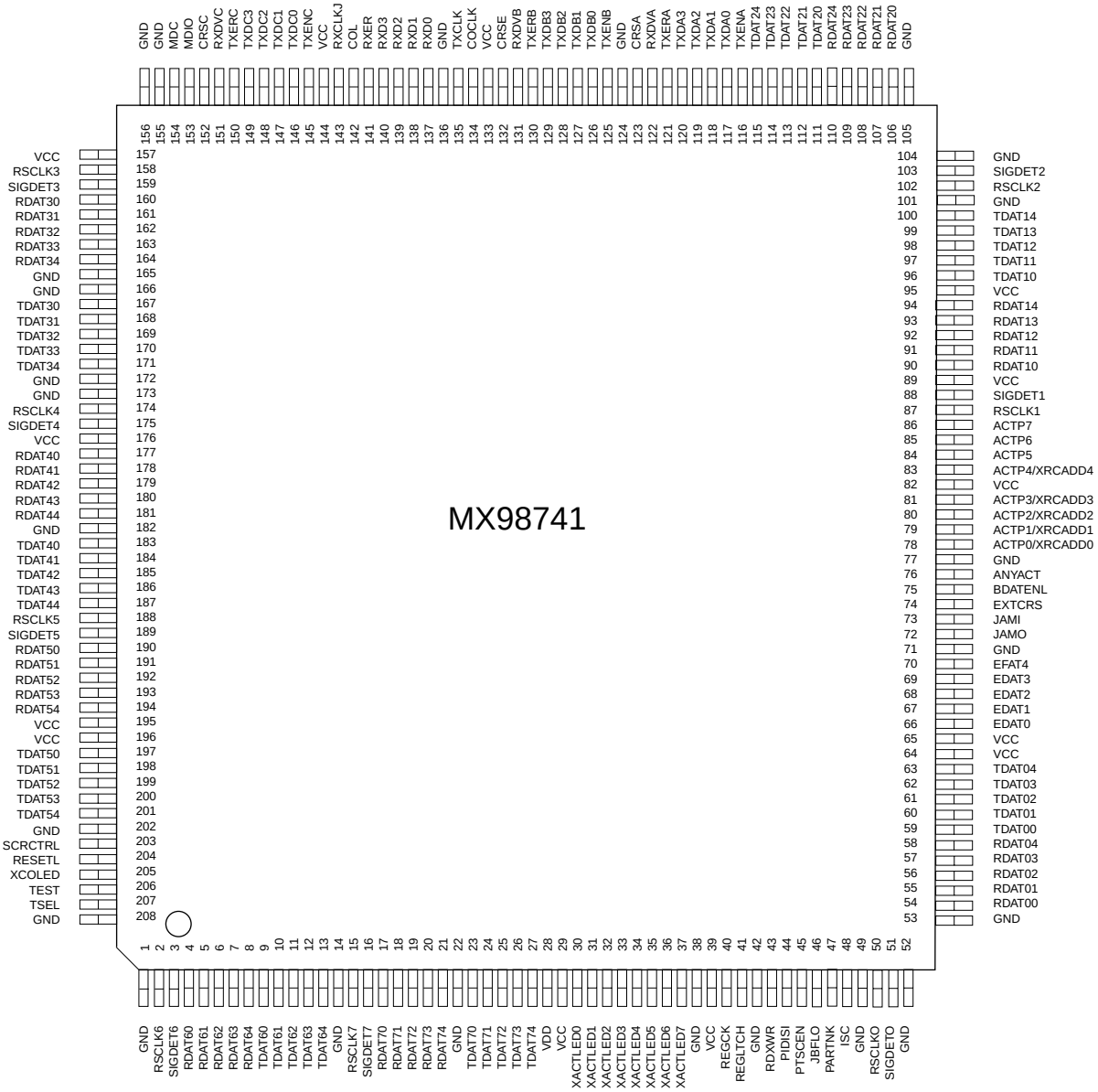
2.0 GENERAL DESCRIPTION

The MX98741 (100BASE-TX Repeater Controller, XRC) is a 208-pin PQFP device that interfaces directly with offshell clock generation/recovery chips. Eight ports can be configured as 100 BASE-TX or FX ports individually. Three additional ports have Media Independent Interfaces (MII) which allow easy connection of management and bridge devices. The expansion port allows multiple XRCs to be linked together to form a repeater of high port counts. LEDs are provided for visual monitoring of TX/FX port activities and collisions.

The XRC's design inserts minimum delay between the TX/FX ports and the expansion port. A master-slave type arbitration is also implemented to shorten the communciation time among multiple XRCs. As a result, design for Class II stackable hub is greatly simplified.

Control Functions and management status are implemented through internal registers. These registers are accessed via either standard MII management interface (MDC, MDIO) or several serial ports. These serial ports are accessed easily by hardware for debugging and configuration purposes. A dedicated management chip can also utilize these serial ports to access the XRC.

3.0 PIN CONFIGURATION



4.0 PIN DESCRIPTION

Table 4-1 Pin Description for MX98741

	A. MX Data Transceiver (Am78965/Am78966 or MC68836), 98 pins		
PAD #	Name	I/O	Description
59-63 96-100 111-115 167-171 183-187 197-201 9-13 23-27	TDAT[0:7][0:4]	O, EXP	Transmit Data. These five outputs are 4B/5B encoded transmit data symbols, driven at the rising edge of TXCLK. TDAT4 is the Most Significant Bit.
135	TXCLK	I, TTL	Transmit Clock. This pin supplies the frequency reference to the transmit logic. It should be driven by an external 25 MHz crystal-controlled clock source.
54-58 90-94 106-110 160-164 177-181 190-194 4-8 17-21	RDAT[0:7][0:4]	I, TTL	Receive Data. These 5-bit parallel data symbols from transceiver are latched by the rising edge of RSCLK. RDAT4 is the Most Significant Bit.
50,87 102,158 174,188 2,15	RSCLK[0:7]	I, TTL	Recovered Sumbol Clock. This is a 25 MHz clock, which is derived from the clock synchroniztion PLL circuit.
51,88 103,159 175,189 3,16	SIGDET[0:7]	I, TTL	Signal Detect. This signal indicates that the received signal is above the detection threshold and will be used for the link test state machine.
134	COCLK	I, TTL	Core Clock. 50M Clock input used by Repeater Core.

B. Expansion Port, 18 pins			
PAD #	Name	I/O	Description
72	JAMO	O, TTL	Forced Jam Out. Active High. The OR'd forced jam signals exclude JAMI input) controlled by Carrier Integrity Monitor of each port. If collision occurs inside the XRC, this pin is also asserted.
73	JAMI	I, Schm	Forced Jam Input. Active High. Asserted by external arbiter, and XRC will generate JAM patterns to all its ports. Note : Glitch on JAMI and EDATENL may cause internal state machine malfunction.
75	EDATENL	I, Schm	Enable Expansion Data. Active Low. Asserted by an external arbitor. XRC will drive data into EDAT.
66-70	EDAT[0:4]	I/O, EXP	Expansion Data. Bidirectional 5-bit wide data. By default, EDAT is an input. When EDATENL is low, EDAT changed from input mode to output mode. Internally pull-up.
84-86	ACTP[5:8]	O, TTL	Activity Out. This is the activity of port 5..8 synchronous to COCLK (50M clock used by core). It also serves as data framing signal for the packet on EDAT. ACTP leads EDAT's /J/K/ pattern by more than 80 ns and deasserted 40ns after the /T/R/ or the last byte of jam patterns.
78-81, 83	ACTP[0:4] /XRCADD[0:4]	I/O, TTL	Activity Out/Physical Address. When RESETL goes high, value on ACTP[0;4] will be latched into internal buffer as physical address of XRC. After reset, these five pins have the same function as ACTP[5:8].
76	ANYACT	O, TTL	Any Activity. Active High. The OR'd ACTP[7:0] and TXEN A to C. This is used as an indication that an XRC is ready to drive data into EDAT.
74	EXTCRS	I, Schm	External Carrier Sense. Active high. Asserted by an external arbitor indicating activity from other XRC's at the expansion port.
		C. Miscellaneous Pins, 2 pins	
204	RESETL	I, Schm	Reset. Active Low. This signal is output by the system to reset all the logic on the chip.
203	SCRCTRL	I, TTL	Scrambler Control. If high, the scrambler/descrambler of each port is individually controlled by MII register 17. If low, the scrambler/descrambler is bypassed in all the ports.

D. Register Access Pins, 8 pins

PAD #	Name	I/O	Description
47	PARTLNK	O, TTL	Partition/Link Status. This pin shows the status of internal register #18 in round-robin fashion starting at port 0 partition status and ending at port7 Link Status after REGLTCH is deasserted.
46	JBFLO	O, TTL	Jabber/Buffer Status. This pin shows the status of internal register #19 in round-robin fashion starting at port 0 Jabber Status and ending at port 7 Elastic Buffer Over/Underflow Status after REGLTCH is deasserted.
45	PTSCEN	I/O, TTL	Port/Scrambler Enable. If RDXWR is high, each port's enable/disable status (register #17) will be displayed at the rising edge of REGCK in round-robin fashion starting at port 0 Port 0 Enable status and ending at port 7 Scrambler Enable status after REGLTCH is deasserted. If RDXWR is low, 16-bit data can be written into the XRC at the rising edge of REGCK in round-robin fashion starting at port 0 Port Enable Signal and ending at port 7 Scrambler enable after REGLTCH is asserted high. Internally pull-up.
44	PIDIS	I/O, TTL	Partition/Isolation Disable. If RDXWR is high, each port's partition/ Isolation Disable status will be displayed at the rising edge of REGCK in round-robin fashion starting at port 0 partition disable status and ending at port7 Isolation Disable status after REGLTCH is deasserted. If RDXWR is low, 16-bit data can be written into the XRC at the rising edge of REGCK in round-robin fashion starting at port 0 partition disable status and ending at port 7 Isolation disable status after REGLTCH is asserted high. Internally pull-down.
48	ISO	O, TTL	Isolation. Active High. Each port's isolation status will be displayed at the rising edge of REGCK in round-robin fashion starting at port0 after REGLTCH is deasserted.
43	RDXWR	I, TTL	Read/Write. High indicates "Read" mode; register is being read out. REGLTCH is output. Low indicates "Write" mode; control registers are being written and REGLTCH is input. When RDXWR is programmed to "Write" Mode, internal "Read" status machine will be reset immediately.
41	REGLTCH	I/O, TTL	Register Latch. An output if RDXWR is high; an input if RDXWR is low. At the rising edge of REGCK, PARTLNK, JBFLO, PTSCEN, PIDIS, ISO display bit 0 status of corresponding registers, at the rising edge of next REGCK, bit 1 status is displayed, etc. After bit 15 is displayed, REGLTCH is asserted at the rising edge of next REGCK. Note : Both Data and REGLTCH are driven at the falling edge of REGCK inside the XRC. To make sure the data setup time, it is strongly recommended that the frequency of REGCK is below 12.5 MHz. Internally pull-down.
40	REGCK	I, TTL	Register Clock. A clock used as reference to display various status of each port or to latch control information inside XRC. The recommended clock's frequency is below 12.5MHz.

		E. LED Pins, 9 pins	
PAD #	Name	I/O	Description
30-37	XACTLED[0:7]	O, TTL	Activity LED. Active Low. This pin provides a minimum 80ms ON time (low) and 20ms OFF time (high) for activities on each port. External buffers are necessary to drive LEDs.
205	XCOLED	O, MII	Collision LED. This pin is capable of driving LED directly to display Activity status. The ON (active low) time and OFF (active high) time of LED's is 80ms and 20ms respectively.
			F. Media Independent Interface (MII), 33 pins
116	TXENA	I, TTL	Transmit Enable MII A. Synchronous to the TXCLK's rising edge. It is asserted by the MAC with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented.
117-120	TXDA[0:3]	I, TTL	Transmit Data MII A. Synchronous to the TXCLK's rising edge. For each TXCLK period in which TXENA is asserted, TXDA[3:0] are also driven by the MAC. While TXENA is de-asserted, the value of TXDA[3:0] is ignored. TXDA3 is the Most Significant Bit.
121	TXERA	I, TTL	Transmit Error MII A. Synchronous to the TXCLK's rising edge. When TXERA is asserted for one or more TXCLK period while TXENA is also asserted, one or more "HALT" symbols will present at TDAT4_0.
122	RXDVA	O, TTL	Receive Data Valid MII A. Synchronous to RXCLK's rising edge. This signal remains asserted through the whole frame, starting with the start-of-frame delimiter and excluding any end-of-frame delimiter. High impedance after reset.
123	CRSA	O, TTL	Carrier Sense MII A. In TX mode, synchronous to RXCLK. This pin is asserted when (1) the receiving medium is not idle, or (2) the transmitting medium is not idle in the half-duplex mode. High impedance after reset.
153	MDIO	I/O, TTL	Management Data Input/Output. A bi-directional signal. After reset, this pin is in high-impedance state. The selection of input/output direction is based on IEEE 802.3u management functions (Section 22.2.4). Low after reset due to internally pull-down. When RDXWR is low (i.e. Write operation, MDIO will be forced to low to disable the function of MDC and MDIO. i.e. Programming internal registers through register access pins owns higher priority.

F. Media Independent Interface (MII, Continued)			
PAD #	Name	I/O	Description
125	TXENB	I, TTL	Transmit Enable MII B. Synchronous to the TXCLK's rising edge. It is asserted by the MAC with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented.
126-129	TXDB[0:3]	I, TTL	Transmit Data MII B. Synchronous to the TXCLK's rising edge. For each TXCLK period in which TXENB is asserted, TXDB[3:0] are also driven by the MAC. While TXENB is de-asserted, the value of TXDB[3:0] is ignored. TXDB3 is the Most Significant Bit.
130	TXERB	I, TTL	Transmit Error MII B. Synchronousto the TXCLK's rising edge. When TXERB is asserted for one or more TXCLK period while TXENB is also asserted, one or more "HALT" symbols will present at TDAT4_0.
131	RXDVB	O, TTL	Receive Data Valid MII B. Synchronous to RXCLK's rising edge. This signal remains asserted through the whole frame, starting with the start-of-frame delimiter and excluding any end-of-frame deliminter. High impedance after reset.
132	CRSB	O, TTL	Carrier Sense MII B. In TX mode, synchronous to RXCLK. This pin is asserted when (1) the receiving medium is not idle, or (2) the transmitting medium is not idle in the half-duplex mode. High impedance after reset.
145	TXENC	I, TTL	Transmit Enable MII C. Synchronous to the TXCLK's rising edge. It is asserted by the MAC with the first nibble of the preamble and remains asserted while all nibbles to be transmitted are presented.
146-149	TXDC[0:3]	I, TTL	Transmit Data MII C. Synchronous to the TXCLK's rising edge. For each TXCLK period in which TXENC is asserted, TXDC[3:0] are also driven by the MAC. While TXENC is de-asserted, the value of TXDC[3:0] is ignored. TXDC3 is the Most Significant Bit.
150	TXERC	I, TTL	Transmit Error MII C. Synchronousto the TXCLK's rising edge. When TXERC is asserted for one or more TXCLK period while TXENC is also asserted, one or more "HALT" symbols will present at TDAT4_0
151	RXDVC	O, TTL	Receive Data Valid MII C. Synchronous to RXCLK's rising edge. This signal remains asserted through the whole frame, starting with the start-of-frame delimiter and excluding any end-of-frame deliminter. High impedance after reset.
152	EDATACT	O, TTL	Expansion DATa Activity. When XRC is outputing data onto expansion EDAT, this pin will be asserted high. User can use this pin to control external EDAT bus switch in case multiple HUBs application is necessary.

PAD #	Name	I/O	Description
141	RXER	O, EXP	Receive Error. Synchronous to RXCLK's rising edge. While RXDV is asserted, i.e. a frame is being received, this signal is asserted if any coding error is detected. High-impedence after reset.
143	RXCLK	O, MII	Receive Clock MII. 25 MHz continuous clock that provides the timing reference for the transfer of the RXDV, RXD and RXER signals. High-impedance after reset.
137-140	RXD[0:3]	O, MII	Receive Data MII. Synchronous to RXCLK's rising edge. For each RXCLK period in which RXDV is asserted, RXD[3:0] should be latched by the MAC. While RXDV is deasserted, RXD[3:0] are the nibbles 5B/4B decoded from RDAT[4:0]. RXD3 is the Most Significant Bit. High-impedance after reset.
142	COL	O, EXP	Collision MII. This signal is asserted if both the receiving media and TXEN are active. High-impedance after reset.
154	MDC	I, TTL	Management Data Clock. The timing reference for MDIO. The minumum high and low times are 200 ns each. No limitation on the maximum high and low time.
G. Power/Ground/Test/Loopback, 39 pins			
206	TEST	I, TTL	Test. Industrial test pin. Set to 0 or left unconnected for normal operation. When programmed to logic 1, XRC is in test mode. Internal Pulldown.
207	TSEL	I, TTL	Test Mode Select. When TEST is high and TSEL is low, XRC is in "Real Time Counter" Mode; when TEST is high and TSEL is high, XRC is in "Test Mode Counter" mode. Internally pull down.
1,14,22, 38,42,49 52,53,71, 77,101 104,105, 124,136, 155,156, 165,166, 173,182, 202,208	GND		Ground.
28,29, 39,64, 65,82, 89,95, 133,144, 157,176, 195,196	VCC		5V Power Supply.

5.0 FUNCTIONAL & OPERATION DESCRIPTION

5.1 MINIMUM AND MAXIMUM MODE APPLICATION

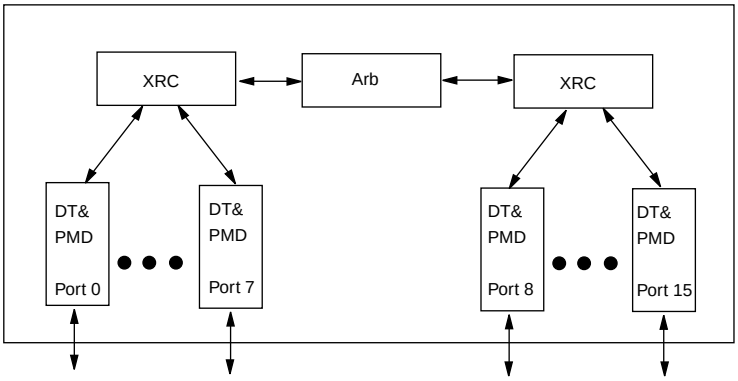


Figure 5-1 Minimum Mode Operation for XRC

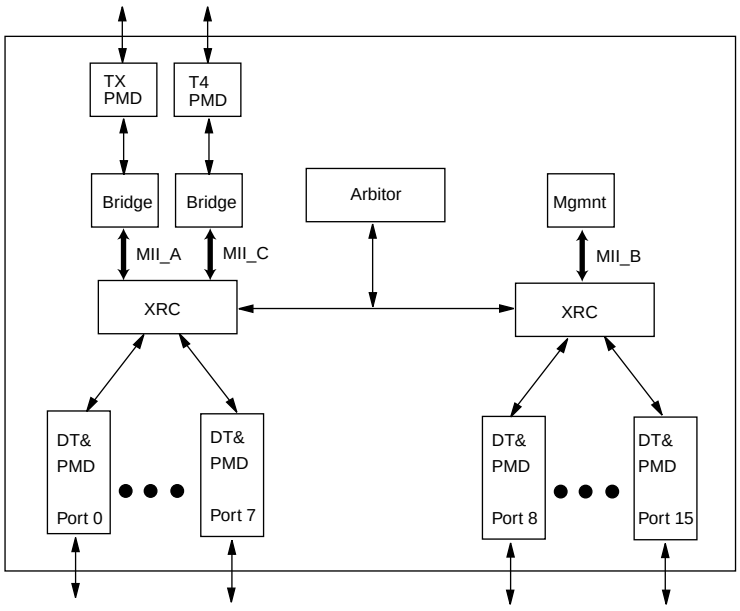


Figure 5-2 Maximum Mode Operation for XRC

5.2 INTERNAL REGISTERS

There are two ways to access the XRC internal registers.

All the registers can be accessed through MII's MDC and MDIO. Although XRC connects to multiple 100-TX PHY's, they are all identical. Each XRC has only one PHY address as defined by ACTP[4:0] pins. If multiple XRC's are on the same MDIO bus, each of them should have different PHY address. Other non-XRC PHY devices (e.g. T4) are also allowed to be managed with the same management interface as long as PHY address of each device is distinct.

Another way to access registers is through register access pins. Register 17 (Scrambler Enable and Port Enable), Register 18 (Link Status, Partition Status), Register 19 (Elastic Buffer Status and Jabber Status), Register 20 (Isolation Status), Register 21 (Isolation Disable and Partition Disable) can also be read through PTSCEN, PARTLNK, JBFLO, ISO and PIDIS, respectively. The exception are register 0 (Command Register), register 1 (Status Register), and register 16 (Port Reset Register) which can only be accessed through MDC and MDIO. The register access pins facilitate a simple read/write protocol suitable for hardware-only configuration and status display design.

A. Command Register (register #0) (R/W)

Table 5-1 Control Register Bit Definition

Bit(s)	Name	Description	R/W
0.15	Reset	1 : PHY reset. A 240ns reset pulse will be generated to reset XRC internal logic.	R/W
		0 : normal operation	SC
0.14	Loop Back	1 : enable loopback mode. 0 : disable loopback mode. The default setting is 0.	R/W
0.13	Speed Selection	Forced to 1 and indicate 100 Mb/s.	
		Write 0 to this bit has no effect.	R
0.12	Auto-Negotiation Enable	Forced to 0 and indicate that Auto-Negotiation process is disabled.	
		Write 1 to this bit has no effect.	R
0.11	Power-Down	1 : power-down. COCLK and TXCLK for each port will be disabled. Clock for Management Block will keep running. During power-down, all state machines will be reset to its default state.	
		0 : normal operation.	R/W
0.10	Isolate	1 : electrically Isolate PHY from MII	
		0 : normal operation	R/W
0.9	Restart Auto-Negotiation	Forced to 0 and indicate that Auto-Negotiation process is disable.	
		Write 1 to this bit has no effect.	R
0.8	Duplex Mode	Forced to 0 and indicate that only Half Duplex is available.	
		Write 1 to this bit has no effect.	R
0.7	Collision Test	1 : enable COL signal test. The PHY will assert the COL signal within 5120 ns in response to the assertion of TXEN. While this bit is set to one, the PHY will deassert the COL signal within 40 ns in response to the deassertion of TXEN.	
		0 : normal operation.	
		Set to 0 after power on reset.	R/W
0.6:0	Reserved	Value 0 will be read when one tries to read these bits.	R

B. Status Register (register #1) (R)

Table 5-2 Status Register Bit Definition

Bit(s)	Name	Description	R/W
1.15	100BASE-T4	Forced to 0 and indicates that XRC is not able to perform 100BASE-T4.	R
1.14	100BASE-X Full Duplex	Forced to 0 and indicates that XRC is not able to perform 100BASE-X Full Duplex.	R
1.13	100BASE-X Half Duplex	Forced to 1 and indicates that XRC is able to perform 100BASE-X Half Duplex.	R
1.12	10 Mb/s Full Duplex	Forced to 0 and indicates that XRC is not able to perform 10 Mb/s Full Duplex.	R
1.11	10 Mb/s Half Duplex	Forced to 0 and indicates that XRC is not able to perform 10 Mb/s Half Duplex.	R
1.10:6	Reserved	Value 0 will be released by XRC when read.	R
1.5	Auto-Negotiation Complete	Forced to 0.	R
1.4	Remote Fault	Forced to 0.	R
1.3	Auto-Negotiation Ability	Forced to 0.	R
1.2	Link Status	1 : All ports are link up. 0 : Any port is link fail. Will be set to 1 after this port is read.	R
1.1	Jabber Detect	1 : Jabber condition in any port is detected. 0 : No Jabber condition detected for all ports	R
1.0	Extended Capability	Forced to 1.	R

C. Port Reset Register (register #16) (R/W)

Table 5-3 Port Reset Register Bit Definition

Bit(s)	Name	Description	R/W
16.15:8	Reserved	Ignored when read.	R
16.7	ResetP7	1 : reset Port 7's Logic.	
		0 : not reset Port 7's Logic.	
		Power on low.	R/W
16.6	ResetP6	1 : reset Port 6's Logic.	
		0 : not reset Port 6's Logic.	
		Power on low.	R/W
16.5	ResetP5	1 : reset Port 5's Logic.	
		0 : not reset Port 5's Logic.	
		Power on low.	R/W
16.4	ResetP4	1 : reset Port 4's Logic.	
		0 : not reset Port 4's Logic.	
		Power on low.	R/W
16.3	ResetP3	1 : reset Port 3's Logic.	
		0 : not reset Port 3's Logic.	
		Power on low.	R/W
16.2	ResetP2	1 : reset Port 2's Logic.	
		0 : not reset Port 2's Logic.	
		Power on low.	R/W
16.1	ResetP1	1 : reset Port 1's Logic.	
		0 : not reset Port 1's Logic.	
		Power on low.	R/W
16.0	ResetP0	1 : reset Port 0's Logic.	
		0 : not reset Port 0's Logic.	
		Power on low.	R/W

D. Port Control Register (register #17) (R/W)

Table 5-4 Port Control Register Bit Definition

Bit(s)	Name	Description	R/W
17.15	ScrenP7	1 : Enable Scrambler/Descrambler at Port 7	
		0 : Disable Scrambler/Descrambler at Port 7	
		The default value after power on is 1.	R/W
17.14	ScrenP6	1 : Enable Scrambler/Descrambler at Port 6	
		0 : Disable Scrambler/Descrambler at Port 6	
		The default value after power on is 1.	R/W
17.13	ScrenP5	1 : Enable Scrambler/Descrambler at Port 5	
		0 : Disable Scrambler/Descrambler at Port 5	
		The default value after power on is 1.	R/W
17.12	ScrenP4	1 : Enable Scrambler/Descrambler at Port 4	
		0 : Disable Scrambler/Descrambler at Port 4	
		The default value after power on is 1.	R/W
17.11	ScrenP3	1 : Enable Scrambler/Descrambler at Port 3	
		0 : Disable Scrambler/Descrambler at Port 3	
		The default value after power on is 1.	R/W
17.10	ScrenP2	1 : Enable Scrambler/Descrambler at Port 2	
		0 : Disable Scrambler/Descrambler at Port 2	
		The default value after power on is 1.	R/W
17.9	ScrenP1	1 : Enable Scrambler/Descrambler at Port 1	
		0 : Disable Scrambler/Descrambler at Port 1	
		The default value after power on is 1.	R/W
17.8	ScrenP0	1 : Enable Scrambler/Descrambler at Port 0	
		0 : Disable Scrambler/Descrambler at Port 0	
		The default value after power on is 1.	R/W
17.7	EnP7	1 : Enable RX/TX functions at Port 7.	
		0 : Disable RX/TX functions at Port 7.	
		The default value after power on is 1.	R/W
17.6	EnP6	1 : Enable RX/TX functions at Port 6.	
		0 : Disable RX/TX functions at Port 6.	
		The default value after power on is 1.	R/W
17.5	EnP5	1 : Enable RX/TX functions at Port 5.	
		0 : Disable RX/TX functions at Port 5.	
		The default value after power on is 1.	R/W

Table 5-4 Port Control Register Bit Definition (Continued)

Bit(s)	Name	Description	R/W
17.4	EnP4	1 : Enable RX/TX functions at Port 4.	
		0 : Disable RX/TX functions at Port 4.	
		The default value after power on is 1.	R/W
17.3	EnP3	1 : Enable RX/TX functions at Port 3.	
		0 : Disable RX/TX functions at Port 3.	
		The default value after power on is 1.	R/W
17.2	EnP2	1 : Enable RX/TX functions at Port 2.	
		0 : Disable RX/TX functions at Port 2.	
		The default value after power on is 1.	R/W
17.1	EnP1	1 : Enable RX/TX functions at Port 1.	
		0 : Disable RX/TX functions at Port 1.	
		The default value after power on is 1.	R/W
17.0	EnP0	1 : Enable RX/TX functions at Port 0.	
		0 : Disable RX/TX functions at Port 0.	
		The default value after power on is 1.	R/W

E. Link and Partition Status Register (register #18) (R)

Table 5-5 Link and Partition Status Register Bit Definition

Bit(s)	Name	Description	R/W
18.15	LinkP7	1 : Link Status is OK at port 7	
		0 : Link Status is Fail at Port 7	
		Status is updated at every TXCLK clock.	R
18.14	LinkP6	1 : Link Status is OK at port 6	
		0 : Link Status is Fail at Port 6	
		Status is updated at every TXCLK clock.	R
18.13	LinkP5	1 : Link Status is OK at port 5	
		0 : Link Status is Fail at Port 5	
		Status is updated at every TXCLK clock.	R
18.12	LinkP4	1 : Link Status is OK at port 4	
		0 : Link Status is Fail at Port 4	
		Status is updated at every TXCLK clock.	R
18.11	LinkP3	1 : Link Status is OK at port 3	
		0 : Link Status is Fail at Port 3	
		Status is updated at every TXCLK clock.	R
18.10	LinkP2	1 : Link Status is OK at port 2	
		0 : Link Status is Fail at Port 2	
		Status is updated at every TXCLK clock.	R
18.9	LinkP1	1 : Link Status is OK at port 1	
		0 : Link Status is Fail at Port 1	
		Status is updated at every TXCLK clock.	R
18.8	LinkP0	1 : Link Status is OK at port 0	
		0 : Link Status is Fail at Port 0	
		Status is updated at every TXCLK clock.	R
18.7	PartP7	1 : Port 7 has been partitioned	
		0 : Port 7 has not been partitioned	
		Status is updated every 40 ns.	R
18.6	PartP6	1 : Port 6 has been partitioned	
		0 : Port 6 has not been partitioned	
		Status is updated every 40 ns.	R
18.5	PartP5	1 : Port 5 has been partitioned	
		0 : Port 5 has not been partitioned	
		Status is updated every 40 ns.	R

Table 5-5 Link and Partition Status Register Bit Definition (Continued)

Bit(s)	Name	Description	R/W
18.4	PartP4	1 : Port 4 has been partitioned	
		0 : Port 4 has not been partitioned	
		Status is updated every 40 ns.	R
18.3	PartP3	1 : Port 3 has been partitioned	
		0 : Port 3 has not been partitioned	
		Status is updated every 40 ns.	R
18.2	PartP2	1 : Port 2 has been partitioned	
		0 : Port 2 has not been partitioned	
		Status is updated every 40 ns.	R
18.1	PartP1	1 : Port 1 has been partitioned	
		0 : Port 1 has not been partitioned	
		Status is updated every 40 ns.	R
18.0	PartP0	1 : Port 0 has been partitioned	
		0 : Port 0 has not been partitioned	
		Status is updated every 40 ns.	R

F. Elastic Buffer Over/Underflow and Jabber Status Register (register #19) (R)

Table 5-6 Elastic Buffer Over/Underflow and Jabber Register Bit Definition

Bit(s)	Name	Description	R/W
19.15	EBOUF7	1 : Elastic Buffer Over/Underflow at Port 7	
		0 : Normal Condition.	
		Clear to 0 by RESETL (or RESETP7).	R
19.14	EBOUF6	1 : Elastic Buffer Over/Underflow at Port 6	
		0 : Normal Condition.	
		Clear to 0 by RESET (or RESETP6).	R
19.13	EBOUF5	1 : Elastic Buffer Over/Underflow at Port 5	
		0 : Normal Condition.	
		Clear to 0 by RESET (or RESETP5).	R
19.12	EBOUF4	1 : Elastic Buffer Over/Underflow at Port 4	
		0 : Normal Condition.	
		Clear to 0 by RESET (or RESETP4).	R
19.11	EBOUF3	1 : Elastic Buffer Over/Underflow at Port 3	
		0 : Normal Condition.	
		Clear to 0 by RESET (or RESETP3).	R
19.10	EBOUF2	1 : Elastic Buffer Over/Underflow at Port 2	
		0 : Normal Condition.	
		Clear to 0 by RESET (or RESETP2).	R
19.9	EBOUF1	1 : Elastic Buffer Over/Underflow at Port 1	
		0 : Normal Condition.	
		Clear to 0 by RESET (or RESETP1).	R
19.8	EBOUF0	1 : Elastic Buffer Over/Underflow at Port 0	
		0 : Normal Condition.	
		Clear to 0 by RESET (or RESETP0).	R
19.7	JABP7	1 : Receive Jabber Active at Port 7	
		0 : No Jabber condition at Port 7	R
19.6	JABP6	1 : Receive Jabber Active at Port 6	
		0 : No Jabber condition at Port 6	R
19.5	JABP5	1 : Receive Jabber Active at Port 5	
		0 : No Jabber condition at Port 5	R
19.4	JABP4	1 : Receive Jabber Active at Port 4	
		0 : No Jabber condition at Port 4	R
19.3	JABP3	1 : Receive Jabber Active at Port 3	
		0 : No Jabber condition at Port 3	R

Table 5-6 Elastic Buffer Over/Underflow and Jabber Register Bit Definition (Continued)

Bit(s)	Name	Description	R/W
19.2	JABP2	1 : Receive Jabber Active at Port 2	
		0 : No Jabber condition at Port 2	R
19.1	JABP1	1 : Receive Jabber Active at Port 1	
		0 : No Jabber condition at Port 1	R
19.0	JABP0	1 : Receive Jabber Active at Port 0	
		0 : No Jabber condition at Port 0	R

G. Isolation Status Register (register #20) (R)

Table 5-7 Isolation Status Register Bit Definition

Bit(s)	Name	Description	R/W
20.15	ISO7	1 : Port Isolation is occuring at port 7, 0 : Port Isolation is not occuring at port 7. Set to 1 by CIM state machine, cleared to 0 by asserting RESETL pin or writing to Port Reset Register or by CIM state machine.	R
20.14	ISO6	1 : Port Isolation is occuring at port 6, 0 : Port Isolation is not occuring at port 6.	R
20.13	ISO5	1 : Port Isolation is occuring at port 5, 0 : Port Isolation is not occuring at port 5.	R
20.12	ISO4	1 : Port Isolation is occuring at port 4, 0 : Port Isolation is not occuring at port 4.	R
20.11	ISO3	1 : Port Isolation is occuring at port 3, 0 : Port Isolation is not occuring at port 3.	R
20.10	ISO2	1 : Port Isolation is occuring at port 2, 0 : Port Isolation is not occuring at port 2.	R
20.9	ISO1	1 : Port Isolation is occuring at port 1, 0 : Port Isolation is not occuring at port 1.	R
20.8	ISO0	1 : Port Isolation is occuring at port 0, 0 : Port Isolation is not occuring at port 0.	R
20.7:0	Reserved	Ignored while read.	R

H. Isolation/Partition Disable Register (register #21) (R/W)

Table 5-8 Isolation/Partition Disable Register Bit Definition

Bit(s)	Name	Description	R/W
21.15	ISODIS7	1 : Port 7 Isolation function is disabled 0 : Port 7 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.14	ISODIS6	1 : Port 6 Isolation function is disabled 0 : Port 6 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.13	ISODIS5	1 : Port 5 Isolation function is disabled 0 : Port 5 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.12	ISODIS4	1 : Port 4 Isolation function is disabled 0 : Port 4 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.11	ISODIS3	1 : Port 3 Isolation function is disabled 0 : Port 3 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.10	ISODIS2	1 : Port 2 Isolation function is disabled 0 : Port 2 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.9	ISODIS1	1 : Port 1 Isolation function is disabled 0 : Port 1 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.8	ISODIS0	1 : Port 0 Isolation function is disabled 0 : Port 0 Isolation function is not disabled. The default value is 0 after reset.	R/W
21.7	PARDIS7	1 : Port 7 Parition function is disbled. 0 : Port 7 Partition function is not disabled. The default value is 0 after reset.	R/W
21.6	PARDIS6	1 : Port 6 Parition function is disbled. 0 : Port 6 Partition function is not disabled. The default value is 0 after reset.	R/W
21.5	PARDIS5	1 : Port 5 Parition function is disbled. 0 : Port 5 Partition function is not disabled. The default value is 0 after reset.	R/W
21.4	PARDIS4	1 : Port 4 Parition function is disbled. 0 : Port 4 Partition function is not disabled. The default value is 0 after reset.	R/W

Table 5-8 Isolation/Partition Disable Register Bit Definition (Continued)

Bit(s)	Name	Description	R/W
21.3	PARDIS3	1 : Port 3 Parition function is disbled.	
		0 : Port 3 Partition function is not disabled.	
		The default value is 0 after reset.	R/W
21.2	PARDIS2	1 : Port 2 Parition function is disbled.	
		0 : Port 2 Partition function is not disabled.	
		The default value is 0 after reset.	R/W
21.1	PARDIS1	1 : Port 1 Parition function is disbled.	
		0 : Port 1 Partition function is not disabled.	
		The default value is 0 after reset.	R/W
21.0	PARDIS0	1 : Port 0 Parition function is disbled.	
		0 : Port 0 Partition function is not disabled.	
		The default value is 0 after reset.	R/W

Note : Physical address input from ACTP[4:0] during RESETL is asserted will be stored at bit 4:0 of register #31.

6.0 ABSOLUTE MAXIMUM RATINGS

Table 6-1 Absolute Maximum Rating for MX98741

RATING	VALUE
Supply Voltage (VCC)	4.75V to 5.25V
DC Input Voltage (Vin)	-0.5V to VCC+0.5V
DC Output Voltage (Vout)	-0.5V to VCC+0.5V
Storage Temperature Range (TSTG)	-55 C to 150 C
Power Dissipation (PD)	750 mW
ESD rating (Rzap = 1.5K, Czap = 100pF)	2000V

Notice :

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cauase permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Preliminary, Subject to change.

7.0 DC CHARACTERISTICS

Table 7-1 DC Characteristics for MX98741

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
		A. Supply Current			
ICC	Average Active (TXing	COCLK = 50MHz			
	/RXing) Supply Current	VIN = Switching	-	50	mA
ICCIDLE	Average Idle Supply Current	COCLK = 50MHz			
		VIN=VCC/GND	-	TBD (Note)	mA
IDD	Static IDD Current	COCLK=Undriven	-	TBD (Note)	uA

Note : These two parameters will be measured while DC/AC characterization is proceeding.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
		B. TTL Inputs, Outputs, Tri-States			
Vil	Maximum Low Level Input Voltage	GND = 0V	-	0.8	V
Vih	Minimum High Level Input Voltage		2.0	VCC+0.5	V
Iin	Input Current	VI=VCC/GND	-1.0	1.0	uA
Voh	Minimum High Level Output Voltage	Ioh = -2mA	2.4	-	V
Vol	Maximum Low Level Output Voltage	Iol = 2mA	-	0.4	V
Ioz	Maximum TRI-STATE				
	Output Leakage Current	VOUT=VCC/GND	-10.0	10.0	uA
		C. EXP Outputs, Tri-States			
Voh	Minimum High Level Output Voltage	Ioh = -4mA	2.4	-	V
Vol	Maximum Low Level Output Voltage	Iol = 4mA	-	0.4	V
Vil	Maximum Low Level Input Voltage		-	0.8	V
Vih	Minimum High Level Input Voltage		2.0	-	V
Ioz	Maximum TRI-STATE				
	Output Leakage Current	VOUT=VCC/GND	-10.0	10.0	uA
		D. MII Inputs, Outputs, Tri-States			
Voh	Minimum High Level Output Voltage	Ioh = -8mA	2.4	-	V
Vol	Maximum Low Level Output Voltage	Iol = 8mA	-	0.4	V
Vil	Maximum Low Level Input Voltage		-	0.8	V
Vih	Minimum High Level Input Voltage		2.0	-	V
Ioz	Maximum TRI-STATE				
	Output Leakage Current	VOUT=VCC/GND	-10.0	10.0	uA

Table 7-1 DC Characteristics for MX98741 (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
		E. TTL Input With Schmitt Trigger			
Vil	Maximum Low Level Input Voltage		-	0.6	V
Vih	Minimum High Level Input Voltage		2.7	-	V

Note :
1.All parameters listed in category A/B/C/D are preliminary, subject to change. After wafer is out, the value measured on tester will be the finalized Voltage Characteristics.
2.For MII port, see item F in next page for one's reference.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
		F. Input Current Limits for MII			
Iih	Input High Current with Vi = 5.25 Volt	All Except COL,			
		MDC, MDIO(Note 1)	-	200	uA
		COL (Note 2)	-	20	uA
		MDC (Note 3)	-	20	uA
		MDIO (Note 4)	-	3000	uA
		MDIO (Note 5)	-	20	uA
Iil	Input Low Current with Vi = 0.00 Volt	All Except COL,			
		MDC, MDIO(Note 1)	-20	-	uA
		COL (Note 2)	-200	-	uA
		MDC (Note 3)	-20	-	uA
		MDIO (Note 4)	-180	-	uA
		MDIO (Note 5)	-3800	-	uA
Iiq	Input Quiescent Current				
	with Vi = 2.4 Volt	MDIO (Note 4)	-	1450	uA
		MDIO (Note 5)	-1450	-	uA

Note1 :
Measured at input of Reconcilation sublayer for CRSs, RXD[3:0], RXCLK, RXDVs, RXER, and TXCLK. Measured at inputs of XRC for TXD[3:0], TXEN, and TXER.

Note 2 :
Measured at input of Reconciliation sublayer.

Note 3 :
Measured at input of XRC.

Note 4 :
Measured at input of STA.

Note 5 :
Measured at input of XRC which cn be attached via the mechanical interface specified in sec tion 22.6 in [1].

Caution : Input Current limit is only for board designer's reference. In MX98741, we will not use this specification to verify the input signals provided by stimulus patterns.

8.0 AC CHARACTERISTICS AND WAVEFORMS

A. Media Independent Interface

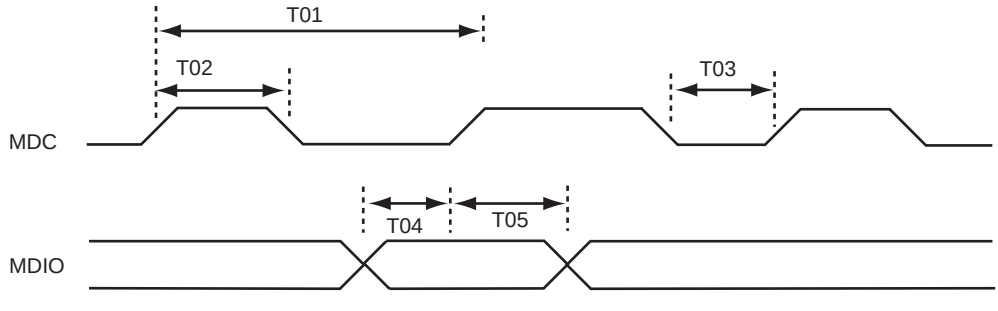


Figure 8-1 MDIO Timing Relationship to MDC

Symbol	Description	MIN.	MAX.	UNIT
T01	Period for MDC	400	-	ns
T02	High Time for MDC	160	-	ns
T03	Low Time for MDC	160	-	ns
T04	MDIO Setup to MDC rising edge (Write Command)	10	-	ns
T05a	MDIO Hold to MDC rising edge (Write Command)	10	-	ns
T05b	MDIO Hold to MDC rising edge (Read Command)	5	10	ns

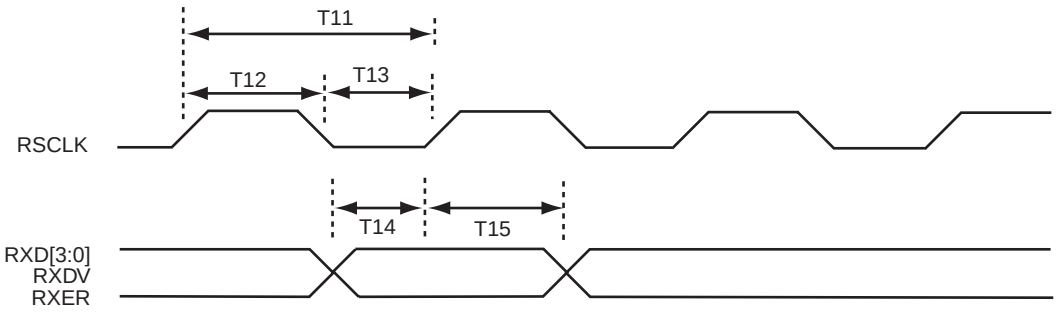


Figure 8-2 Receive Signal Timing Relationships at the MII

Symbol	Description	MIN.	MAX.	UNIT
T11	RXCLK Period (Note 1)	40	40	ns
T12	RXCLK High Time	19	-	ns
T13	RXCLK Low Time	17	-	ns
T14	RXD[3:0]/RXDVs/RXER Setup Time to RXCLK rising edge (Note 2)	10	-	ns
T15	RXD[3:0]/RXDVs/RXER Hold Time to RXCLK rising edge (Note 2)	15	-	ns

Note 1 :

The accurate RXCLK frequency shall be 25MHz +/- 100 ppm.

Note 2 :

The setup time of an MII signal relative to an MII clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region. The hold time of an MII signal relative to an MII clock edge is defined as the length of time between when the clock exits the switching region and when the signal enters the switching region.

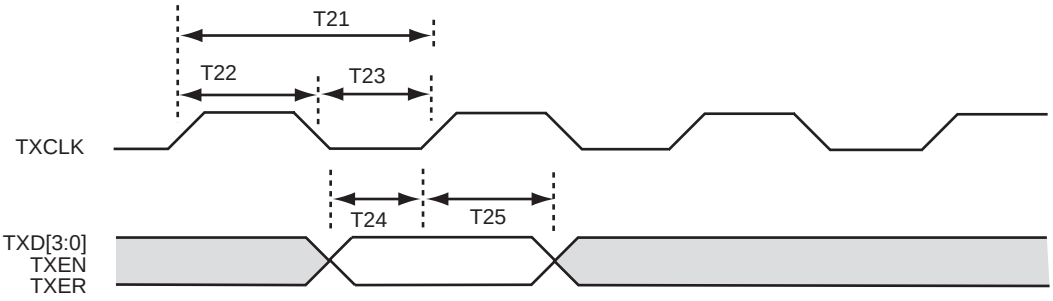


Figure 8-3 Trannsmit Signal Timing Relationships at the MII

Symbol	Description	MIN.	MAX.	UNIT
T21	TXCLK Period (Note 1)	40	40	ns
T22	TXCLK High Time	0.35*T21	0.65*T21	ns
T23	TXCLK Low Time	0.35*T21	0.65*T21	ns
T24	TXD[3:0]/TXENs/TXERs Setup Time to TXCLK rising edge (Note 2)	10	-	ns
T25	TXD[3:0]/TXENs/TXERs Hold Time to TXCLK rising edge (Note 2)	10	-	ns

Note 1 :

The accurate TXCLK frequency shall be 25 MHz +/- 100 ppm.

Note 2 :

The setup time of an MII signal relative to an MII clock edge is defined as the length of time between when the signal exits and remains out of the switching region and when the clock enters the switching region. The hold time of an MII signal relative to an MII clock edge is defined as the length of time between when the clock exits the switching region and when the signal enters the switching region.

B. Data Transceiver Interface

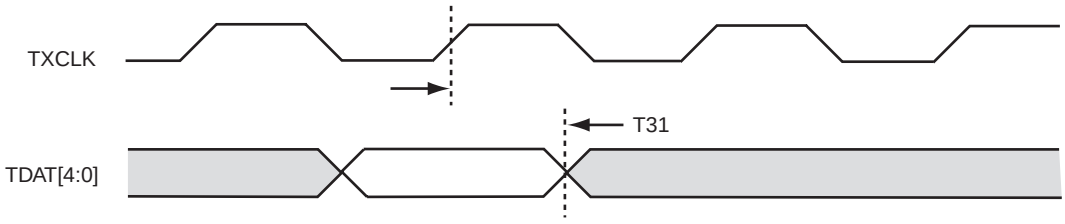


Figure 8-4 Trannsmit Signal Timing Relationships at the DT

Symbol	Description	MIN.	MAX.	UNIT
T31	TDAT[4:0] to TXCLK Rise Delay Time	5	15	ns

Note : Tested under 30pF loading.

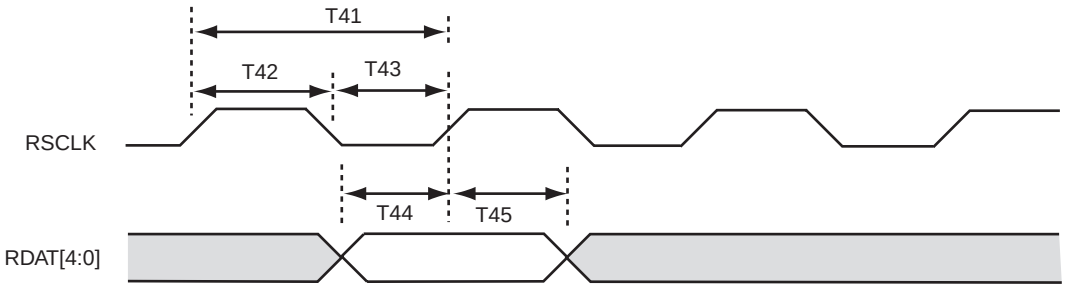


Figure 8-5 Receive Signal Timing Relationships at the DT

Symbol	Description	MIN.	MAX.	UNIT
T41	RSCLK Period (Note 1)	40	40	ns
T42	RSCLK Pulse Width High	10	-	ns
T43	RSCLK Pulse Width Time	20	-	ns
T44	RDAT[4:0] Valid to RSCLK Rise	2	-	ns
T45	RSCLK Rise to RDAT[4:0] Invalid	4	-	ns

Note 1 : The accurate RXCLK frequency shall be 25 MHz +/- 100 ppm.

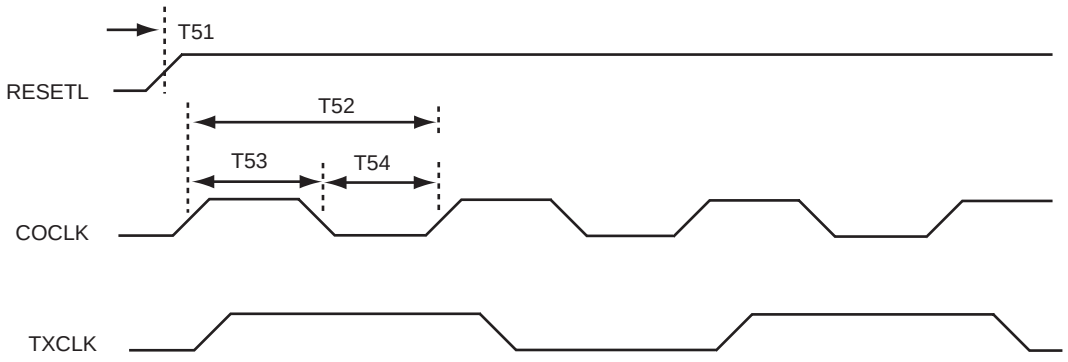


Figure 8-6 Timing Relationship for COCLK, TXCLK, and RESETL

Symbol	Description	MIN.	MAX.	UNIT
T51	Pulse Width for RESETL	2400	-	ns
T52	COCLK Period (Note 1)	20	20	ns
T53	COCLK Pulse Width High	8	-	ns
T54	COCLK Pulse Width Low	8	-	ns

Note 1 : The Maximum Frequency variation for COCLK shold be less than 100ppm.

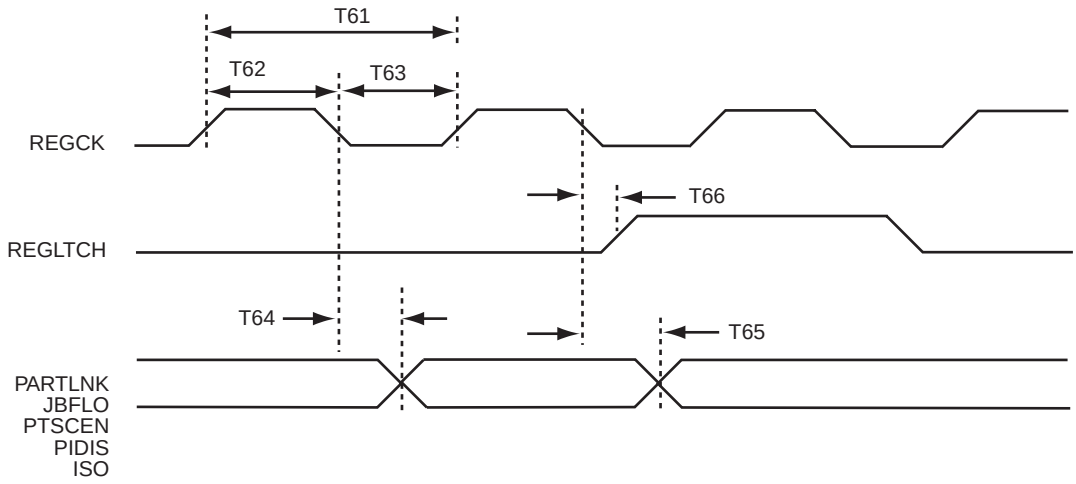


Figure 8-7 Timing Relationship for REGCK, REGLTCH and Round-Robin Status pins

D. Status Pins

Symbol	Description	MIN.	MAX.	UNIT
T61	REGCK Period	50	-	ns
T62	REGCK Pulse width High	12	-	ns
T63	REGCK Pulse Width LOW	12	-	ns
T64	REGCK falling to Status Valid	-	10	ns
T65	RegCK Falling to Status Invalid	-	12	ns
T66	REGCK falls to REGLTCH asserted (Note 1)	5	10	ns

Note 1 : One can use REGCK rising edge to latch data in system application.
Note 2 : Test under 30pF loading.

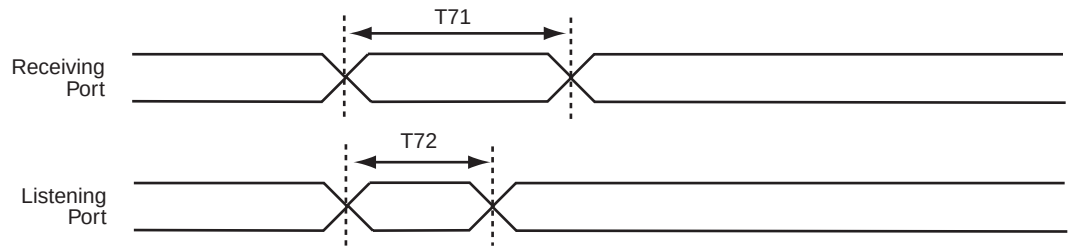


Figure 8-8 Receive Signal Timing Relationships at the DT

E. Network Interface Pins

Symbol	Description	MIN.	MAX.	UNIT
T71	Receiving Port goes to IDLE to activate again (Note)	100	-	ns
T72	Listening Port activate after other port IDLE (Note)	100	-	ns

Note : The restriction in IEEE 802.3u specifiction is 96BT. i.e 960 ns. Interframe Gap time less than the value shown above may cause packet loss and internal state machine malfunction.

F. Expansion Port Interface

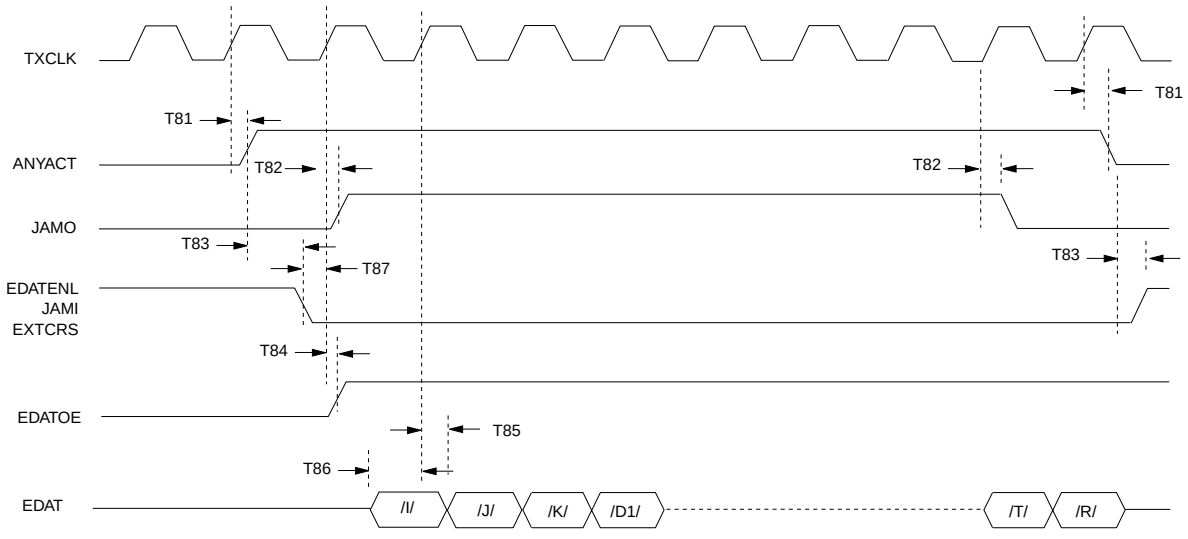


Figure 8-9 Expansion Port Timing Relationship

Symbol	Description	MIN.	MAX.	UNIT
T81	TXCLK rising to ANYACT assert/deassert	-	18	ns
T82	TXCLK rising to JAMO assert /deassert	-	13	ns
T83	ANYACT assert to EDATENL assert (Note)	-	17	ns
T84	TXCLK rising to EDATOE assert	-	25	ns
T85a	EDAT to TXCLK delay time (Output by MX98741)	12	26	ns
T85b	EDAT to TXCLK hold time (Input by MX98741)	4	-	ns
T86	EDAT to TXCLK setup time (Input by MX98741)	2	-	ns
T87	EDATENL asserted to TXCLK rising setup time	5	-	ns

Note :
If the external arbitor cannot generate EDATENL signals within 35 ns form TXCLK rising edge (or 17 ns after ANYACT is asserted in figure 9-9) for some reason, EDAT has to be delayed by one TXCLK cycle. Consequently, the longer the delay time changes the repeater from Class II to Class I. A 7ns PAL is suggested to be used for external arbitor to minimize the delay.

REVISION HISTORY

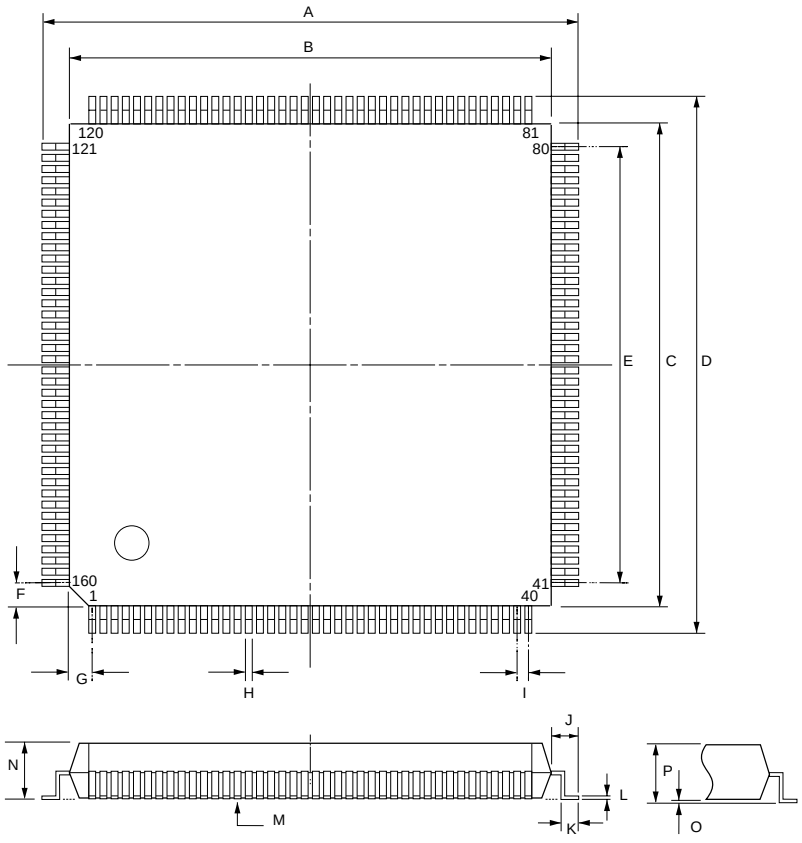
Revision	Description	Page	Date
1.4	(1) 5.2 Internal Registers, register 0, 1, and 16 can only be accessed through MDC and MD10.	P.13	NOV/07/1998
	(2) Delete the redundant page.	P.21	
	(3) Figure 8-6, delete T55.	P.35	
	(4) Figure 9-9, EDAT to TXCLK setup/hold time and EDATENL to TXCLK rising edge setup time are added.	P.38	

10.0 PACKAGE INFORMATION

208-PIN PLASTIC QUAD FLAT PACK

ITEM	MILLIMETERS	INCHES
A	31.20 ±.30	1.228 ±.12
B	28.00 ±.10	1.102 ± .004
C	28.00 ±.10	1.102 ±.004
D	31.20 ±.30	1.228 ±.012
E	25.35	.999
F	1.33 [REF.]	.052 [REF.]
G	1.33 [REF.]	.052 [REF.]
H	.30 [Typ.]	.012 [Typ.]
I	.65 [Typ.]	.026 [Typ.]
J	1.60 [REF.]	.063 [REF.]
K	.80 ±.20	.031 ±.008
L	.15 [Typ.]	.006 [Typ.]
M	.10 max.	.004 max.
N	3.35 max.	.132 max.
O	.10 min.	.004 min.
P	3.68 max.	.145 max.

NOTE: Each lead centerline is located within .25 mm[.01 inch] of its true position [TP] at maximum material condition.



MACRONIX INTERNATIONAL CO., LTD.

HEADQUARTERS:
TEL:+886-3-578-8888
FAX:+886-3-578-8887

EUROPE OFFICE:
TEL:+32-2-456-8020
FAX:+32-2-456-8021

JAPAN OFFICE:
TEL:+81-44-246-9100
FAX:+81-44-246-9105

SINGAPORE OFFICE:
TEL:+65-747-2309
FAX:+65-748-4090

TAIPEI OFFICE:
TEL:+886-3-509-3300
FAX:+886-3-509-2200

MACRONIX AMERICA, INC.
TEL:+1-408-453-8088
FAX:+1-408-453-8488

CHICAGO OFFICE:
TEL:+1-847-963-1900
FAX:+1-847-963-1909

http : //www.macronix.com