Description

The LG50N10 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

●

| V_{DSS}	$R_{DS(ON)}$ @4.5V (Typ)	$R_{DS(ON)}$ @10V (Typ)	I_D
100V	15 mΩ	14 mΩ	50A

● High density cell design for ultra low Rdson
● Fully characterized avalanche voltage and current
● Good stability and uniformity with high E_{AS}
● Excellent package for good heat dissipation
● Special process technology for high ESD capability

Application

● Power switching application
● LED backlighting
● Uninterruptible power supply
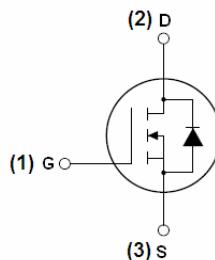
Schematic diagram

(2) D
(1) G
(3) S
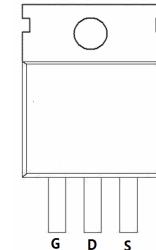
Marking and pin assignment

G D S
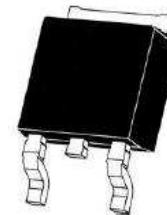
TO-252

Absolute Maximum Ratings (T_C=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	50	A
Drain Current-Continuous(T_C=100℃)	I_D (100℃)	35	A
Pulsed Drain Current	I_{DM}	150	A
Maximum Power Dissipation	P_D	130	W
Debating factor		0.87	W/℃
Single pulse avalanche energy [Note 5]	E_{AS}	450	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	℃

Thermal Characteristic

	Symbol		
Thermal Resistance,Junction-to-Case[Note 2]	$R_{θJC}$	1.15	℃/W

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Electrical Characteristics (T_C=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250µA	100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=100V,V_{GS}=0V	-	-	1	µA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250µA	0.9	1.3	1.7	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=30A	-	14	17	mΩ
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=30A	-	15	18	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V,I_D=30A	20	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{Iss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz	-	5320	-	PF
Output Capacitance	C_{oss}		-	950	-	PF
Reverse Transfer Capacitance	C_{rss}		-	360	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=50V,I_D=2A,R_L=1Ω V_{GS}=10V,R_{GEN}=3Ω	-	17	-	nS
Turn-on Rise Time	t_r		-	9	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	48	-	nS
Turn-Off Fall Time	t_f		-	36	-	nS
Total Gate Charge	Q_g	V_{DS}=50V,I_D=30A, V_{GS}=10V	-	73	-	nC
Gate-Source Charge	Q_{gs}		-	11	-	nC
Gate-Drain Charge	Q_{gd}		-	18	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=30A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S		-	-	50	A
Reverse Recovery Time	t_{rr}	TJ = 25℃, IF =30A di/dt = 100A/µs (Note3)	-	43		nS
Reverse Recovery Charge	Qrr		-	46		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. Surface Mounted on FR4 Board, t ≤ 10 sec.

3. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

5. E_{AS} condition: Tj=25℃,V_{DD}=30V,V_G=10V,L=0.5mH,Rg=25Ω

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Test circuit

1) E$_{AS}$ test Circuits

BV$_{DSS}$ L

R$_G$

+ V$_{DD}$ -
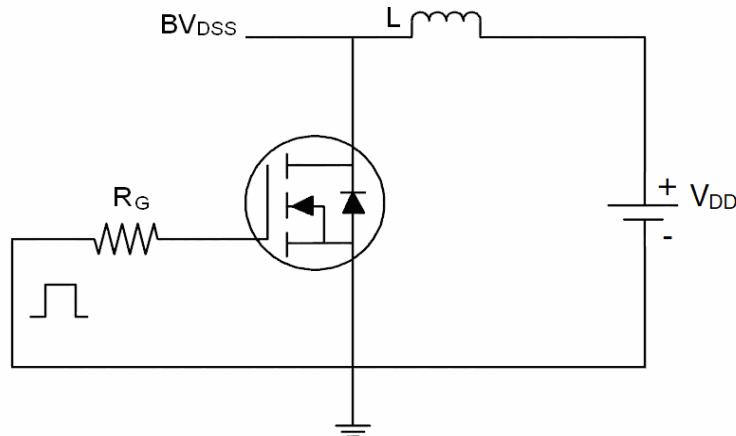
2) Gate charge test Circuit

0

1K

DUT

L

VCC
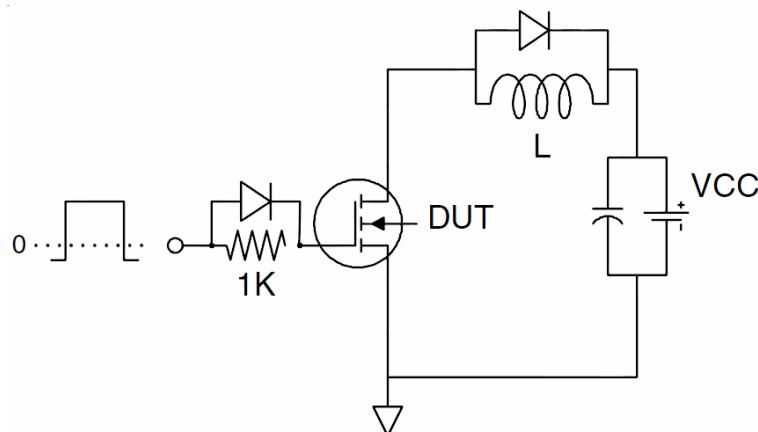
3) Switch Time Test Circuit

V$_{DS}$ R$_L$

R$_G$

+ V$_{DD}$ -

D.U.T

V$_{GS}$
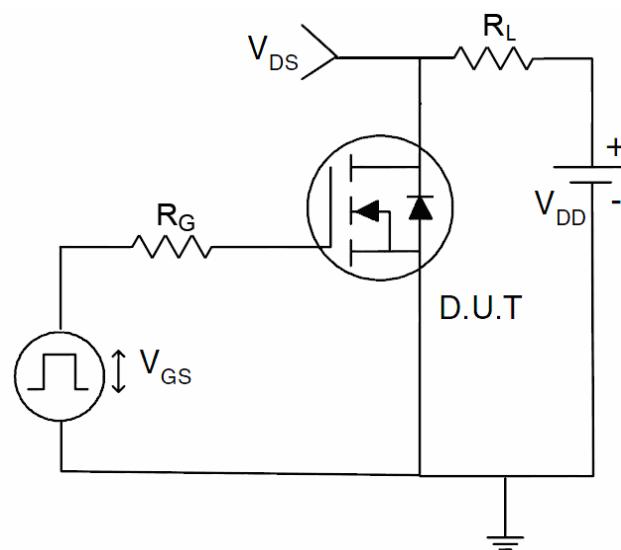
Typical Electrical and Thermal Characteristics (Curves)
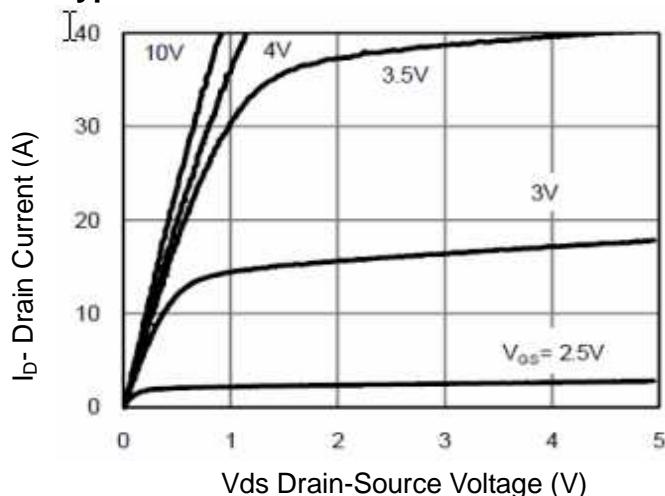
Figure 1 Output Characteristics
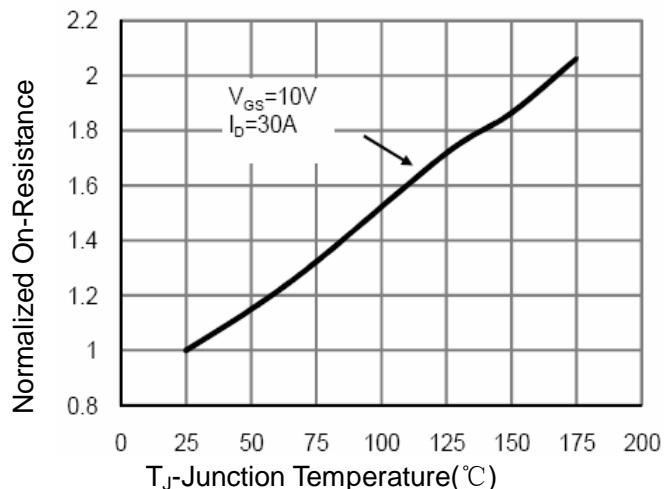
Figure 4 Rdson-JunctionTemperature
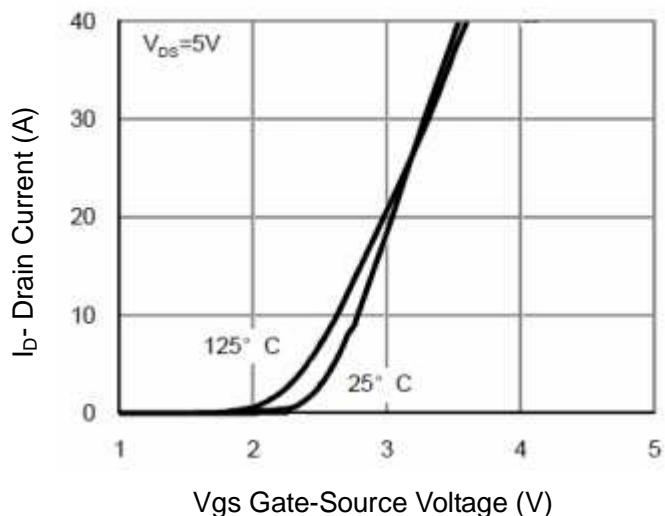
Figure 2 Transfer Characteristics
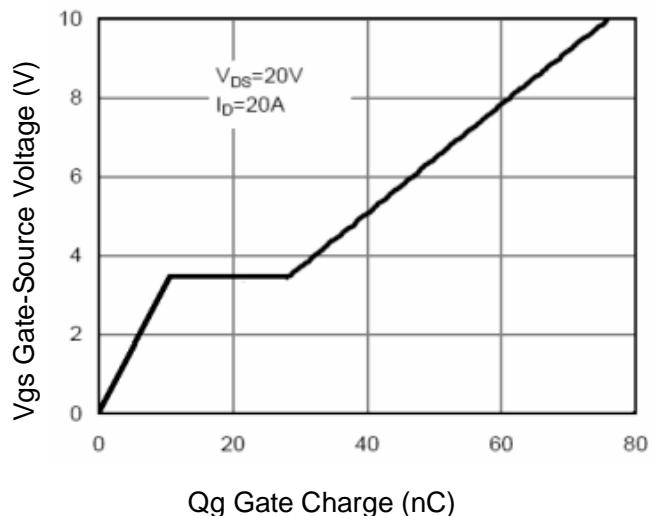
Figure 5 Gate Charge
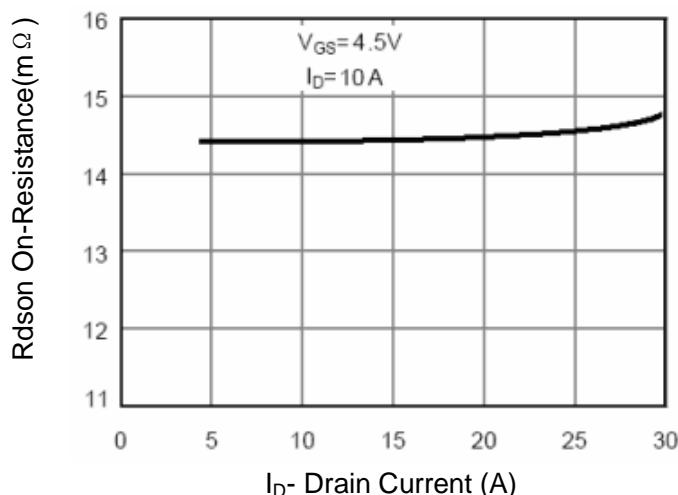
Figure 3 Rdson- Drain Current
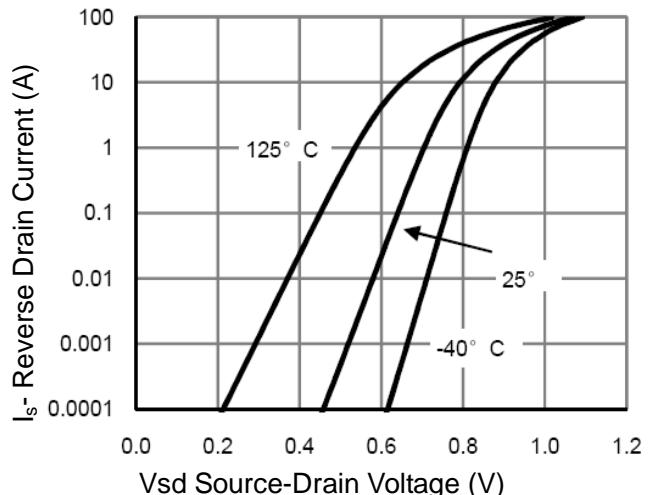
**Figure 6 Source- Drain Diode Forward**
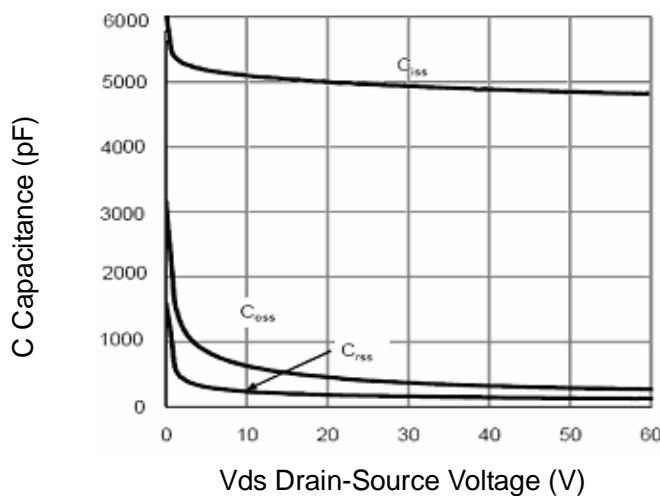
Figure 7 Capacitance vs Vds
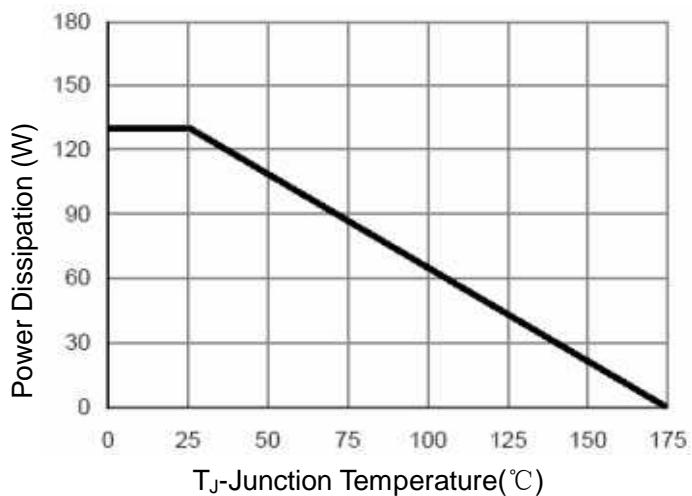
Figure 9   Power De-rating
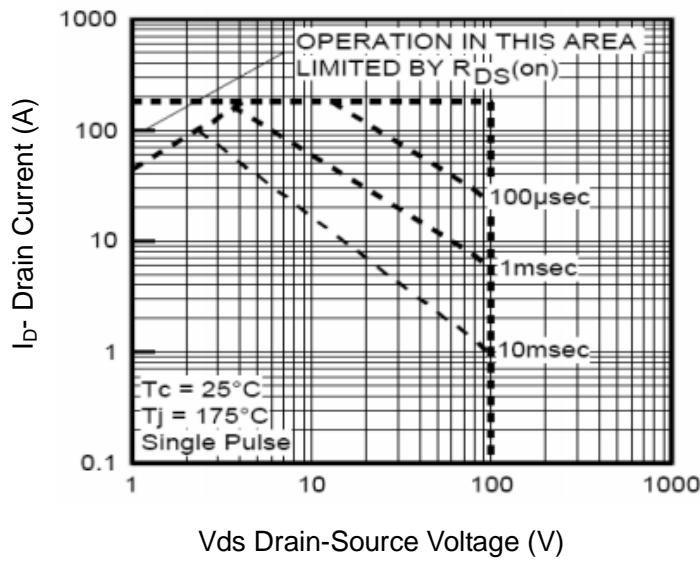
**Figure 8 Safe Operation Area**

Square Wave Pluse Duration(sec)
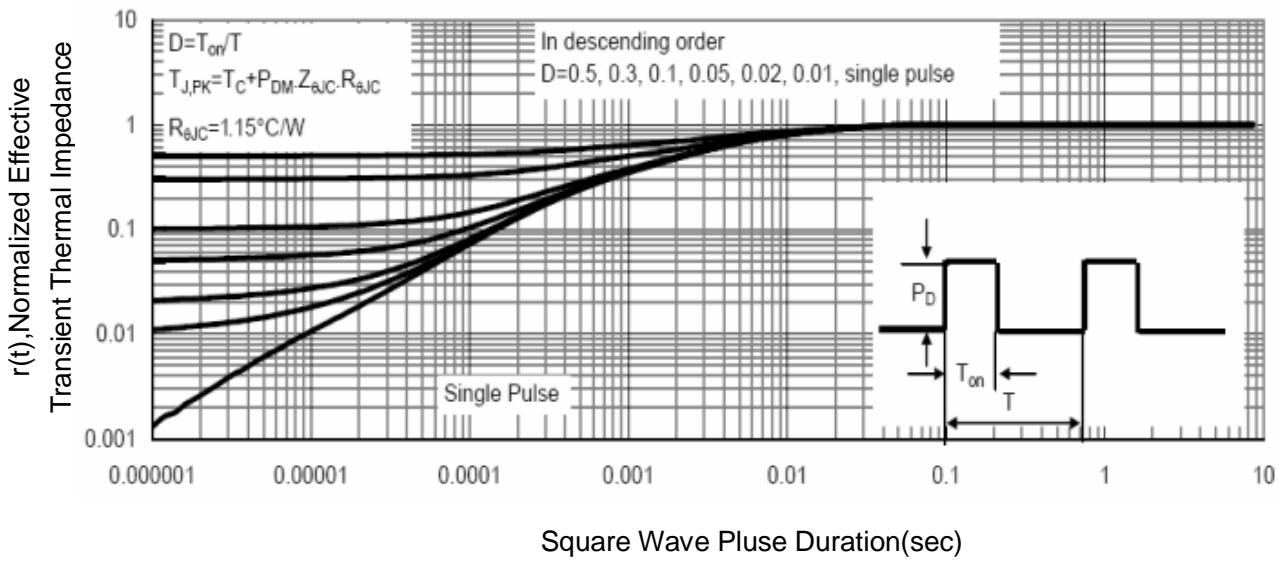
Figure 10 Normalized Maximum Transient Thermal Impedance

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