4-28V Input 8A Output Power Supply in Inductor (PSI²) Module

RoHS compliant

FEATURES

- **Integrated Point of Load power module using PSI² Power Supply in Inductor technology**
- **Small Footprint, low-profile, 15mm x 9mm x 3mm, with LGA Package (0.63 mm pads)**
- **Efficiency of 94% at 4A and 93% at 6A for 5V output, 12V input**
- **Up to 8A maximum output current; up to 6A at 85°C ambient with no air flow**
- **±4% Output Voltage Regulation**
- **Single resistor output voltage programming for voltages from 0.6V to 5V**
- **Output voltage remote sensing**
- **Input voltage range 4V to 28V**
- **Pre-bias start up capability**
- **Enable signal input and Power Good signal output**
- **Output voltage sequencing**
- **Programmable Under Voltage Lock Out (UVLO)**
- **Output Over-Current Protection (OCP)**
- **Operating temperature range -40°C to 85°C**
- **Qualified to IPC9592B, Class II**
- **MSL3 and RoHS compliant**

APPLICATIONS

- **Broadband and communications equipment**
- **DSP and FPGA Point of Load applications**
- **High density distributed power systems**
- **Automated PCI / PCI express / PXI express**
- **Automated test and medical equipment**

DESCRIPTION

SPM1006 is an easy-to-use 8A output integrated Point of Load (POL) power supply module. It contains power MOSFETs, driver, PWM controller, a high performance inductor, input and output capacitors and other passive components in one low profile LGA package using PSI² technology.

Only one external input capacitor and one external output capacitor are needed for typical applications. There is no need for loop compensation, sensitive PCB layout, inductor selection, or in-circuit production testing.

The SPM1006 can be programmed for any output voltage between 0.6V and 5.0V using a single external resistor. For an output voltage of 0.6V no resistor is required.

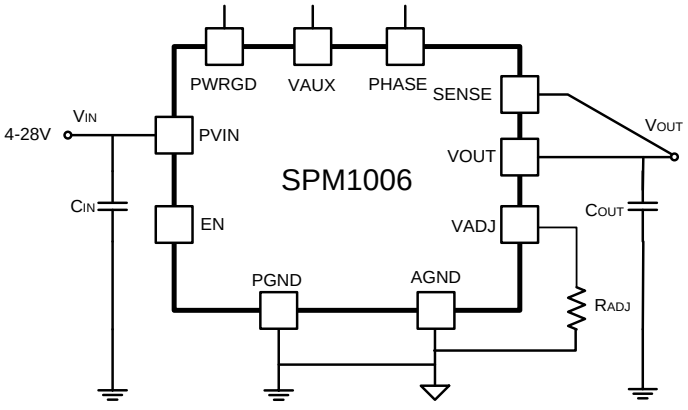
The SPM1006 delivers up to 8A load current, and can deliver up to 6A at 85°C ambient temperature with no airflow.

Small size (15mm x 9mm) and low profile (3mm) allows the SPM1006 to be placed very close to its load, or on the back side of the PCB board for high density applications.

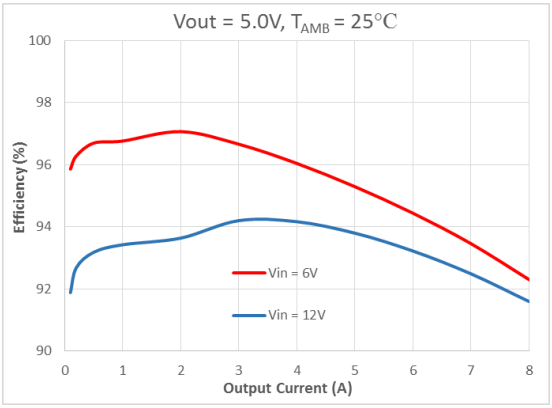
Instant PWM control is used to achieve excellent transient response to line and load changes without sacrificing stability and high efficiency at light load.

Sumida's PSI² technology ensures optimal inductor design, uniform temperature distribution and very low temperature difference between case and IC die.

SIMPLIFIED APPLICATION



EFFICIENCY VS LOAD CURRENT



ABSOLUTE MAXIMUM(1) RATINGS over operating temperature range (unless otherwise noted)

		VALUE		Unit
		MIN	MAX	
Inputs	PVIN	-0.3	30	V
	EN	-0.3	30	V
	VSENSE	-0.3	30	V
	VADJ	-0.3	4	V
Outputs	VOUT	-0.6	PVIN	V
	PHASE	-0.6	PVIN	V
	PWRGD	-0.3	30	V
	VAUX	-0.3	4	V
Temperature	Operating Junction Temperature	-40	150	°C
	Storage Temperature	-65	150	°C
	Lead Temperature (10 seconds max)		260	°C

(1) Stresses beyond these absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

The electrical performance is based on the following conditions unless otherwise stated: 25°C ambient temperature, no air flow; V_{IN} = 12V, I_{OUT} = 6A, C_{IN} = 4X 22µF ceramic, C_{OUT} = 2X 100µF ceramic.

PARAMETERS		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Specifications							
V_{IN}	Input voltage [**Note 1**]	Over I_{OUT} range		4	12	28	V
V_{START}	Start up voltage [**Note 2**]	Over I_{OUT} range			3.65		V
V_{EN_ON}	Enable on voltage	Enable high voltage (module turned on)				0.8	V
V_{EN_OFF}	Enable off voltage	Enable low voltage (module turned off)		0.4			V
I_{STBY}	Input standby current	EN pin to PGND (shut down)			0.3		mA
		EN = 2V, I_{OUT} = 0A				1.5	mA
UVLO Under Voltage Lock Out [**Note 2**]					3.55		V
UVLO Hysteresis					0.1		V
Output Specifications							
I_{OUT}:	Output continuous current	T_A = -40°C to 85°C, natural convection		0		6	A
I_{OUT}:	Maximum current	T_A = -40°C to 50°C, refer to Fig. 28-Fig. 30				8	A
V_{OUT}	Set point accuracy [**Note 3**]	T_A = 25°C, V_{IN} = 12V, I_{OUT} = 3A			±1.5%		
	Temperature variation	-40°C < T_A < +85°C, I_{OUT} = 3A			±1%		
	Line regulation	Over V_{IN} range, T_A = 25°C, I_{OUT} = 3A			±0.5%		
	Load regulation	Over I_{OUT} range, T_A = 25°C, V_{IN} = 12V			±1%		
	Total variation [**Note 3**]	Set-point, line, load, temperature variation				±4%	
$V_{OUT(adj)}$: Output voltage adjust range		Over I_{OUT} range [**Note 4**]		0.6		5.5	V
V_{o_rip},	Output voltage ripple	20MHz bandwidth, V_{IN} = 12V, I_{OUT} = 6A			20		mVpp
V_{AUX}: Auxiliary output		Output voltage			3.3		V
		Output current				10	mA
OVP	Over-voltage Protection	OVP threshold (percentage of nominal)		115%	120%	125%	
		OVP shutdown delay			20		µs
PWRGD	Power Good Signal	V_{OUT} rising (% of V_{OUT})	PWRGD high	88%	90%	92%	
			PWRGD delay		10		µs
		V_{OUT} falling (% of V_{OUT})	Hysteresis		2%		
F_S	Switching frequency	V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 6A			760		kHz
Performance Specifications							
η	Efficiency (V_{OUT} = 5V)	V_{IN} = 12V	I_{OUT} = 3A		94.2%		
			I_{OUT} = 6A		93.2%		
Transient Response (V_{OUT} = 5V)		1A/µs load step between 3A and 6A	Over/undershoot		55		mV
			Recovery time		150		µs
Soft-Start Time		V_{IN} = 12V, Over I_{OUT} range			500		µs
Current Limit and Thermal Specifications							
I_{LIM}	Current Limit Point	V_{IN} = 12V		8	11		A
Thermal shutdown (die temperature)		Thermal shutdown			150		°C
		Thermal shutdown recovery hysteresis			15		°C

Note 1: Input voltage must be at least 1.5V higher than the output voltage

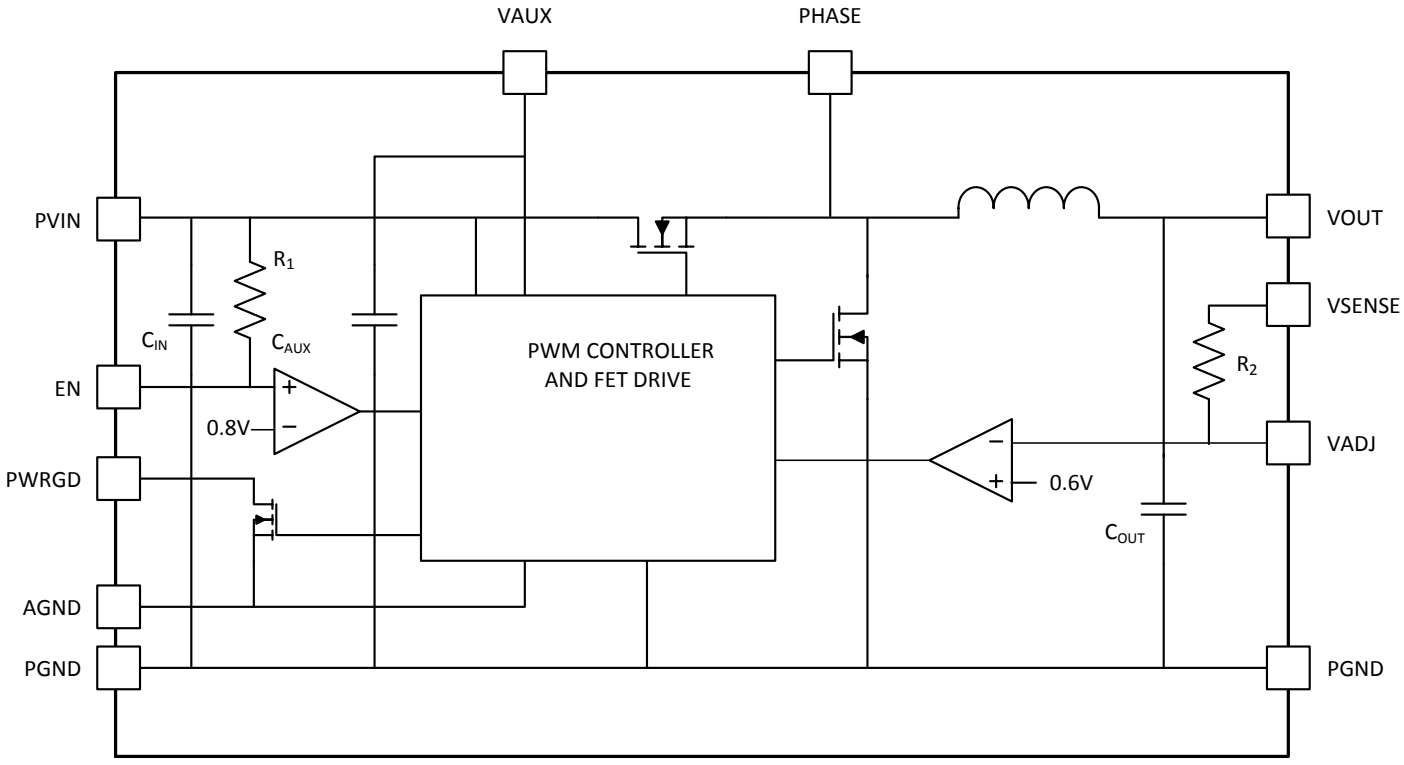
Note 2: Startup voltage and UVLO are with no external resistor; startup and UVLO can be increased using an external programming resistor – refer to Startup Voltage on page 13.

Note 3: With 0.1% tolerance external voltage set resistor.

Note 4: For applications requiring output voltage higher than 5V, please consult Sumida.

POWER MODULE INFORMATION

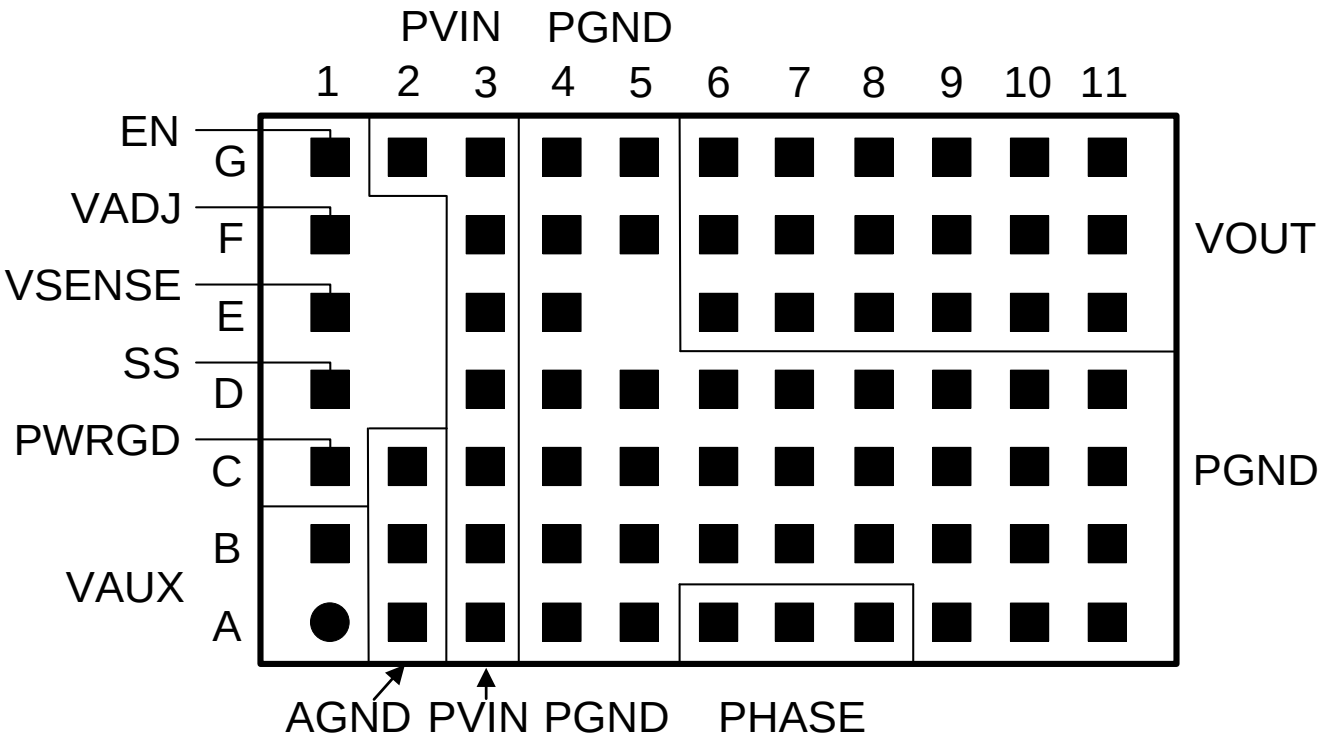
FUNCTIONAL BLOCK DIAGRAM for SPM1006



PIN DESCRIPTIONS

PIN Name	Description
PVIN (A3, B3, C3, D3, E3, F3, G2-G3)	**Input voltage pins, referenced to PGND**. Connect input ceramic capacitors between these pins and PGND plane, close to the power module. It is suggest to place the ceramic capacitors at both sides of the module, one between PIN A3 and PIN A4-A5 and one between PIN G2-G3 and PIN G4-G5.
VAUX (A1, B1)	**Auxiliary output** from an LDO in the module, which is referenced to AGND. An external capacitor is not normally necessary but can be added if required. **Note:** VAUX pin can only provide 10mA maximum current.
PHASE (A6-A8)	**Switching node of the Buck converter**. Please connect these pins together using a small and isolated copper plane under the device for better thermal performance. Do not connect any external component to these pins. Do not use these pins for other functions.
VOUT (E6-E11, F6-F11, G6-G11)	**Output voltage pins.** Connect these pins together onto a copper plane. Connect external output filter capacitors between these pins and PGND plane, close to the device.
PGND (A4-A5, A9-A11, B4-B11, C4-C11, D4-D11, E4, F4-F5, G4-G5)	**Zero DC voltage reference for power circuitry**. These pins should be connected directly to the PCB ground plane. All pins must be connected together externally with a copper plane or poured directly under the module.
AGND (A2, B2, C2)	**Zero DC voltage reference for the analog control circuitry.** A small analog ground plane is recommended. VADJ, SS, and VSENSE pins should be referenced to analog ground. These pins should be connected directly to the PCB analog ground plane. A single point connection between AGND and PGND in motherboard is recommended.
EN (G1)	**Enable pin**. When above Enable On Voltage (V_{EN_ON}), the power module will be turned on when the power input voltage (PVIN) is above start up voltage (V_{START}). When EN pin is below Enable Off Voltage (V_{EN_OFF}), the power module will be off.
VADJ (F1)	**Output voltage programming pin.** Connect a resistor between this pin and PGND top set the output voltage.
VSENSE (E1)	**Remote sensing pin.** Connect this pin to VOUT close to the load for improved voltage regulation. **Note**: this pin is not connected to VOUT inside the module, and must be connected externally.
NC (D1)	There is no connection to this pin. Leave open or connect to PGND
PWRGD (C1)	**Power Good pin**, an open drain output. A resistor connected between PWRGD and any voltage up to V_{IN} can be used. PWRGD is high if the output voltage is higher than 90% of the nominal value. It will be pulled down if the output voltage is less than 80% or higher than 120% of the nominal value.

LGA PACKAGE
73 PINS,
(TOP VIEW)



TYPICAL EFFICIENCY AND POWER LOSS DATA (Note 1)

A. Efficiency and power loss at 12V input

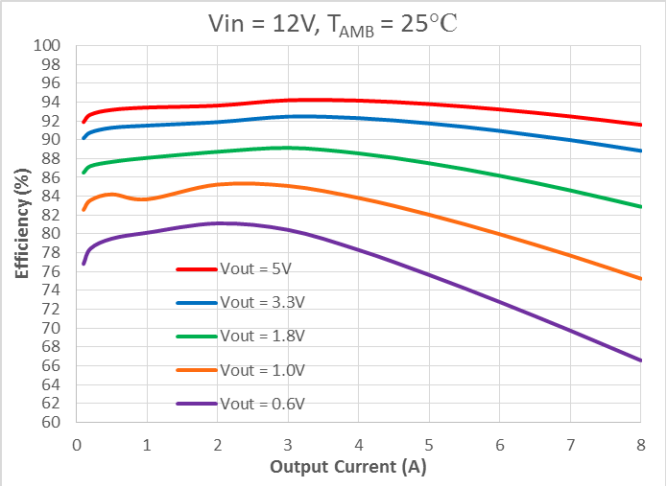


Fig. 1 Efficiency vs Output Current (V_{IN}=12V)

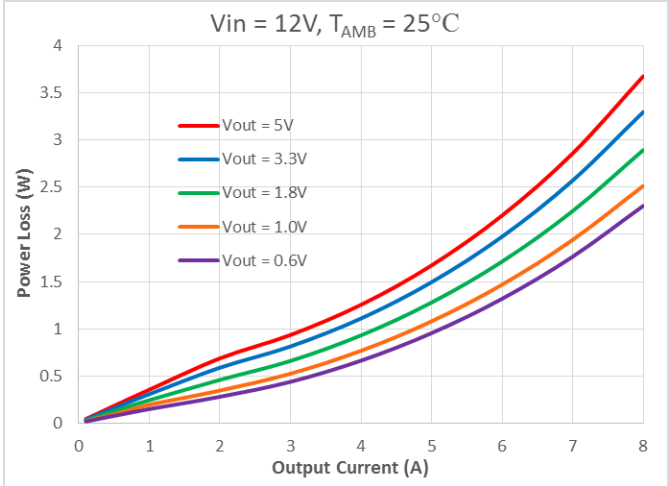


Fig. 2 Power Dissipation vs Output Current (V_{IN}=12V)

B. Efficiency and power loss at min, nominal and max input

V_{OUT} = 5V, T_A = 25°C

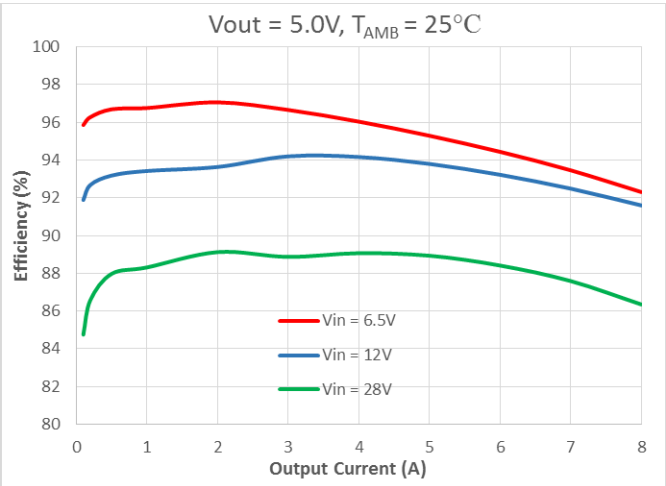


Fig. 3 Efficiency vs Output Current (V_{OUT}=5V)

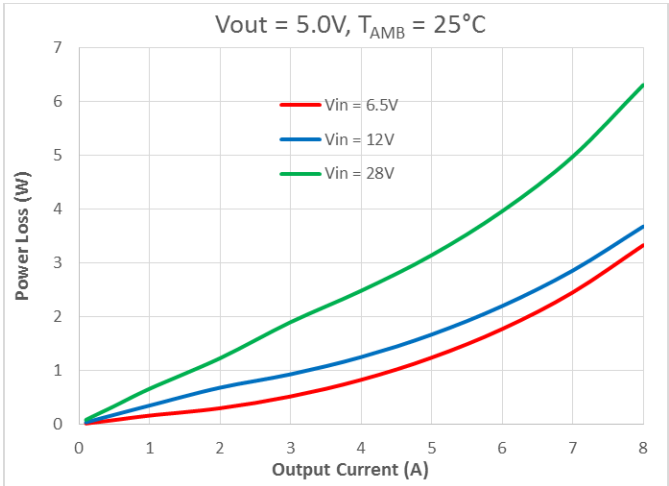


Fig. 4 Power Dissipation vs Output Current (V_{OUT}=5V)

V_{OUT} = 3.3V, T_A = 25°C

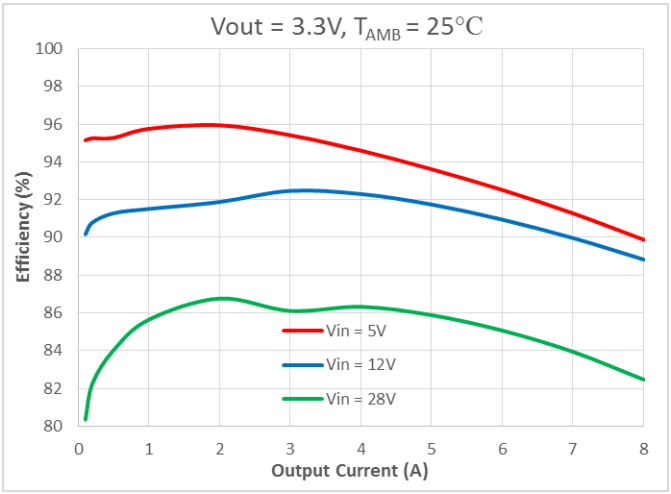


Fig. 5 Efficiency vs Output Current (V_{OUT}=3.3V)

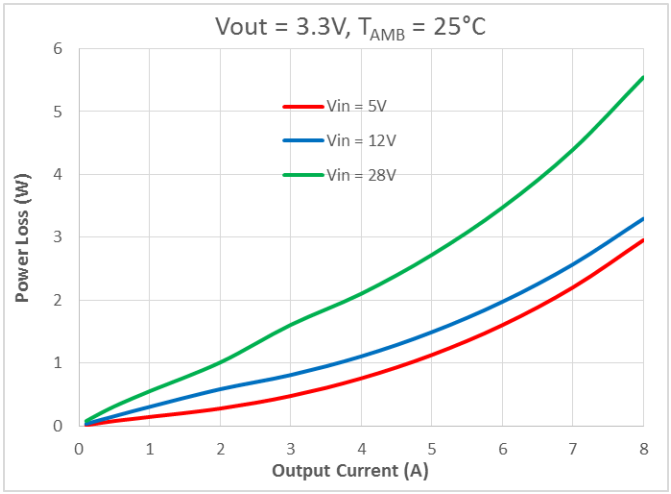


Fig. 6 Power Dissipation vs Output Current (V_{OUT}=3.3V)

V_{OUT} = 1.8V, T_A = 25°C

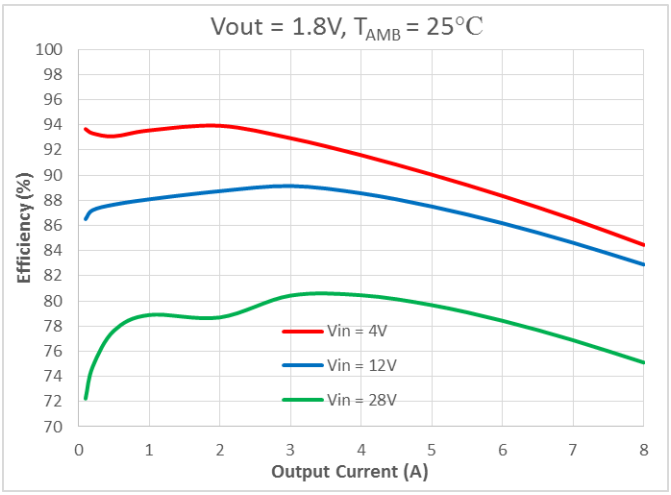


Fig. 7 Efficiency vs Output Current (V_{OUT}=1.8V)

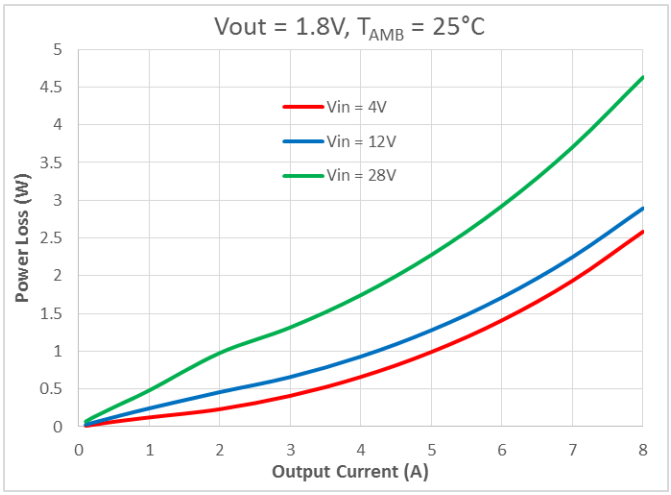


Fig. 8 Power Dissipation vs Output Current (V_{OUT}=1.8V)

V_{OUT} = 1.0V, T_A = 25°C

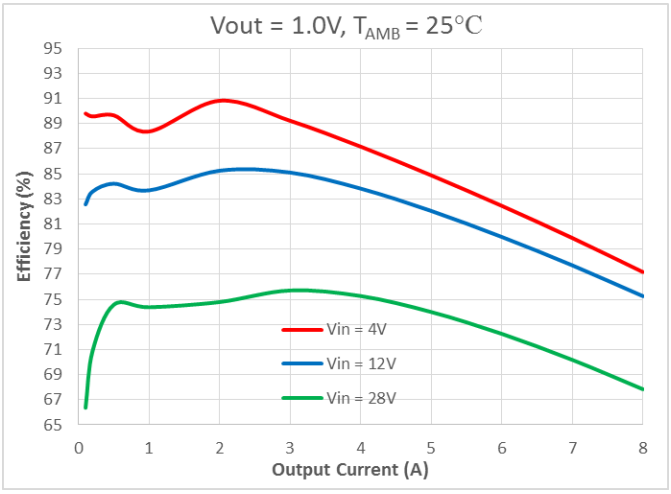


Fig. 9 Efficiency vs Output Current (V_{OUT}=1.0V)

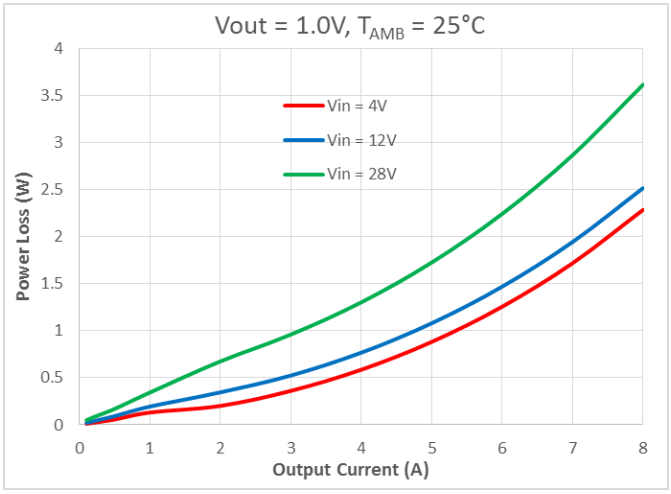


Fig. 10 Power Dissipation vs Output Current (V_{OUT}=1.0V)

V_{OUT} = 0.6V, T_A = 25°C

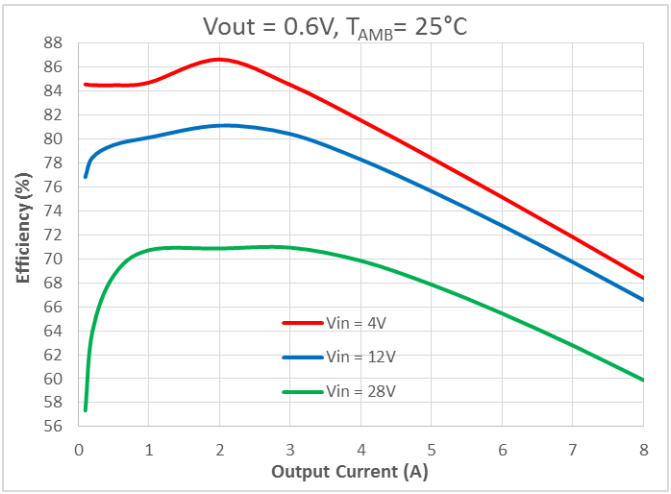


Fig. 11 Efficiency vs Output Current (V_{OUT}=0.6V)

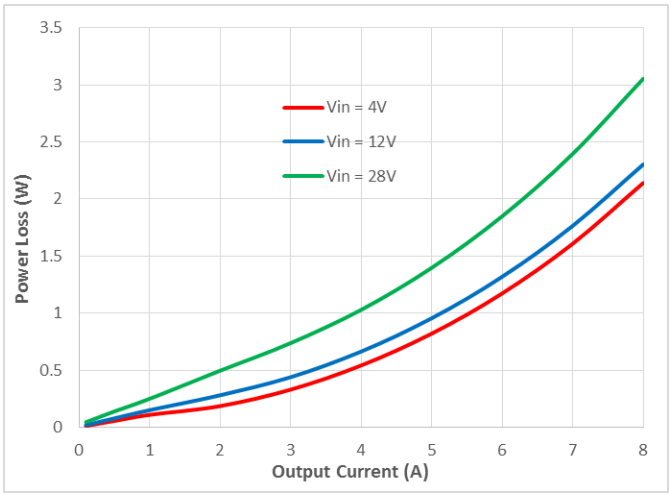


Fig. 12 Power Dissipation vs Output Current (V_{OUT}=0.6V)

Note 1: The above curves (Figure 1 to Figure 12) are derived from measured data taken on samples of the SPM1006 tested at room temperature (25°C), and are considered to be typical for the product.

APPLICATION INFORMATION

Output Voltage Programming

The output voltage is programmed using a resistor R_{PROG} from VADJ to PGND, as shown in Fig. 13. By default, the output voltage is 0.6V without a resistor connected.

Note that the input voltage must be at least 1.5V higher than the output voltage

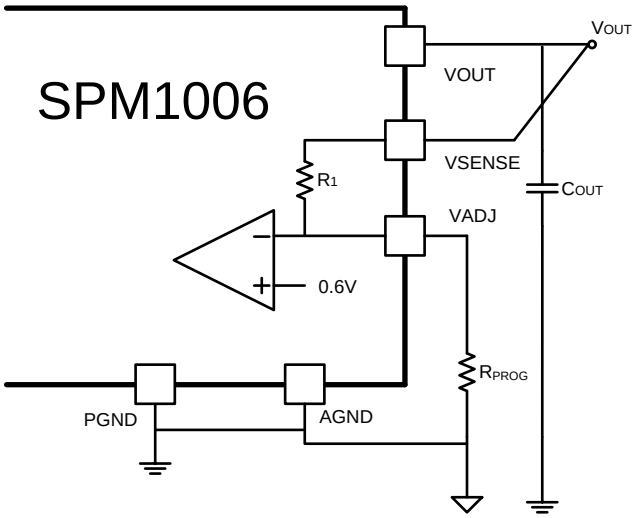


Fig. 13 Output Voltage Programming Circuit

A single standard 1% resistor can be used to program for any of the common voltages shown in Table 1.

Table 1 - Output Voltage Programming Resistor

0.8V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5.0V
33.2kΩ	16.5kΩ	11kΩ	7.32kΩ	5.49kΩ	3.48kΩ	2.43kΩ	1.5kΩ

The programming resistor can be calculated for any output voltage using equation (1).

$$R_{PROG} = \frac{11k\Omega}{V_{OUT} / 0.6V - 1} \quad (1)$$

Note that the VADJ pin is noise sensitive and the connections to this pin should be kept as short as possible.

To further adjust the output voltage, another resistor R_{TRIM} may be connected between VSENSE and VADJ, as shown Fig. 14. The resulting output voltage is a function of equation (2).

$$V_{OUT} = 0.6V * (1 + \frac{(\frac{R_{TRIM} * 11k\Omega}{R_{TRIM} + 11k\Omega})}{R_{PROG}}) \quad (2)$$

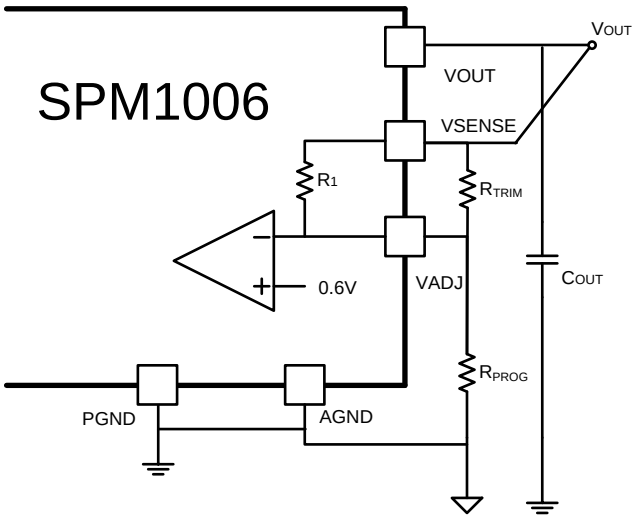


Fig. 14 Output Voltage Trim Circuit

Enable (EN) Control

The EN pin provides an electrical on/off control of the power module. Once the voltage at the EN pin exceeds the threshold voltage (0.8V) or is left open, the power module starts operation when the input voltage is higher than the input start up voltage (V_{START}).

When the voltage at EN pin is pulled below the threshold voltage, the switching converter stops switching and the power module enters low quiescent current state.

If an application requires controlling the EN pin, an open drain or open collector output logic can be used to interface with the pin, as shown in Fig. 15, where high ON/OFF signal (low EN) disables the power module.

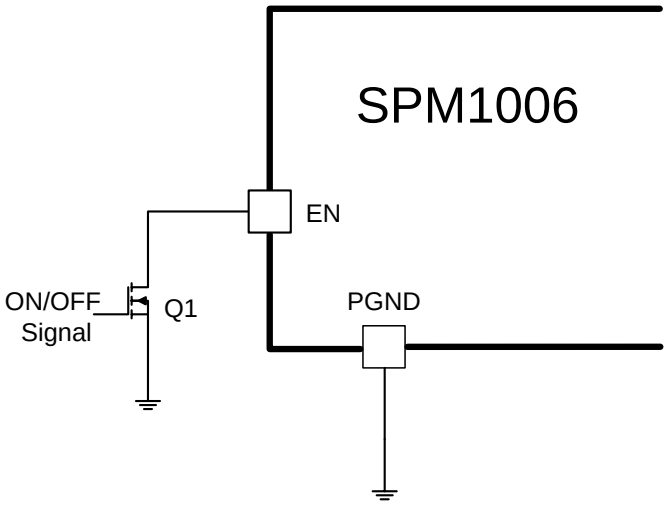


Fig. 15 Typical ON/OFF Control

When EN pin is open (or connected to a logic high voltage), SPM1006 produces a regulated output voltage following the application of a valid input voltage. Fig. 16 shows the startup waveform for SPM1006 without EN control. The top trace is input voltage, the middle trace is Power Good signal (PWRGD), and the bottom trace is the output voltage.

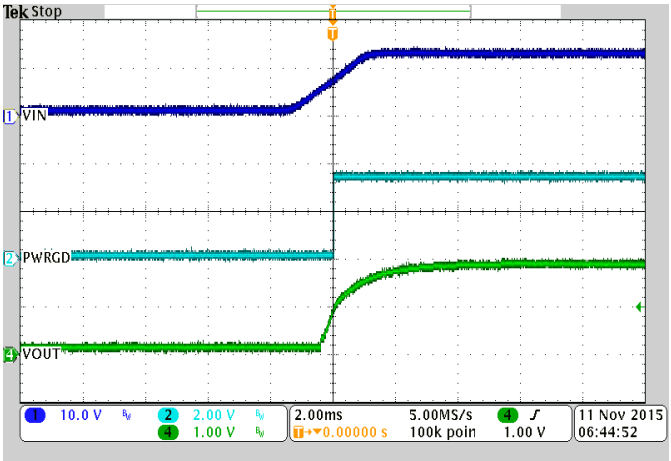


Fig. 16 Start-Up Waveforms for SPM1006
(set to 1.8V output) without EN control

Fig. 17 and Fig. 18 show the typical output voltage waveforms when SPM1006 is turned on and turned off by the EN pin. In these figures, the top trace is enable signal (EN), the middle trace is Power Good signal (PWRGD), and the bottom trace is the output voltage.

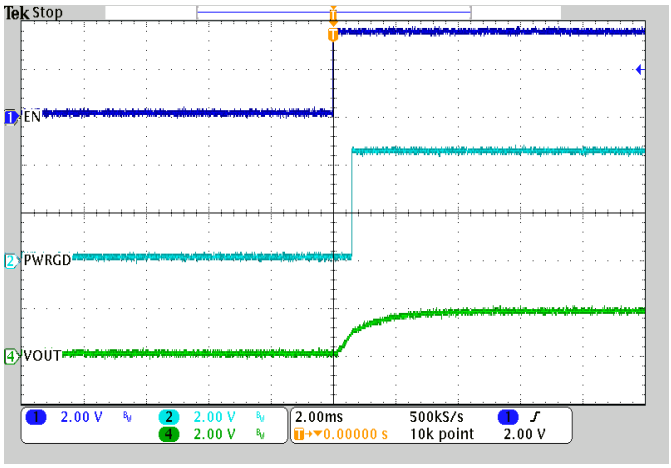


Fig. 17 Enable Turn-On for SPM1006
(set to 1.8V, with I_{OUT} = 6A)

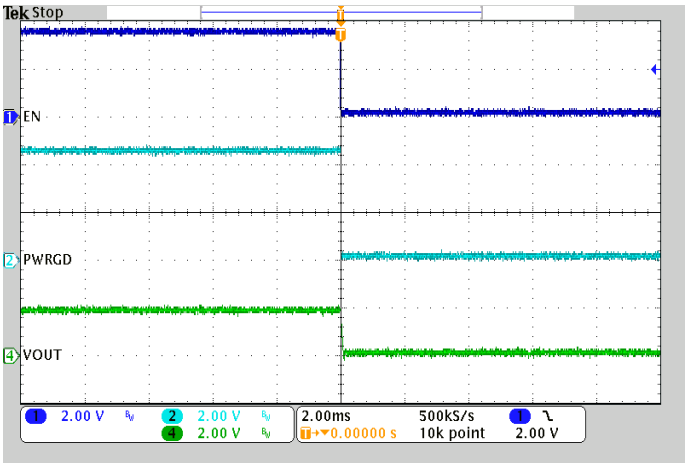


Fig. 18 Enable Turn-Off for SPM1006
(set to 1.8V, with I_{OUT} = 6A)

The startup and shutdown waveforms are similar for other output voltages.

Pre-bias Startup

Some applications require startup when there is a residual pre-bias voltage on the output. The SPM1006 can start in this condition and as long as the pre-bias voltage is lower than the final output the start-up waveform will be normal. Fig. 19 illustrates start up with pre-bias of approximately 50% of the nominal output voltage. Fig. 20 shows the start-up when the pre-bias is about 80% of the nominal output.

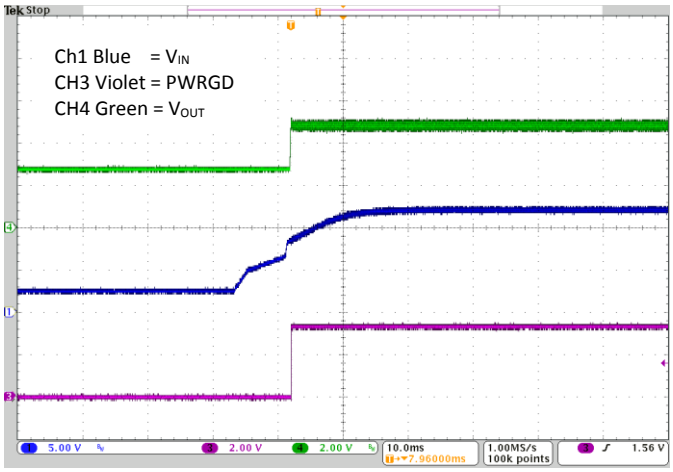


Fig. 19 Start-up with pre-bias 2.62V (V_{OUT}=5V)

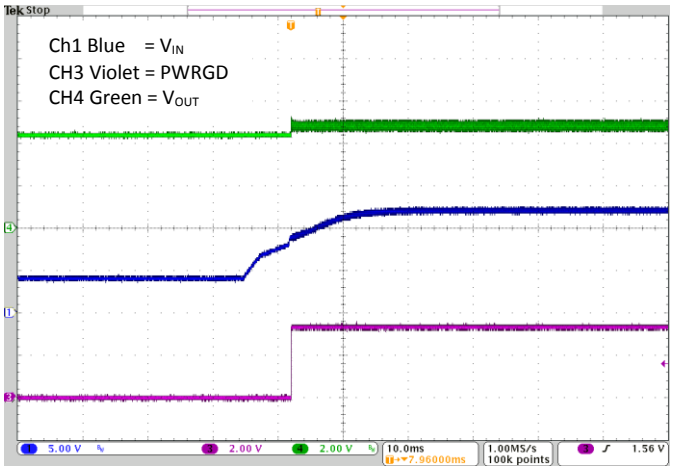


Fig. 20 Start-up with pre-bias 4.21V (V_{OUT}=5V)

Start Up Voltage

By default, the SPM1006 will turn on when the input voltage reaches the startup voltage (V_{START}). The SPM1006 will turn off when the input voltage reduces to below the Under Voltage Lock-Out (UVLO) level. Startup voltage cannot be reduced below the values provided in the table of Electrical Characteristics. Startup voltage can be increased by an external resistor (R_{EN}) connected between EN pin and PGND pin.

The resistor value R_{EN} (in kΩ) can be calculated using equation (3) below based on the required start up voltage, V_{START}. Note: V_{START} must be higher than 3.9V.

$$R_{EN} = \frac{400}{(5V_{START} - 4)} \quad (3)$$

For example, to set the start-up voltage to 9.0V the value of R_{EN} will be 9.76 kΩ.

The shutdown voltage is given by equation (4) below:

$$V_{SHUTDOWN} = \frac{0.4 * (100 + R_{EN})}{R_{EN}} \quad (4)$$

For example, if R_{EN} = 9.76 kΩ the shutdown voltage will be 4.5V.

Power Good (PWRGD)

The PWRGD pin is an open drain output. Connect a pull up resistor (10kΩ to 100kΩ) between PWRGD pin and VAUX pin, or to a suitable external voltage. [Note: maximum voltage on this pin is V_{IN}, but any lower voltage logic level can be used.] PWRGD signal becomes high when the output voltage reaches 90% of normal output voltage. The PWRGD signal becomes low when the output voltage is lower than 80% or higher than 120% of the normal output voltage.

Soft Start Operation

Soft-start operation is internal to the SPM1006. It has an internally programmed fixed start-up time of 600us nominal for any output voltage setting and load current.

Input and Output Capacitance

Recommended minimum capacitance is 47µF ceramic (input) and 150µF ceramic (output). Additional capacitors can be connected in parallel if required, to reduce output ripple and improve transient response.

Application Schematics

Fig. 21 shows a typical application schematic for 12V input and 3.3V output. Startup voltage is set to 9V using the resistor R_{EN}, with value 9.76 kΩ. If required, a MOSFET can also be connected to the EN pin, as shown in Fig. 15 to provide on-off control.

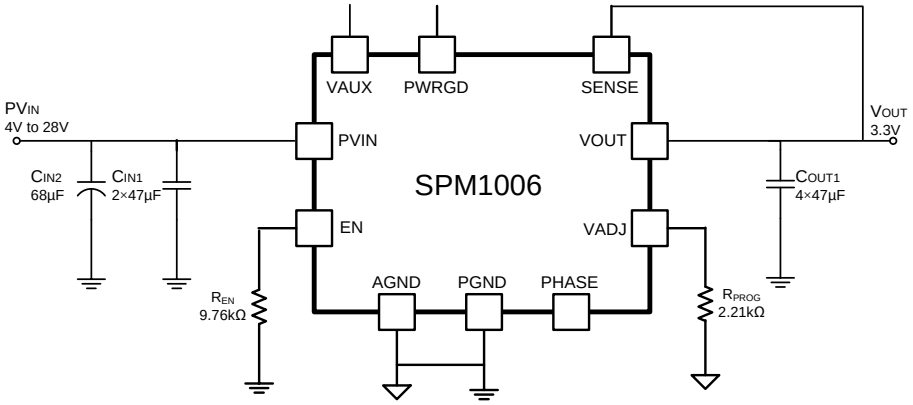


Fig. 21 Typical schematic for V_{IN} = 12V, V_{OUT} = 3.3V with start-up voltage set to 9V

Sequencing Operation

The term *sequencing* is used when two or more separate modules are configured to start one after the other, in sequence.

Sequencing operation between two or more SPM1006 power modules can be implemented with PWRGD pin and EN pin. Fig. 22 shows an example configuration when one SPM1006 (set to 5V) starts first and a second SPM1006 (set to 3.3V) starts after the output voltage of the first SPM1006 has reached 5V. In this case, the Power Good signal (PWRGD) of the first module turns on the second module through the EN pin.

Fig. 23 shows the output voltage waveforms of two SPM1006 modules used in sequential start-up mode. It shows that PWRGD signal becomes high when the first SPM1006 enters into regulation, and then the second SPM1006 starts up.

Note: The SPM1006 can start in sequence with another SPM1006 or with any other POL having a compatible Power Good output. All Sumida power modules are fully compatible and can operate in sequence.

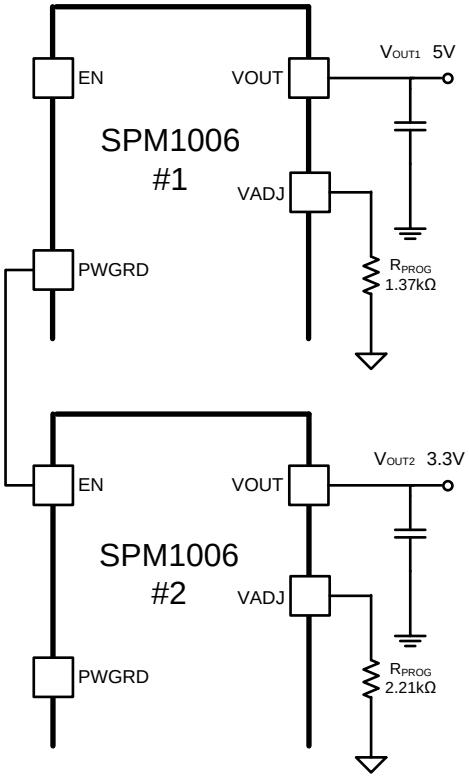


Fig. 22 Sequential Startup, V_{OUT1} = 5V, V_{OUT2} = 3.3V

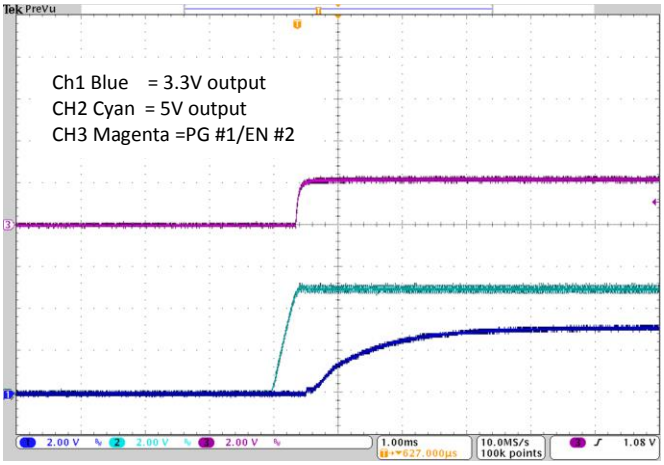


Fig. 23 Typical sequential startup waveforms

Transient Response

SPM1006 uses instant PWM control and achieves excellent transient performance. The following table summarizes the measured data when the load current undergoes a step change between 2A and 5A for output voltage setting of 5V and input voltage of 12V. The slew rate for the load current change is 1A/µs.

V_{OUT} setting	Transient voltage (3A step)	Recovery time
5V	40mV	150µs
0.6V	20mV	50µs

The measured transient waveform for 5V output is given in Fig. 24, and for 0.6V output in Fig. 25.

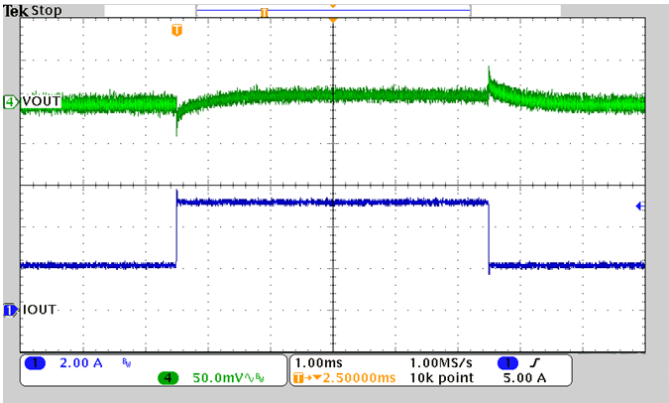


Fig. 24 Transient Response (V_{IN} = 12V, V_{OUT} = 5V)

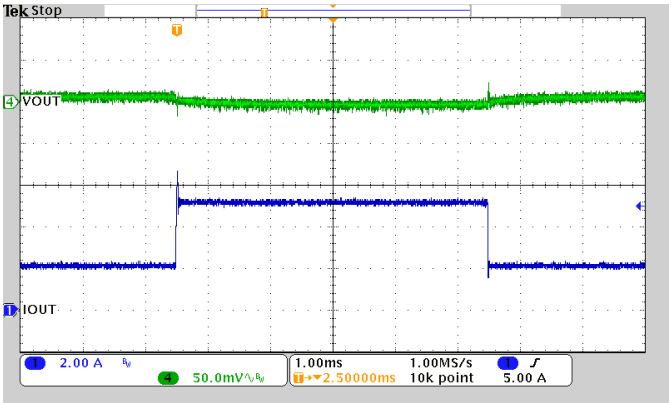


Fig. 25 Transient Response (V_{IN} = 12V, V_{OUT} = 0.6V)

The above figures show the typical output voltage waveform when the load current undergoes a step change between 2A and 5A (3A step), showing that the SPM1006 can achieve excellent dynamic performance.

Over Current Protection

For protection against over-current faults, SPM1006 will shut down when the load current is higher than the over-current protection (OCP) level. During an over-current condition, SPM1006 will operate in hiccup mode and will try to re-start automatically. The hiccup operation will continue until the over-current condition is removed or input power is removed.

Fig. 26 shows the output voltage and output current waveforms during over-current protection operation for SPM1006 set to 1.8V output. Performance at other output voltage settings is similar. When the over-current condition is removed, the output voltage recovers automatically to the nominal voltage, as shown in Fig. 27.

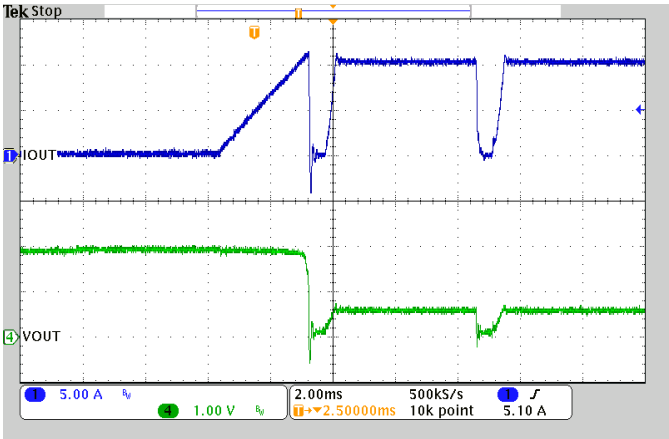


Fig. 26 Overcurrent protection (hiccup mode)

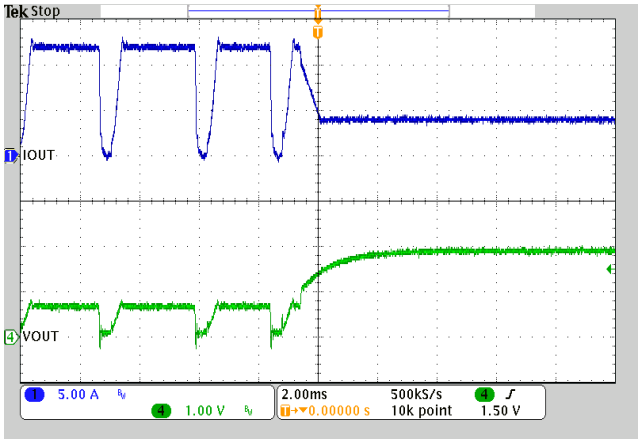


Fig. 27 Recovery from overcurrent

Input protection

In most applications the input power source provides current limiting (typically fold-back or hiccup mode) and as long as the average fault current is limited to approximately 10A or less, no further protection is required.

If the SPM1006 is powered from a battery or other high current source, it is recommended to include an external fuse (maximum 10A) in the input to the module. The SPM1006 includes full protection against output overcurrent or short-circuit, and the fuse will not operate under any output overload condition. For more information refer to PM_AN-2 “Input Protection”.

Thermal Considerations

The maximum continuous current rating depends on the ambient temperature, input voltage and output voltage as shown in Fig. 28, Fig. 29 and Fig. 30. Output current can exceed these values for short periods, as long as the average does not exceed the derating curve. The peak current duration is limited by the thermal time constant, typically in the order of 60 seconds in most applications.

The maximum rating is also influenced by the PCB layout; thermal performance can be improved by using more copper on the motherboard. The derating shown in these curves is measured using the Sumida Evaluation Module (EVM) layout. Derating also depends on airflow; these curves are based on data measured under natural convection (no forced air).

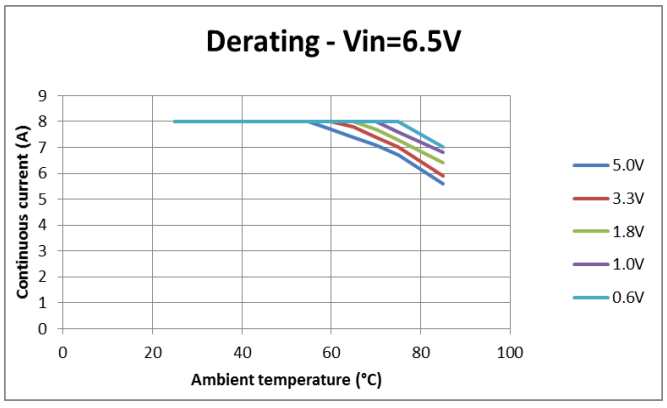


Fig. 28 Output current derating (6.5V input)

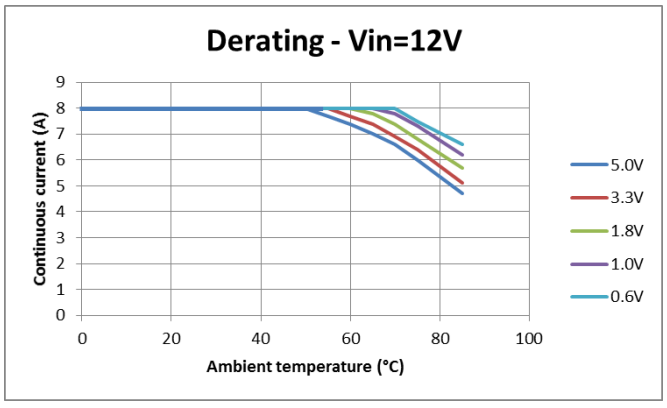


Fig. 29 Output current derating (12V input)

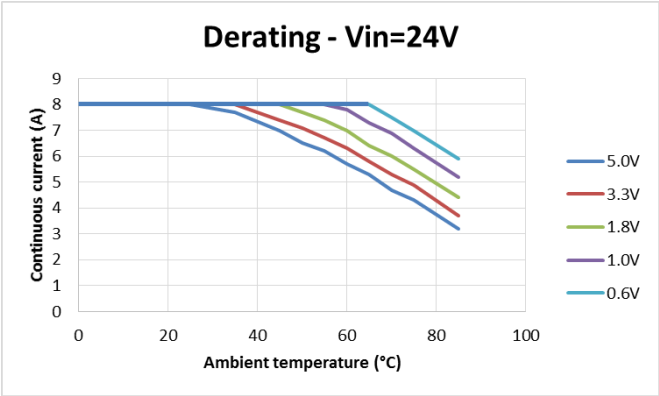


Fig. 30 Output current derating (24V input)

For more information refer to Application Note PM_AN-3 “SPM1006 Current Ratings”.

The absolute maximum operating junction temperature is 150°C and it is recommended to keep the operating temperature well below this value under worst-case conditions. Maximum recommended case temperature is 115°C, which corresponds to a junction temperature of approximately 125°C.

The thermal resistance from case to ambient (θ_{CA}) depends on the PCB layout as well as the amount of cooling airflow. When mounted on the EVM, θ_{CA} is approximately 15°C/watt in still air. Please refer to the EVM User Guide for EVM PCB layout information.

The SPM1006 implements an internal thermal shutdown to protect itself against over-temperature conditions. When the junction temperature of the power MOSFET is above 150°C, the power module stops operating to protect itself from thermal damage. When the MOSFET temperature reduces to approximately 135°C (with hysteresis of 15°C), SPM1006 will restart automatically.

Layout Considerations

To achieve optimal electrical and thermal performance, an optimized PCB layout is required. Some considerations for an optimized layout are:

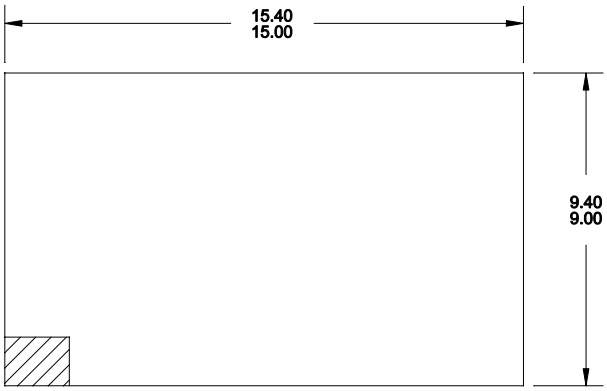
- Use large copper areas for power planes (PVIN, VOUT, and PGND) to minimize conduction loss and thermal stress;
- Place ceramic input and output capacitors close to the module pins to minimize high frequency noise;
- Locate additional output capacitors between the main ceramic capacitor and the load;
- Connect AGND plane and PGND plane at single point;
- Place resistors and capacitors connected to SENSE and VADJ pins as close as possible to their respective pins;
- Do not connect PHASE pin to other components;
- Use multiple vias to connect the power planes to internal layers.

Refer to SPM1006 Evaluation Module (EVM) User Manual for suggested PCB layout.

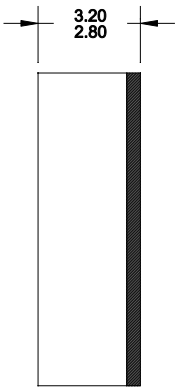
MECHANICAL DATA

Package Dimensions and PCB pads

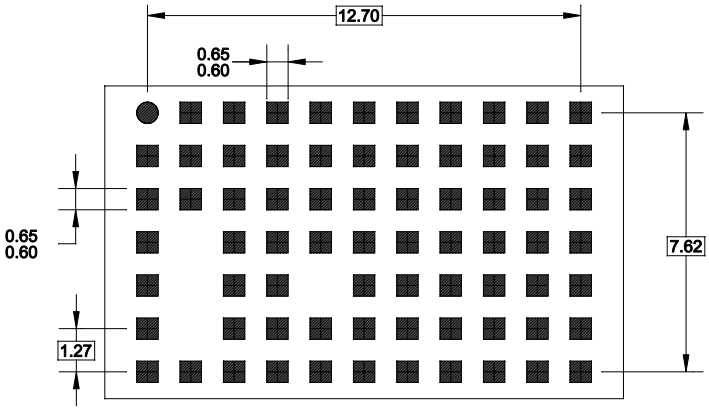
ALL DIMENSIONS IN MILLIMETERS



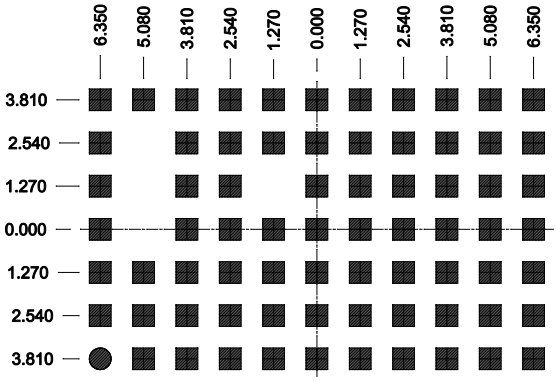
Package Top View



Package Side View



Package Bottom View



Suggested PCB Layout
Top View

Tape and Reel Packaging Information

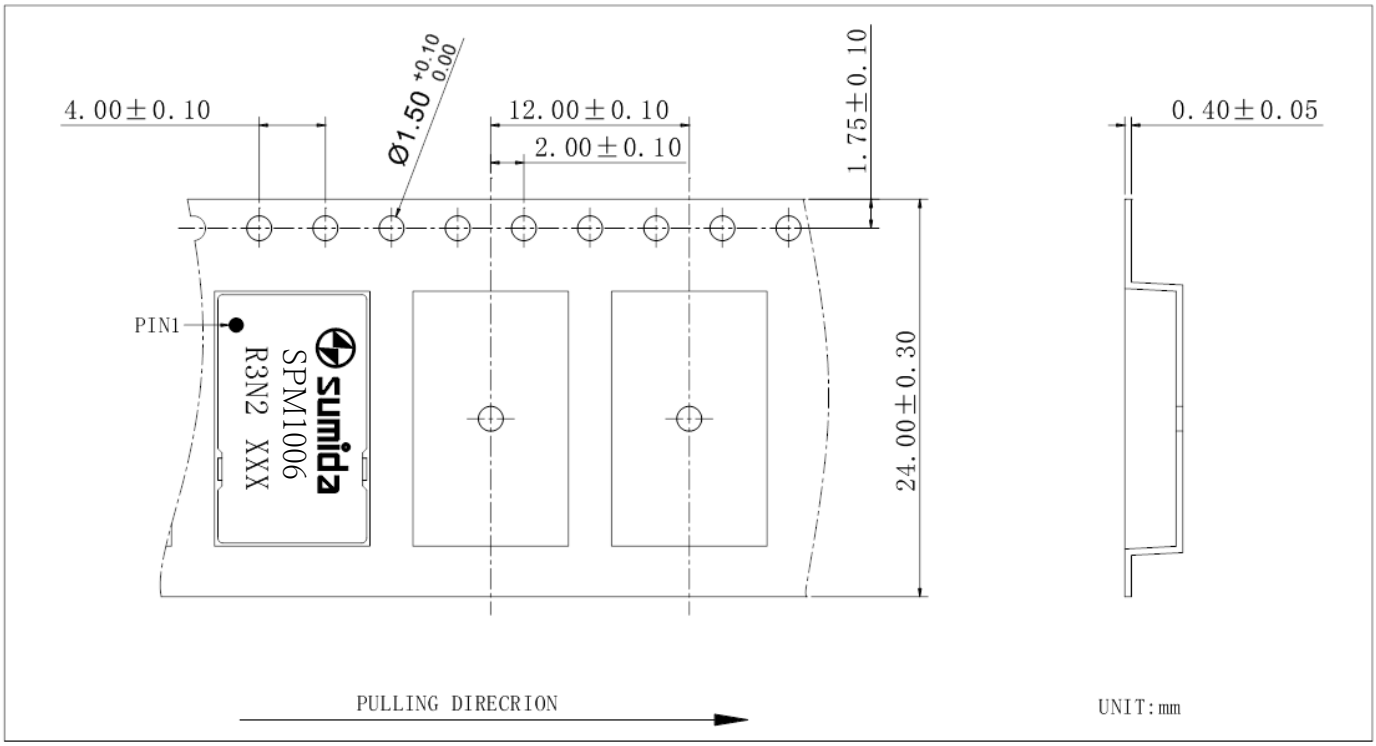


Fig. 31 Tape Dimensions and Loading Information

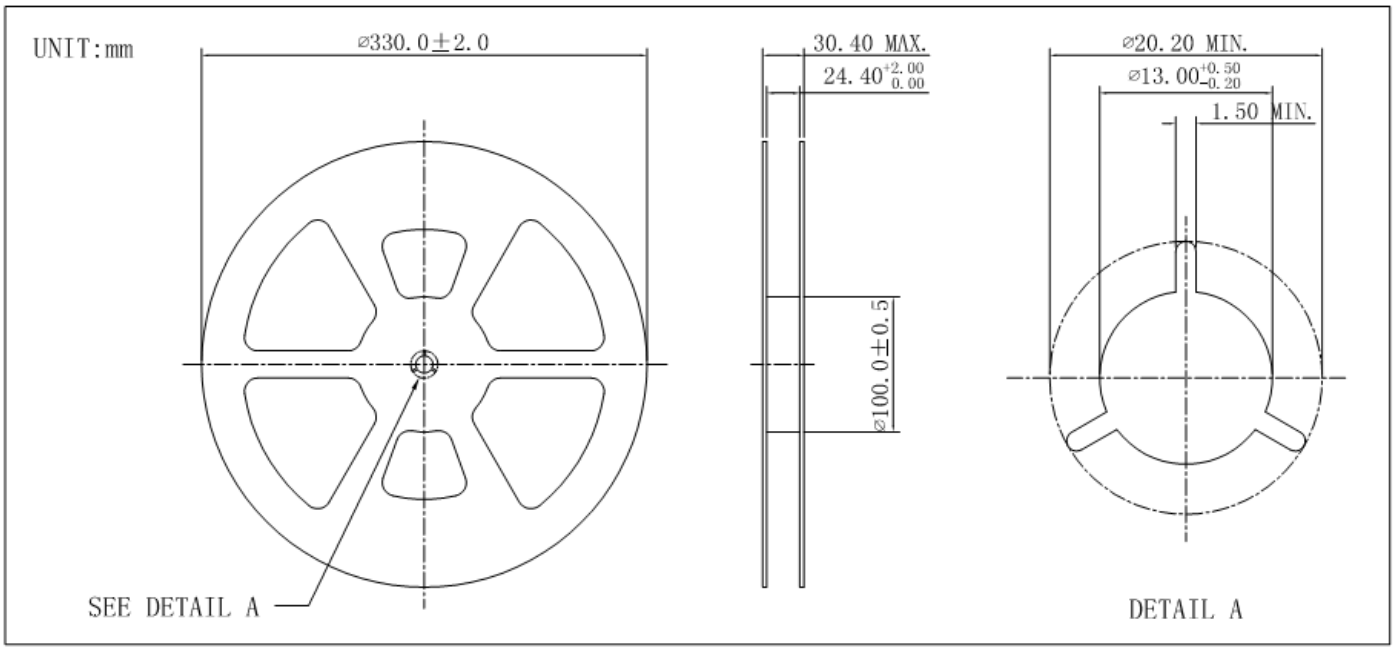


Fig. 32 Reel Dimensions

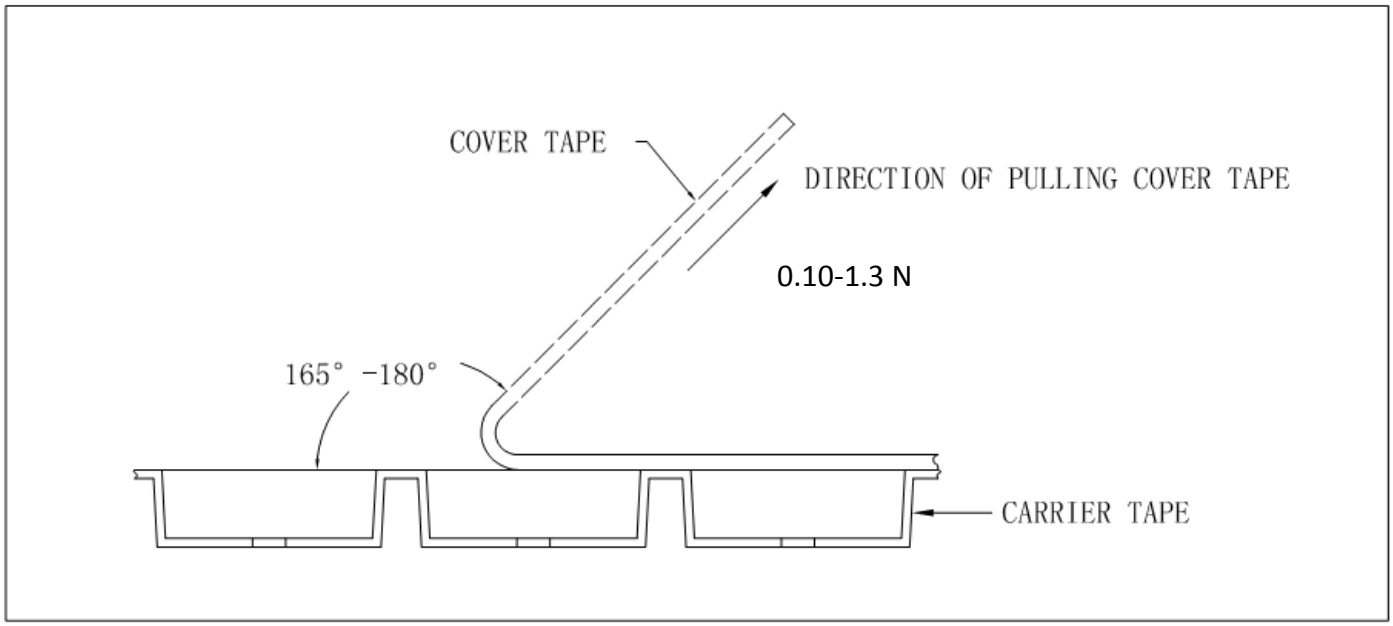


Fig. 33 Peel Speed and Strength of Cover Tape

Note:

1. The peel speed shall be approximately 300mm/min.
2. The peel force of the top cover tape shall be between 0.1N and 1.3N.

Storage and handling

Moisture barrier bag

The modules are packed in a reel, and then an aluminum foil moisture barrier bag is used to pack the reel in order to prevent moisture absorption. Silica gel is put into the aluminum moisture barrier bag as absorbent material.

Storage

SPM1006 is classified MSL level 3 according to JEDEC J-STD-033 and J-STD-020 standards, with a floor life of 168 hours after the outer bag is opened. Any unused SPM1006 modules should be resealed in the original moisture barrier bag as soon as possible. If the module's floor life exceeds 168 hours, the modules should be dehumidified before use by baking in an oven at 125°C/1% RH (e.g. hot nitrogen gas atmosphere) for 48 hours.

Handling precautions

1. Handle carefully to avoid unnecessary mechanical stress. Excessive external stress may cause damage.

2. Normal ESD handling procedures are recommended to be used whenever handling the module.

3. If cleaning the module is necessary, use isopropyl alcohol solution at normal room temperature. Avoid the use of other solvents.

Reflow soldering

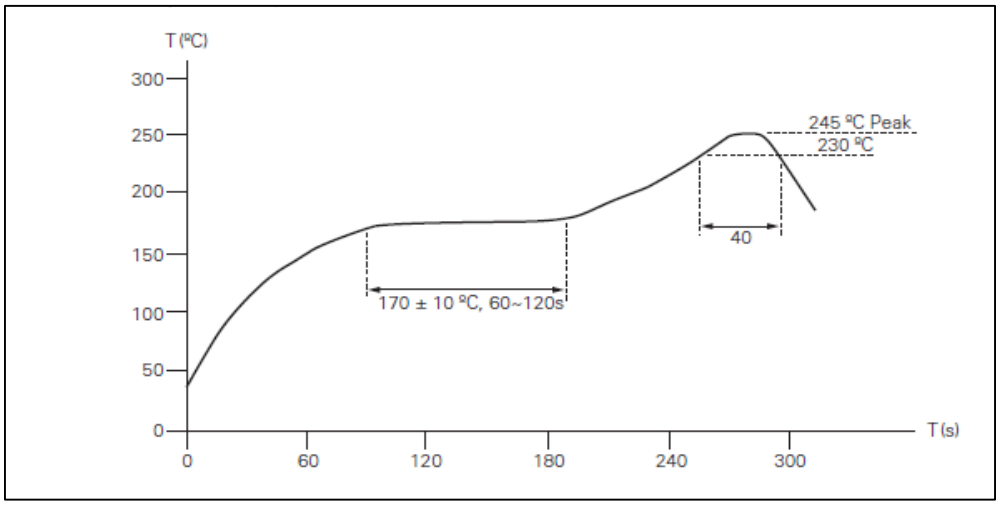


Fig. 34 Recommended Reflow Solder Profile (Lead-free)

Ordering Information

Output Voltage	Module Part Number	Pad Finish	Package Type	Temperature Range
Adjustable	SPM1006-ZC	Au (RoHS)	LGA	-40˚C to 85˚C
0.6V	SPM1006-0V6C			
0.8V	SPM1006-0V8C			
1.0V	SPM1006-1V0C			
1.2V	SPM1006-1V2C			
1.5V	SPM1006-1V5C			
1.8V	SPM1006-1V8C			
2.5V	SPM1006-2V5C			
3.3V	SPM1006-3V3C			
5.0V	SPM1006-5V0C			