EVALUATION KIT AVAILABLE

MAX16963

Dual 2.2MHz, Low-Voltage Step-Down DC-DC Converter

General Description

The MAX16963 is a high-efficiency, dual synchronous step-down converter that operates with a 2.7V to 5.5V input voltage range and provides a 0.8V to 3.6V output voltage range. The device delivers up to 1.5A of load current per output. The low input/output voltage range and the ability to provide high output currents make this device ideal for on-board point-of-load and postregulation applications. The device achieves ±3% output error over load, line, and temperature ranges.

The device features a 2.2MHz fixed-frequency PWM mode for better noise immunity and load transient response, and a skip mode for increased efficiency during light-load operation. The 2.2MHz frequency operation allows for an all-ceramic capacitor design and small-size external components. An optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions due to the switching frequency.

On-board low R_{DSON} switches help minimize efficiency losses at heavy loads and reduce critical/parasitic inductance, making the layout a much simpler task with respect to discrete solutions. Following a simple layout and footprint ensures first-pass success in new designs.

The device is offered in a factory-preset output voltage or adjustable output-voltage version (see the *Selector Guide* for options). Factory-preset output-voltage versions allow customers to achieve ±3% output-voltage accuracy without using external resistors, while the adjustable output-voltage version provides the flexibility to set the output voltage to any desired value between 0.8V and 3.6V using an external resistive divider.

Additional features include 8ms fixed soft-start, 16ms fixed power-good delay, overcurrent, and overtemperature protections.

The MAX16963 is available in thermally enhanced 16-pin TSSOP-EP and 4mm x 4mm, 16-pin TQFN-EP packages, and is specified for operation over the -40°C to +125°C automotive temperature range.

Applications

Automotive Postregulation

Industrial/Military

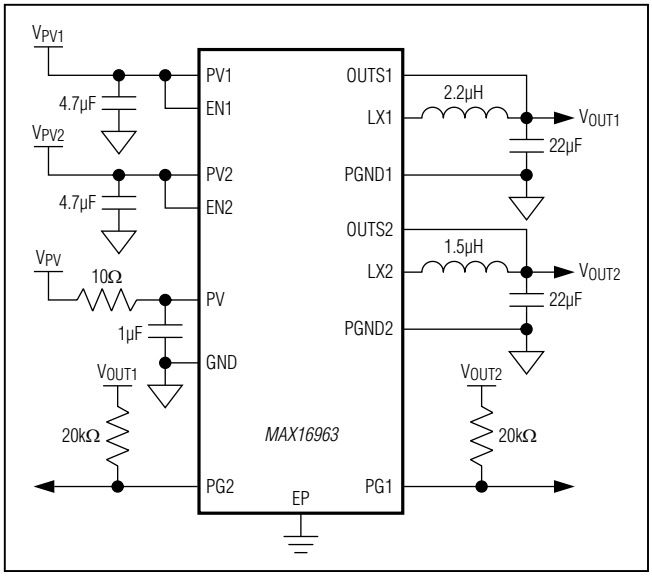
Point-of-Load Applications

Benefits and Features

- **Small Size Components**
  - ✧ **Dual 2.2MHz DC-DC Converter**
- **Ideal for Point-of-Load Applications**
  - ✧ **Up to 1.5A Output Current**
  - ✧ **Adjustable Output Voltage: 0.8V to 3.6V**
  - ✧ **2.7V to 5.5V Operating Supply voltage**
- **High Efficiency at Light Load**
  - ✧ **Skip Mode with 36µA Quiescent Current**
- **Low Electromagnetic Emission**
  - ✧ **Programmable SYNC I/O Pin**
  - ✧ **Spread Spectrum**
- **Low Power Mode Saves Energy**
  - ✧ **Independent Enable Inputs**
- **Output Rail Monitoring Helps Prevent System Failure**
  - ✧ **Open-Drain Power-Good Output**
- **Limits Inrush Current During Startup**
  - ✧ **Built-In Soft-Start Timer**
- **Overtemperature and Short-Circuit Protections**
- **4mm x 4mm, 16-Pin TQFN and 16-Pin TSSOP Packages**
- **-40°C to 125°C Operating Temperature Range**

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6487; Rev 5; 7/15

ABSOLUTE MAXIMUM RATINGS

PV, PV1, PV2 to GND ..... -0.3V to +6V
EN1, EN2, PG1, PG2 to GND ..... -0.3V to +6V
LX_ Current ..... ±1.6 (Note 1)
PGND1 and PGND2 to GND ..... -0.3V to +0.3V
PV to PV1 and PV2 ..... -0.3V to +0.3V
LX1 and LX2 Continuous RMS Current 1A
All Other Pins Voltages to GND .. (V_{PV} + 0.3V) to (V_{GND} - 0.3V)
Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 25mW/°C above +70°C) 2000mW*
TSSOP (derate 26.1mW/°C above +70°C) 2088.8mW*
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

**As per JEDEC51 Standard (multilayer board).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: LX_ has internal clamp diodes for PGND_ and PV_. Applications that forward bias these diodes should take care not to exceed the IC's package power-dissipation limits.

PACKAGE THERMAL CHARACTERISTICS (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 40°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 6°C/W

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 38.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 3°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{PV} = V_{PV1} = V_{PV2} = 5V, $V_{EN\_}$ = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{PV}	Normal operation	2.7		5.5	V
Supply Current	I_{PV}	No load, V_{PWM} = 0V	16	36	60	µA
Shutdown Supply Current	I_{SHDN}	V_{EN1} = V_{EN2} = 0V, T_A = +25°C		1	5	µA
Undervoltage Lockout Threshold Low	V_{UVLO_L}		2.37			V
Undervoltage Lockout Threshold High	V_{UVLO_H}				2.6	V
Undervoltage Lockout Hysteresis				0.07		V
SYNCHRONOUS STEP-DOWN DC-DC CONVERTER 1						
FB Regulation Voltage	V_{OUTS1}			800		mV
Feedback Set-Point Accuracy	V_{OUTS1}	I_{LOAD} = 4% to 100%	-3	0	+3	%
		I_{LOAD} = 0%	-0.5	+2	+3	%
pMOS On-Resistance	R_{DSON_P1}	V_{PV1} = 5V, I_{LX1} = 0.4A		90	148	mΩ
nMOS On-Resistance	R_{DSON_N1}	V_{PV1} = 5V, I_{LX1} = 0.8A		68	128	mΩ
Maximum pMOS Current-Limit Threshold	I_{LIMP1}		1.95	2.35	3.15	A

ELECTRICAL CHARACTERISTICS (continued)

(V_{PV} = V_{PV1} = V_{PV2} = 5V, $V_{EN\_}$ = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Output Current	I_{OUT1}	(V_{OUT1} + 0.5V ≤ V_{PV1} ≤ 5.5V) (Note 4)		1.5			A
OUTS1 Bias Current	I_{B_OUTS1}	Fixed output-voltage variants		-1		+1	µA
		Adjustable output variants		-1		+1	
LX1 Leakage Current	I_{LX1_LEAK}	V_{PV1} = 6V, LX1 = PGND1 or PV1	T_A = +25°C	-1		+1	µA
			T_A = +125°C	-5		+5	
Minimum On-Time	t_{ON_MIN}				60		ns
LX1 Discharge Resistance	R_{LX1}	V_{EN1} = 0V, through the OUTS_ pin		15	24	55	Ω
Maximum Short-Circuit Current						3.9	A
SYNCHRONOUS STEP-DOWN DC-DC CONVERTER 2							
FB Regulation Voltage	V_{OUTS2}				800		mV
Feedback Set-Point Accuracy	V_{OUTS2}	I_{LOAD} = 4% to 100%		-3	0	+3	%
		I_{LOAD} = 0%		+1	+2	+3	
pMOS On-Resistance	R_{DSON_P2}	V_{PV2} = 5V, I_{LX2} = 0.4A			90	148	mΩ
nMOS On-Resistance	R_{DSON_N2}	V_{PV2} = 5V, I_{LX2} = 0.8A			68	128	mΩ
Maximum pMOS Current-Limit Threshold	I_{LIMP2}			1.95	2.55	3.15	A
Maximum Output Current	I_{OUT2}	(V_{OUT2} + 0.5V ≤ V_{IN2} ≤ 5.5V) (Note 4)		1.5			A
OUTS2 Bias Current	I_{B_OUTS2}	Fixed output-voltage variants		1	2	5	µA
		Adjustable output variants				1	
LX2 Leakage Current	I_{LX2_LEAK}	V_{PV2} = 6V, LX2 = PGND2 or PV2	T_A = +25°C	-1		+1	µA
			T_A = +125°C	-5		+5	
Minimum On-Time	t_{ON_MIN}				60		ns
LX2 Discharge Resistance	R_{LX2}	V_{EN2} = 0V, through the OUTS_ pin		15	24	55	Ω
Maximum Short-Circuit Current						3.9	A
OSCILLATOR							
Oscillator Frequency	f_{SW}			2.0	2.2	2.4	MHz
Spread Spectrum	Δf/f	Spread spectrum enabled			+6		%
SYNC Input Frequency Range	f_{SYNC}	50% duty cycle (Note 5)		1.7		2.4	MHz
THERMAL OVERLOAD							
Thermal Shutdown Threshold					165		°C
Thermal Shutdown Hysteresis					15		°C
POWER-GOOD OUTPUTS (PG1, PG2)							
PG_ Overvoltage Threshold	PG_{OVTH}	Percentage of nominal output		106	110	114	%
PG_ Undervoltage Threshold	PG_{UVTH}	Percentage of nominal output		89.5	92	94	%
Active Timeout Period					16		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{PV} = V_{PV1} = V_{PV2} = 5V, $V_{EN\_}$ = 5V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

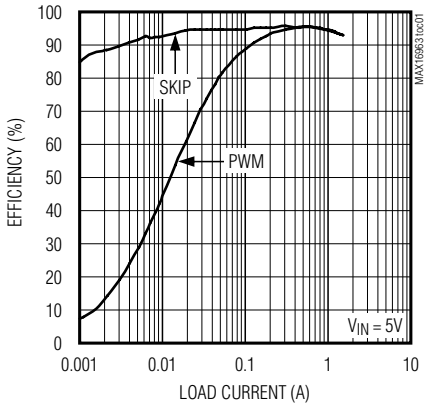
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage/Overvoltage Propagation Delay				28		µs
Output High Leakage Current		T_A = +25°C			0.2	µA
PG1 Output Low Voltage		2.6V ≤ V_{PV1} ≤ 5.5V, I_{SINK} = 3mA			0.4	V
		V_{PV1} = 1.2V, I_{SINK} = 100µA			0.4	
PG2 Output Low Voltage		2.6V ≤ V_{PV2} ≤ 5.5V, I_{SINK} = 3mA			0.4	V
		V_{PV2} = 1.2V, I_{SINK} = 100µA			0.4	
ENABLE INPUTS (EN1, EN2)						
Input Voltage High	V_{INH}	Input rising	2.4	1.7	2.4	V
Input Voltage Low	V_{INL}	Input falling	0.5	0.85	0.5	V
Input Hysteresis				0.85		V
Input Current		$V_{EN\_}$ = high	0.1	1.0	2	µA
Pulldown Resistor		$V_{EN\_}$ = low	50	100	200	kΩ
DIGITAL INPUTS (SYNC, PWM)						
Input Voltage High	V_{INH}		1.8			V
Input Voltage Low	V_{INL}				0.4	V
Input Voltage Hysteresis				50		mV
Pulldown Resistor			50	100	200	kΩ
DIGITAL OUTPUT (SYNC)						
SYNC Output Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
SYNC Output Voltage High	V_{OH}	$V_{PV\_}$ = 5V, I_{SOURCE} = 3mA	4.2			V

Note 3: All limits are 100% production tested at +25°C. Limits over temperature are guaranteed by design.
Note 4: Calculated value based on an assumed inductor ripple of 30%.
Note 5: For SYNC frequency outside (1.7, 2.4)MHz, contact the factory.

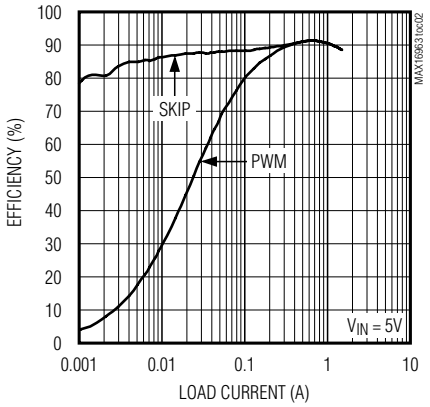
Typical Operating Characteristics

(V_{PV} = V_{PV1} = 5V, V_{EN1} = V_{EN2} = 5V, V_{OUT1} = 3.3V, V_{OUT2} = 1.8V, T_A = +25°C, unless otherwise noted.)

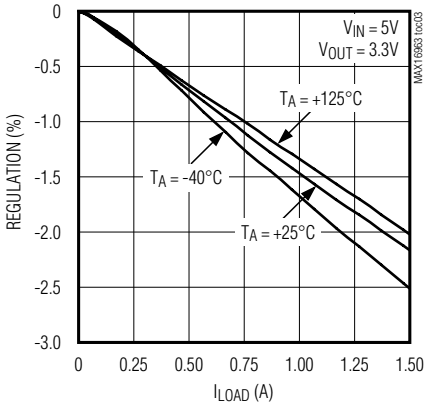
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 3.3V)



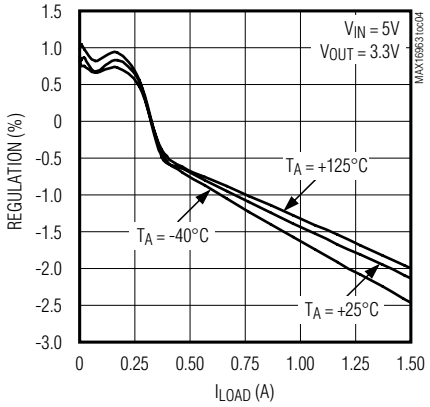
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.8V)



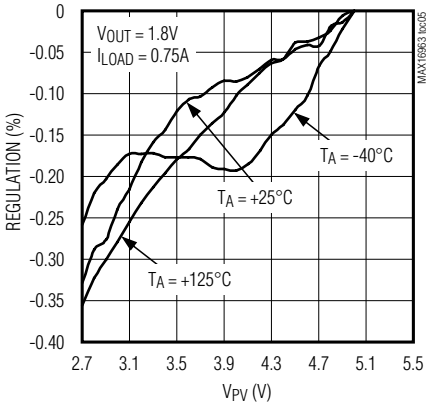
V_{OUT} LOAD REGULATION (PWM)



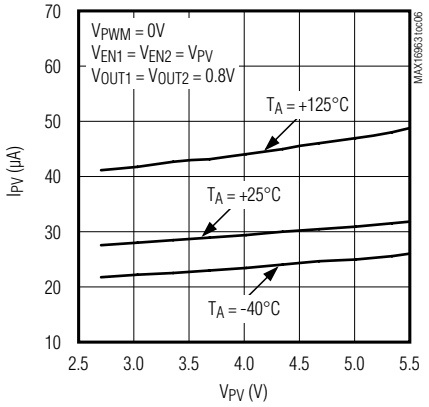
V_{OUT1} LOAD REGULATION (SKIP)



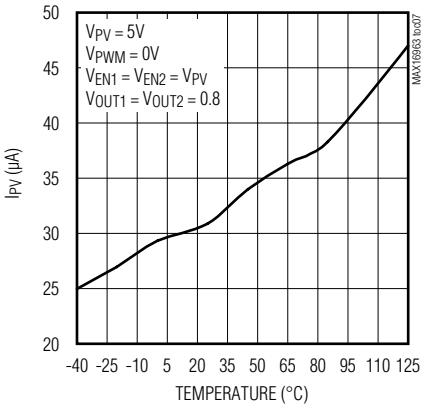
V_{OUT} LINE REGULATION (PWM)



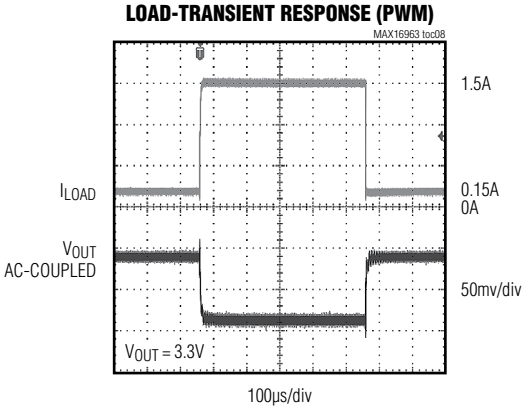
I_{PV} vs. V_{PV} (SKIP)



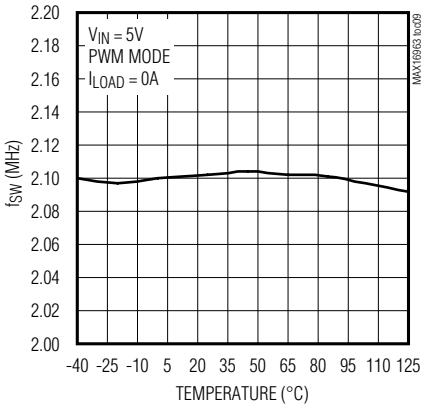
I_{PV} vs. TEMPERATURE (SKIP)



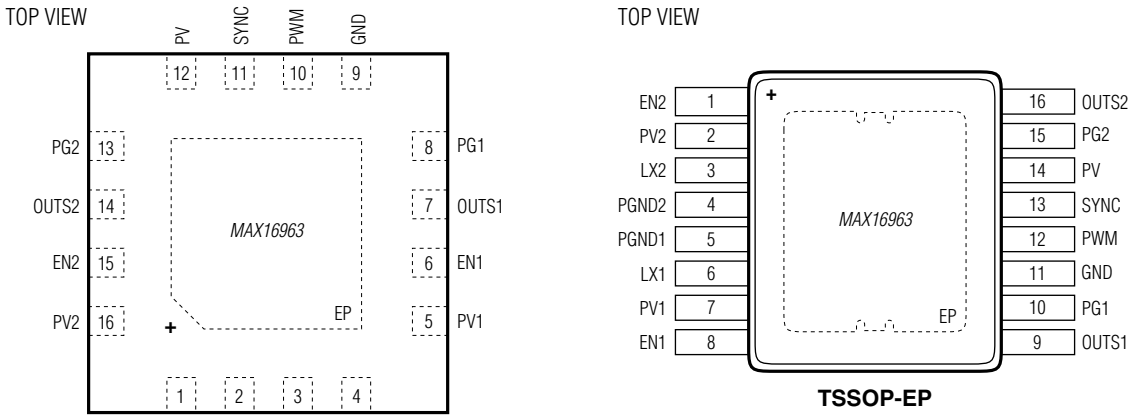
LOAD-TRANSIENT RESPONSE (PWM)



f_{SW} vs. TEMPERATURE



Pin Configurations



TQFN-EP
(4mm x 4mm)

TSSOP-EP

Pin Descriptions

PIN		NAME	FUNCTION
TQFN	TSSOP		
1	3	LX2	Converter #2 Switching Node. LX2 is high impedance when converter #2 is off.
2	4	PGND2	Converter #2 Power Ground
3	5	PGND1	Converter #1 Power Ground
4	6	LX1	Converter #1 Switching Node. LX1 is high impedance when converter #1 is off.
5	7	PV1	Converter #1 Input Supply. Bypass PV1 with at least a 4.7µF ceramic capacitor to PGND1.
6	8	EN1	Converter #1 Enable Input. Drive EN1 high to enable converter #1. Drive EN1 low to disable converter #1.
7	9	OUTS1	Converter #1 Feedback Input (Adjustable Output Option Only). Connect an external resistive divider from V_{OUT1} to OUTS1 and GND to set the output voltage.
8	10	PG1	OUT1 Power-Good Output. Open-drain output. PG1 asserts when V_{OUT1} drops by 8%. Connect to a 10kΩ pullup resistor.
9	11	GND	Ground
10	12	PWM	PWM Control Input. Drive PWM high to put converters in forced PWM mode. Drive PWM low to put converters in skip mode.
11	13	SYNC	Factory-Set Sync Input or Output. As an input, SYNC accepts a 1.7MHz to 2.5HMz external signal. As an output, SYNC outputs a 90° phase-shifted signal with respect to internal oscillator.

Pin Descriptions (continued)

PIN		NAME	FUNCTION
TQFN	TSSOP		
12	14	PV	Device Supply Voltage Input. Bypass with at least a 1µF ceramic capacitor to GND. In addition, connect a 10Ω decoupling resistor between PV and the bypass capacitor.
13	15	PG2	OUT2 Power-Good Output. Open-drain output. PG2 asserts when V_{OUT2} drops by 8%. Connect to a 10kΩ pullup resistor.
14	16	OUTS2	Converter #2 Feedback Input (Adjustable Output Option Only). Connect an external resistive divider from V_{OUT2} to OUTS2 and GND to set the output voltage.
15	1	EN2	Converter #2 Enable Input. Drive EN2 high to enable converter #2. Drive EN2 low to disable converter #2.
16	2	PV2	Converter #2 Input Supply. Bypass PV2 with at least a 4.7µF ceramic capacitor to PGND2.
—	—	EP	Exposed Pad. Connect EP to a large-area contiguous copper ground plane for effective power dissipation. Do not use as the only IC ground connection. EP must be connected to GND.

Detailed Description

The MAX16963 is a high-efficiency, dual synchronous step-down converter that operates with a 2.7V to 5.5V input voltage range and provides a 0.8V to 3.6V output voltage range. The MAX16963 delivers up to 1.5A of load current per output and achieves ±3% output error over load, line, and temperature ranges.

The device features a PWM input that, when set to logic-high, forces the MAX16963 into a fixed-frequency, 2.2MHz PWM mode. A logic-low at the PWM input enables the device to enter a low-power pulse frequency modulation mode (PFM) under light-load conditions. An optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions due to the switching frequency and a factory programmable synchronization I/O (SYNC) allows better noise immunity.

On-board low R_{DSON} switches help minimize efficiency losses at heavy loads and reduce critical/parasitic inductance, making the layout a much simpler task with respect to discrete solutions. Following a simple layout and footprint ensures first-pass success in new designs.

The device is offered in factory-preset output voltages to allow customers to achieve ±3% output-voltage accuracy without using expensive ±1% resistors. In addition, the adjustable output-voltage versions can be set to any desired values between 0.8V to 3.6V using an external resistive divider. See the *Selector Guide* for available options.

Additional features include 8ms fixed soft-start, 16ms fixed power-good output, overcurrent, and overtemperature protections. See Figure 1.

Power-Good Output

The MAX16963 features an open-drain power-good output that asserts when the output voltage drops 8% below the regulated voltage. PG_ remains asserted for a fixed 16ms timeout period after the output rises up to its regulated voltage. Connect PG_ to OUTS_ with a 10kΩ resistor.

Soft-Start

The MAX16963 includes an 8ms fixed soft-start time. Soft-start time limits startup inrush current by forcing the output voltage to ramp up towards its regulation point.

Spread-Spectrum Option

The MAX16963 featuring spread-spectrum (SS) operation varies the internal operating frequency up by SS = 6% relative to the internally generated operating frequency of 2.2MHz (typ). This function does not apply to externally applied oscillation frequency. The internal oscillator is frequency modulated with a 6% frequency deviation. See the *Selector Guide* for available options.

Synchronization (SYNC)

SYNC is a factory-programmable I/O. See the *Selector Guide* for available options. When SYNC is configured as an input, a logic-high on PWM enables SYNC to accept signal frequency in the range of 1.7MHz < f_{SYNC} < 2.5MHz. When SYNC is configured as an output, a logic-high on PWM enables SYNC to output a 90° phase-shifted signal with respect to internal oscillator.

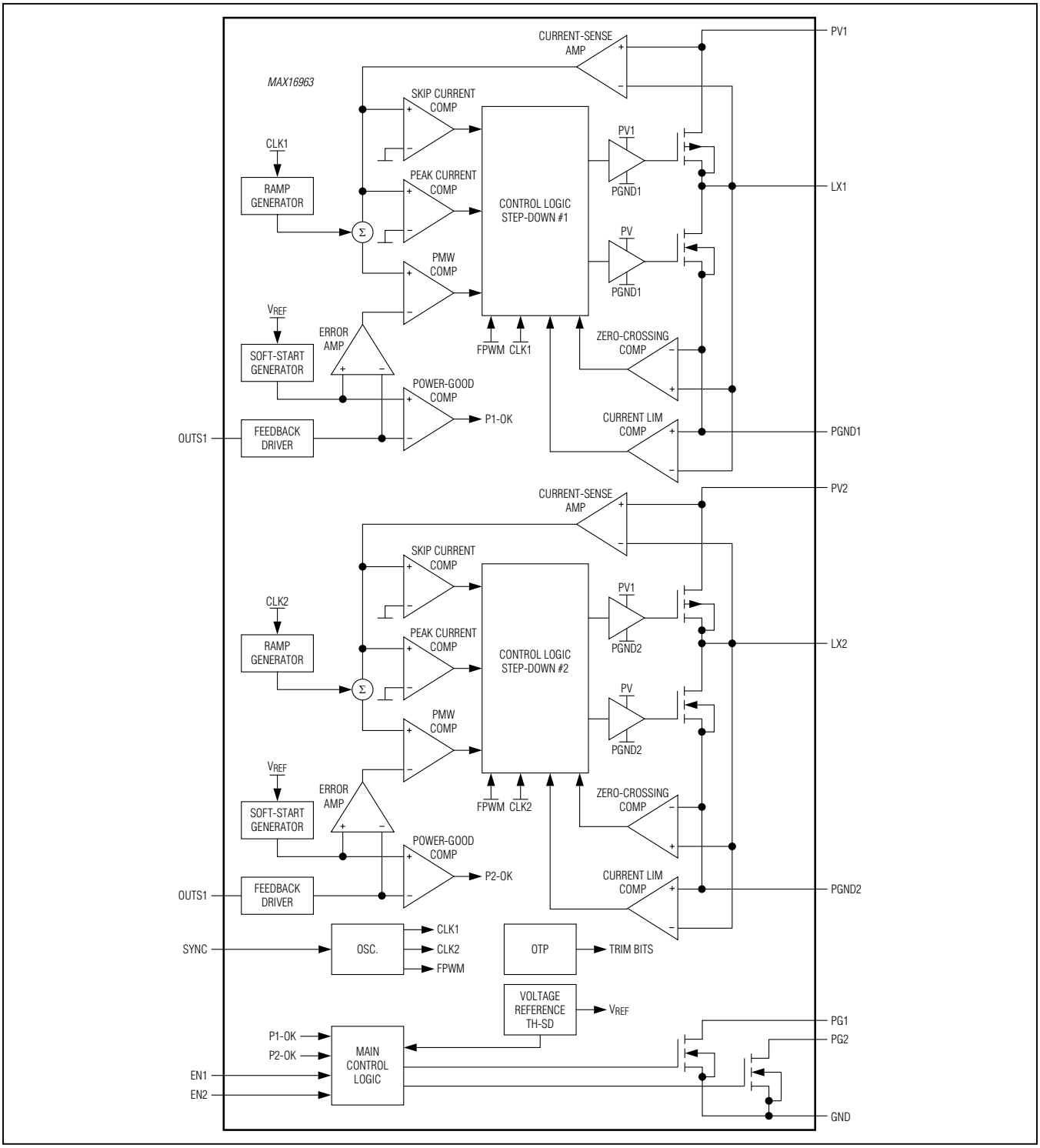


Figure 1. Internal Block Diagram

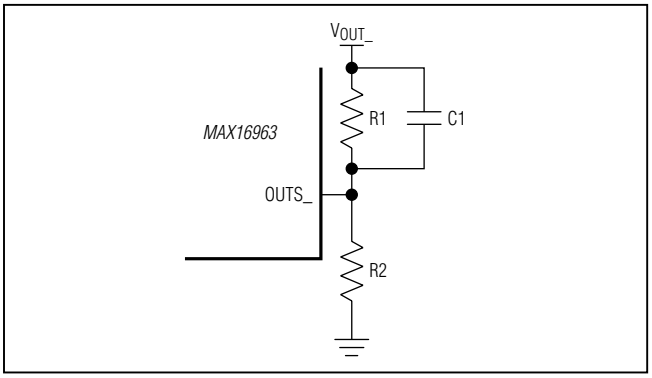


Figure 2. Adjustable Output Voltage Setting

Current-Limit/Short-Circuit Protection

The MAX16963 features current limit that protects the device against short-circuit and overload conditions at an output. In the event of a short-circuit or overload condition at an output, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET and the inductor current ramps down. The converter allows the high-side MOSFET to turn on only when the inductor current ramps down to the low-side MOSFET's current threshold. This cycle repeats until the short or overload condition is removed.

FPWM/Skip Modes

The MAX16963 features an input (PWM) that puts the converter either in skip mode for forced PWM (FPWM) mode of operation. See the *Pin Descriptions* for mode detail. In FPWM mode, the converter switches at a constant frequency with variable on-time. In skip mode, the converter's switching frequency is load-dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the FPWM mode. Skip mode helps improve efficiency in light-load applications by allowing the converters to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off as often as is the case in the FPWM mode. Consequently, the gate charge and switching losses are much lower in skip mode.

Overtemperature Protection

Thermal overload protection limits the total power dissipation in the MAX16963. When the junction temperature exceeds 165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

Applications Information

Adjustable Output-Voltage Option

The MAX16963 has an adjustable output voltage (see the *Selector Guide* for options) that allows the customer to set the outputs to any voltage between 0.8V and 3.6V. Connect a resistive divider from output ($V_{OUT\_}$) to OUTS_ to GND to set the output voltage (Figure 2). Select R2 (OUTS_ to GND resistor) less than or equal to 100kΩ. Calculate R1 ($V_{OUT\_}$ to OUTS_ resistor) with the following equation:

$$R1 = R2\left[\left(\frac{V_{OUT\_}}{V_{OUTS\_}}\right) - 1\right]$$

$$\text{where } \frac{R1 \times R2}{R1 + R2} \le 7.5k\Omega$$

where $V_{OUTS\_}$ = 800mV (see the *Electrical Characteristics* table).

The external feedback resistive divider must be frequency compensated for proper operation. Place a capacitor across each resistor in the resistive divider network. Use the following equation to determine the value of the capacitors:

$$C1 = 10pF\left(\frac{R2}{R1}\right)$$

Connect OUTS_ to $V_{OUT\_}$ for the fixed output-voltage versions.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX16963: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). Use the following formulas to determine the minimum inductor value:

$$L_{MIN1} = \left[(V_{IN} - V_{OUT\_}) \times \left(\frac{V_{OUT\_}}{V_{IN}}\right) \times \left(\frac{3}{f_{OP} \times V_{REF} \times G_{CS}}\right)\right]$$

where f_{OP} is the operating frequency; this value is 2.2MHz, unless externally synchronized to a different frequency; V_{REF} is the reference voltage equal to 1.25V; G_{CS} is the internal current-sense conductance equal to 0.8.

The next equation ensures that the inductor current down slope is less than the internal slope compensation. For

Table 1. Inductor Values vs. (V_{IN} - V_{OUT})

V_{IN} - V_{OUT} (V)	5.5 to 3.3	5.5 to 2.5	5.5 to 1.5	3.0 to 0.8
INDUCTOR (µH), I_{LOAD} = 1.5A	1.5	1.5	1.0	0.68

this to be the case, the following equation needs to be satisfied:

$$-m \geq \frac{m2}{2}$$

where m2 is the inductor current down slope:

$$\frac{V_{OUT}}{L}$$

and -m is the slope compensation:

$$\frac{0.8 \times V_{REF}}{\mu s \times G_{CS}}$$

Solving for L:

$$L_{MIN2} = V_{OUT} \times \frac{\mu s}{1.6 \times V_{REF} \times G_{CS}}$$

The equation that provides the bigger inductor value must be chosen for proper operation.

$$L_{MIN} = \max(L_{MIN1}, L_{MIN2})$$

Then:

$$L_{MAX} = 2 \times L_{MIN}$$

The maximum inductor value must not exceed the calculated value from the above formula. This ensures that the current feedback loop receives the correct amount of current ripple for proper operation.

Table 1 lists some of the inductor values for 1.5A output current and several output voltages.

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT\_}(V_{PV\_} - V_{OUT\_})}}{V_{PV\_}}$$

I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{PV\_} = 2V_{OUT\_}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input-voltage ripple is composed of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high-ripple current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT\_} + \frac{\Delta I_L}{2}}$$

where:

$$\Delta I_L = \frac{(V_{PV\_} - V_{OUT\_}) \times V_{OUT\_}}{V_{PV\_} \times f_{SW} \times L}$$

and:

$$C_{IN} = \frac{I_{OUT\_} \times D(1-D)}{\Delta V_Q \times f_{SW}} \text{ and } D = \frac{V_{OUT\_}}{V_{PV\_}}$$

where $I_{OUT\_}$ is the maximum output current, and D is the duty cycle.

Output Capacitor

The minimum capacitor required depends on output voltage, maximum device current capability, and the error-amplifier voltage gain. Use the following formula to determine the required output capacitor value:

$$C_{OUT(MIN)} = \frac{V_{REF} \times G_{EAMP}}{2\pi \times f_{CO} \times V_{OUT} \times R_{CS}}$$

$$= \frac{0.8V \times 31.7}{2\pi \times 210kHz \times V_{OUT} \times 378m\Omega}$$

where f_{CO} is the target crossover frequency equal to 210kHz, G_{EAMP} is the error-amplifier voltage gain equal to 31.7V/V, and R_{CS} is 378mΩ.

PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise immunity and power dissipation. Follow these guidelines for good PCB layout:

1) Use a large contiguous copper plane under the MAX16963 package. Ensure that all heat-dissipating components have adequate cooling. The bottom pad of the MAX16963 must be soldered down to this copper plane for effective heat dissipation and maximizing the full power out of the MAX16963. Use multiple vias or a single large via in this plane for heat dissipation.
2) Isolate the power components and high current path from the sensitive analog circuitry. This is essential to prevent any noise coupling into the analog signals.
3) Add small footprint blocking capacitors with low self-resonance frequency close to PV1, PV2, and PV.
4) Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. The high current path composed of input capacitors at PV1 and PV2, inductor, and the output capacitor should be as short as possible.
5) Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
6) OUTS_ are sensitive to noise for devices with external feedback option. The resistive network, R1, R2, and C1 must be placed close to OUTS_ and far away from the LX_ node and high switching current paths. The ground node of R2 must be close to GND.
7) The ground connection for the analog and power section should be close to the IC. This keeps the ground current loops to a minimum. In cases where only one ground is used enough isolation between analog return signals and high power signals must be maintained.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1644+4	21-0139	90-0070
16 TSSOP-EP	U16E+3	21-0108	90-0120

Selector Guide

ROOT PART	PACKAGE SUFFIX	OPTION SUFFIX	I_{LOAD} PER OUTPUT (A)	OUTPUT VOLTAGE	SPREAD SPECTRUM	SYNC IN/ OUT	POWER-GOOD DELAY (ms)
MAX16963	RAUE	A/V+	1.5/1.5	Ext. Adj.	Disabled	In	16
MAX16963	SAUE	A/V+	1.5/1.5	Ext. Adj.	Enabled	In	16
MAX16963	RATE	A/V+	1.5/1.5	Ext. Adj.	Disabled	In	16
MAX16963	SATE	A/V+	1.5/1.5	Ext. Adj.	Enabled	In	16
MAX16963	SATE	C/V+	1.5/1.5	Ext. Adj.	Enabled	Out	16
MAX16963	SATE	D/V+	1.5/1.5	Ext. Adj.	Enabled	In	8
MAX16963	SATE	F/V+	1.5/1.5	Ext. Adj.	Enabled	Out	8

Note: *Contact the factory for variants with different output voltage, spread spectrum, and power-good delay time settings.*

Ordering Information

PART	TEMP RANGE	LOAD CURRENT CAPABILITY PER OUTPUT (A)	PIN-PACKAGE
MAX16963_ATE_/V+	-40°C to +125°C	1.5/1.5	16 TQFN-EP*
MAX16963_AUE_/V+	-40°C to +125°C	1.5/1.5	16 TSSOP-EP*

/V denotes an automotive qualified part.
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/12	Initial release	—
1	9/13	Updated input voltage high min spec and input voltage low max spec, Figure 2, equation, step 6 in the *PCB Layout Guidelines* section, and the *Ordering Information*	4, 9, 11, 12
2	10/13	Updated *Ordering Information* and added MAX16963SATE/V+ and PG timing column to *Selector Guide*	12
3	2/14	Added FB regulation voltage to the *Electrical Characteristics* table, corrected V_{OUT} mismatch in the *Typical Operating Characteristic* section, updated *Inductor Selection* and *Output Capacitor* sections, updated Table 2, updated note in the *Selector Guide*	2, 3, 5, 9, 10, 12
4	4/14	Updated $V_{PV\_}$ condition for PG_ output low voltage specification	4
5	7/15	Added formula to equation in the *Setting the Output Voltage* section, replaced the *Output Capacitor* section, and deleted Table 2	9–11