3.0W Stereo & 3D Enhancement Class D Audio Power Amplifier (SOP16)

FEATURES

- 3.0W stereo into 4Ω from 5.5V power supply at THD+N = 10%.
- 2.5V~5.5V Power supply.
- Low shutdown Current.
- Low Quiescent Current.
- Minimum external components.
- No output filter required for inductive loads.
- Short-Circuit and Thermal Protection. (Short to GND, VDD. and output to output)
- Low noise during device turn-on.
- Support 3D enhance function.
- Lead free and green package available. (RoHS Compliant)
- Package : 16-pin 150 mil SOP
  16-pin 5x5 QFN

GENERAL DESCRIPTION

The LY8221 is a 3.0W stereo, high efficiency class D audio power amplifier. It is a low noise, filterless, PWM architecture eliminates the output filter, reducing external component count, BOM (system) cost, and simplify design.

The LY8221 features a low power consumption in shutdown mode and thermal shutdown protection. It also utilizes circuitry to reduce low noise during device turn-on.

The outputs are also fully protected against short to GND, VDD, and output-to-output. The short-circuit protection and thermal protection include an auto-recovery feature.

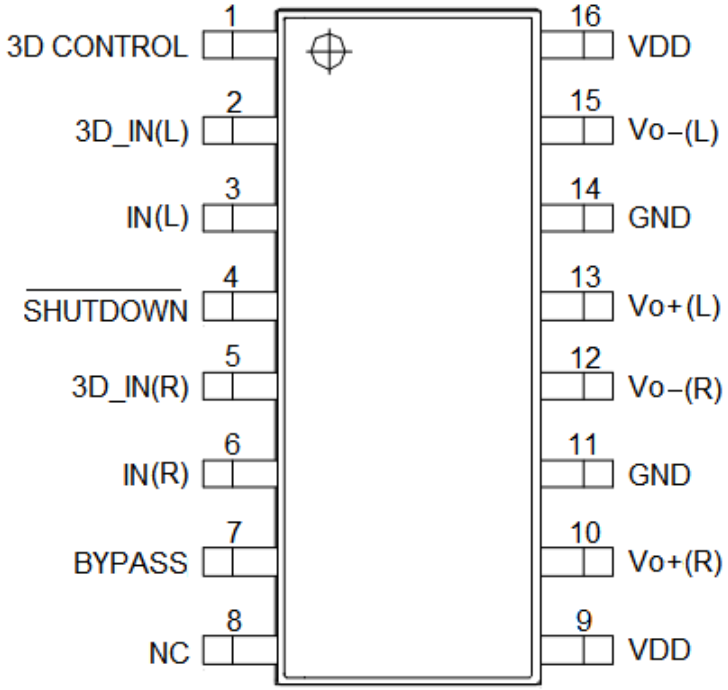
LY8221 support the 3D function. When selectable the 3D enhance mode function provides enhanced stereo imaging.

APPLICATION

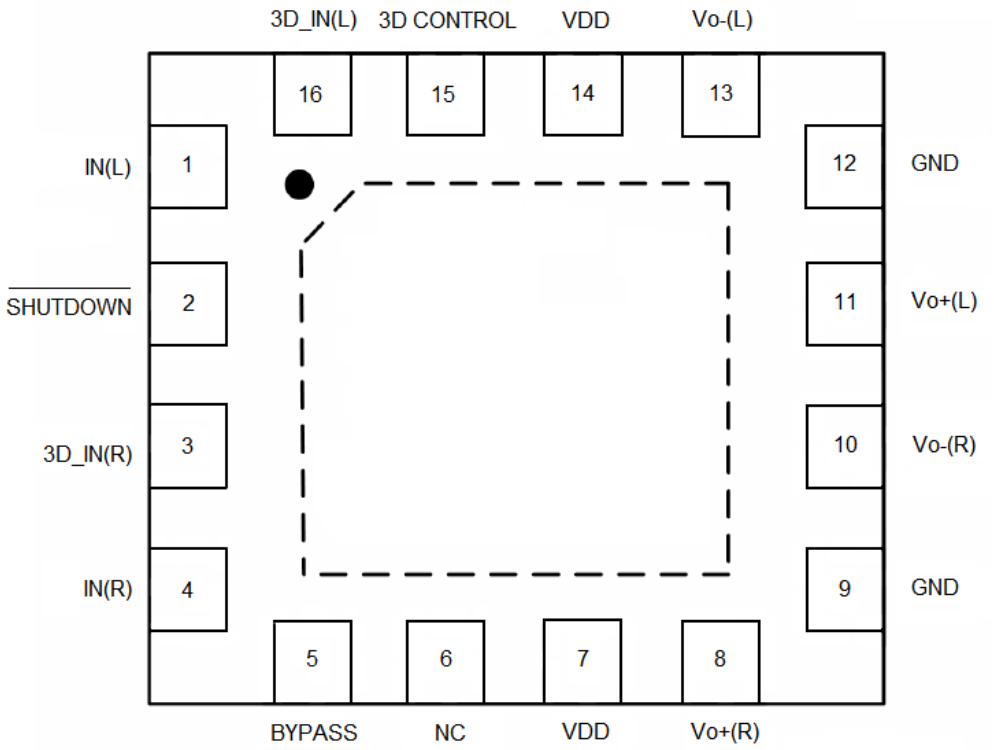
- Portable electronic devices.
- Mobile Phones.
- Multimedia TFT LCD TVs / Monitors.

PIN CONFIGURATION

LY8221 SOP16 Pin Configuration (Top View)



LY8221 QFN16 Pin Configuration (Top View)



PIN DESCRIPTION

SYMBOL	Pin No.		DESCRIPTION
	SOP16	QFN16	
3D CONTROL	1	15	3D selection pin. (when **HIGH** level is 3D mode).
3D_INL	2	16	3D Input of left channel.
INL	3	1	Input of left channel.
Shutdown	4	2	Shutdown control pin. (when **LOW** level is shutdown mode).
3D_INR	5	3	3D Input of right channel.
INR	6	4	Input of right channel.
Bypass	7	5	Bypass pin.
NC	8	6	No connection
V_{DD}	9/16	7/14	Power supply of left and right channel.
Vo+(R)	10	8	Positive(+) BTL output of right channel.
GND	11/14	9/12	Ground
Vo-(R)	12	10	Negative(-) BTL output of right channel.
Vo+(L)	13	11	Positive(+) BTL output of left channel.
Vo-(L)	15	13	Negative(-) BTL output of left channel.

ORDERING INFORMATION

Ordering Code	Speaker Channels	Pin/ Package	Output Power (THD+N=10%)	Input Type	Output Type	Feature
						3D
LY8221SL	Stereo	SOP16	3.0W/4Ω @5.5V_BTL 2.5W/4Ω @5.0V_BTL 1.8W/8Ω @5.5V_BTL 1.5W/8Ω @5.0V_BTL	SE	BTL	Yes
LY8221EL	Stereo	QFN16	3.0W/4Ω @5.5V_BTL 2.5W/4Ω @5.0V_BTL 1.8W/8Ω @5.5V_BTL 1.5W/8Ω @5.0V_BTL	SE	BTL	Yes

TYPICAL APPLICATION CIRCUIT

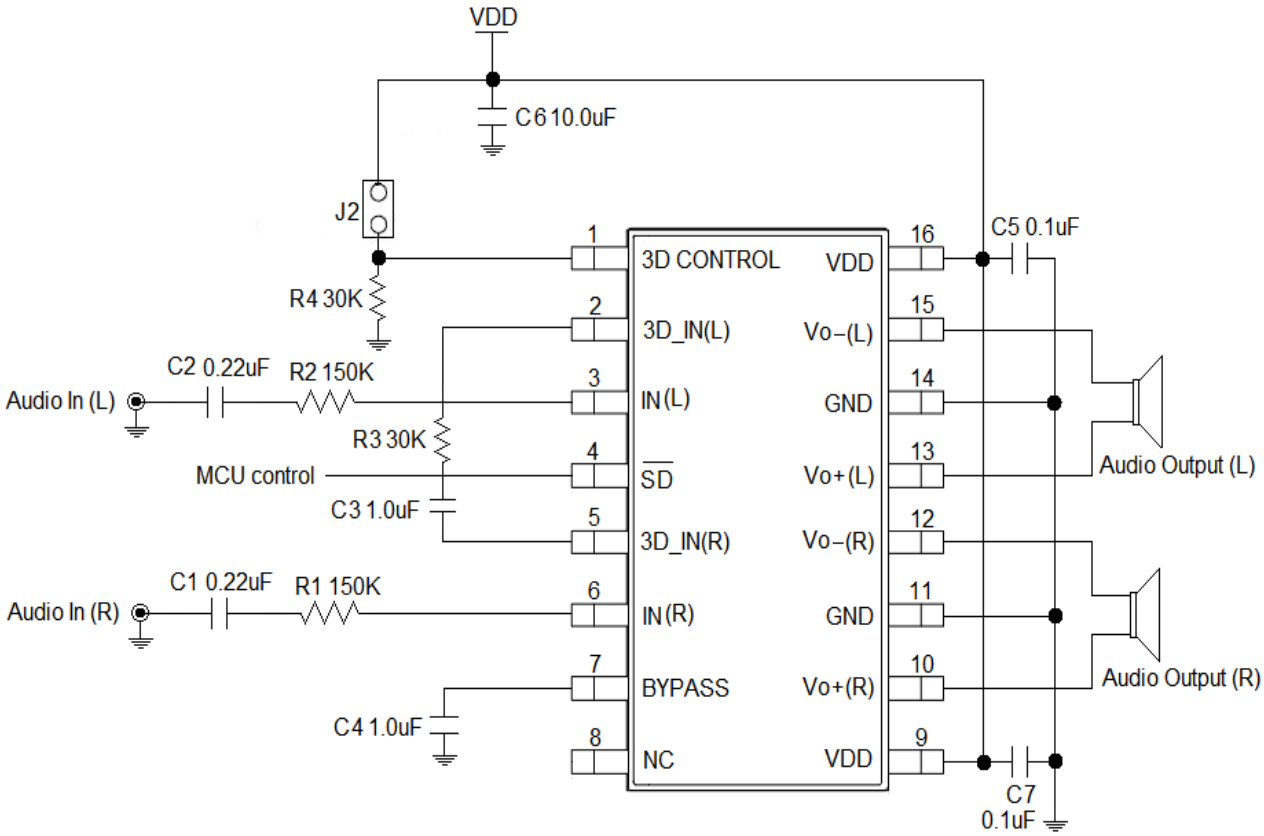


Figure 1. LY8221SL Typical Application Circuit with 3D

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{DD}	6.0	V
Operating Temperature	T_A	-40 to 85 (I grade)	℃
Input Voltage	V_I	-0.3V to V_{DD} +0.3V	V
Storage Temperature	T_{STG}	-65 to 150	℃
Power Dissipation	P_D	Internally Limited	W
ESD Susceptibility	V_{ESD}	2000	V
Junction Temperature	T_{JMAX}	150	℃
Soldering Temperature (under 10 sec)	T_{SOLDER}	260	℃

ELECTRICAL CHARACTERISTICS (T_A = 25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.*1	MAX.	UNIT
Power supply voltage	V_{DD}		2.5	-	5.5	V
Quiescent Current	I_Q	V_{DD} = 5.5V, No Load	-	6.5	-	mA
		V_{DD} = 3.6V, No Load	-	5.5	-	
		V_{DD} = 2.5V, No Load	-	4.5	-	
Shutdown Current	I_{SD}	$V_{SHUTDOWN} \leqq$ 0.8V, V_{DD} = 2.5V to 5.5V	-	0.1	-	μA
High-level input voltage	V_{IH}	$\overline{\text{Shutdown}}$	1.2	-	V_{DD}	V
Low-level input voltage	V_{IL}	$\overline{\text{Shutdown}}$	0	-	0.4	V
Output offset voltage	$\lvert V_{OS} \rvert$	V_I = 0 V, Av = 2 V/V, V_{DD} = 2.5 V to 5.5 V	-	-	25	mV

▪ OPERATING CHARACTERISTICS (1)(T_A = 25℃)

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP.*1	MAX.	UNIT
Out Power / Channel	P_O	R_L= 4Ω f = 1 kHz,	THD+N=10%	V_{DD}=5.5V	-	3.0	-	W
				V_{DD}=5.0V	-	2.5	-	
				V_{DD}=3.6V	-	1.25	-	
				V_{DD}=2.5V	-	0.55	-	
			THD+N=1%	V_{DD}=5.5V	-	2.5	-	
				V_{DD}=5.0V	-	2.0	-	
				V_{DD}=3.6V	-	1.0	-	
				V_{DD}=2.5V	-	0.4	-	
		R_L= 8Ω f = 1 kHz,	THD+N= 10%	V_{DD}=5.5V	-	1.8	-	
				V_{DD}=5.0V	-	1.5	-	
				V_{DD}=3.6V	-	0.75	-	
				V_{DD}=2.5V	-	0.35	-	
			THD+N= 1%	V_{DD}=5.5V	-	1.45	-	
				V_{DD}=5.0V	-	1.2	-	
				V_{DD}=3.6V	-	0.6	-	
				V_{DD}=2.5V	-	0.25	-	

(*1)Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at VCC = VCC(TYP.) and T_A = 25℃

▪ OPERATING CHARACTERISTICS (2)(T_A = 25℃)

PARAMETER	SYMBOL	TEST CONDITION			MIN.	TYP. *1	MAX.	UNIT
Crosstalk	Cs	V_{DD} = 3.6 V, R_L = 8Ω f=1kHz,		V_{DD}=3.6V	-	-100	-	dB
Signal-to-noise ratio	SNR	PO= 1.0 W, R_L = 8Ω		V_{DD}=5.0V	-	85	-	dB
Output voltage noise	Vn	V_{DD} = 5.0 V, R_L = 8Ω, f = 20 Hz to 20 kHz, Inputs ac-grounded with Ci = 0.22 µF		No weighting	-	100	-	uV_{RMS}
Start-up time from shutdown	Z_I	V_{DD} = 5.0V	C_{bypass} = 2.2µF		-	316	-	ms
			C_{bypass} = 1.0µF		-	272	-	
			C_{bypass} = 0.47µF		-	96	-	
			C_{bypass} =0.1µF		-	60	-	
			C_{bypass} =56nF		-	36	-	
		V_{DD} = 3.7V	C_{bypass} = 2.2µF		-	244	-	
			C_{bypass} = 1.0µF		-	192	-	
			C_{bypass} = 0.47µF		-	76	-	
			C_{bypass} =0.1µF		-	40	-	
			C_{bypass} =56nF		-	36	-	
Frequency	Fc	VDD=2.5V~5.5V			-	230	-	kHz
Closed-loop Gain	Gv	V_{DD} = 2.5V to 5.5V			-	150kΩ/Ri	-	

(*1)Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at VCC = VCC(TYP.) and T_A = 25℃

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 2
Total Harmonic Distortion + Noise vs Output Power (R_L = 4Ω, Stereo)

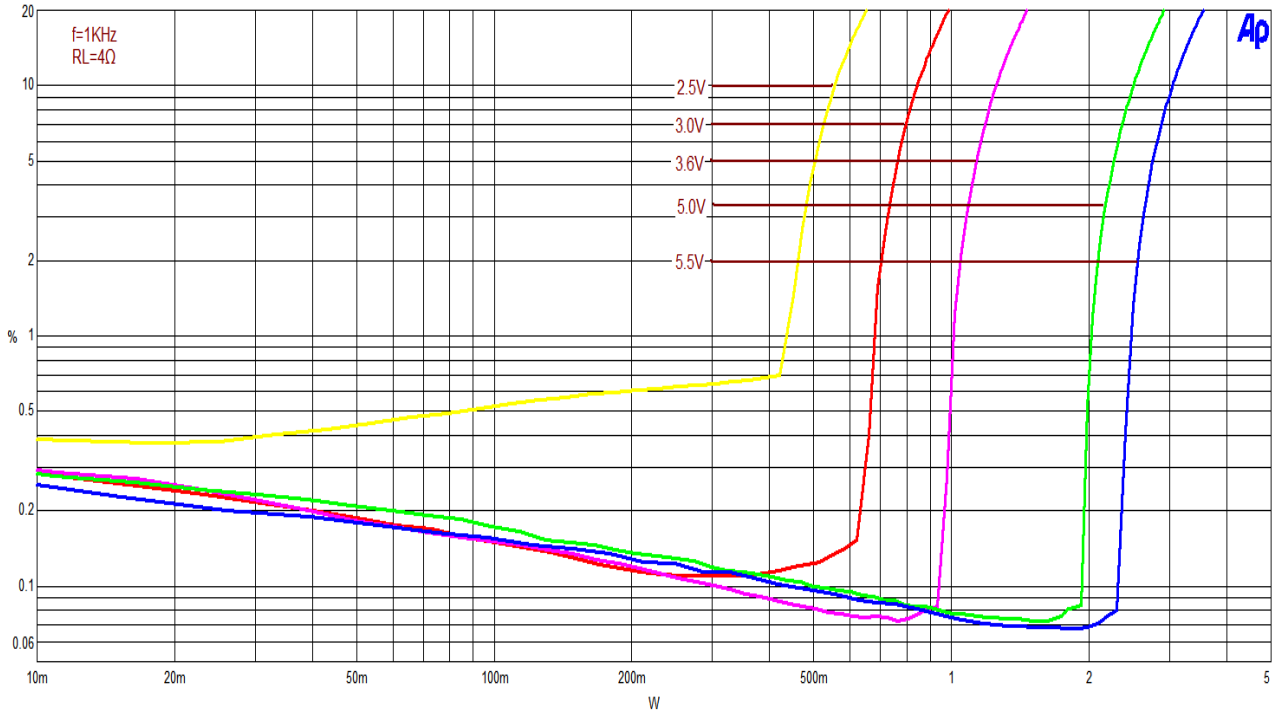


Figure 3
Total Harmonic Distortion + Noise vs Output Power (R_L = 8Ω, Stereo)

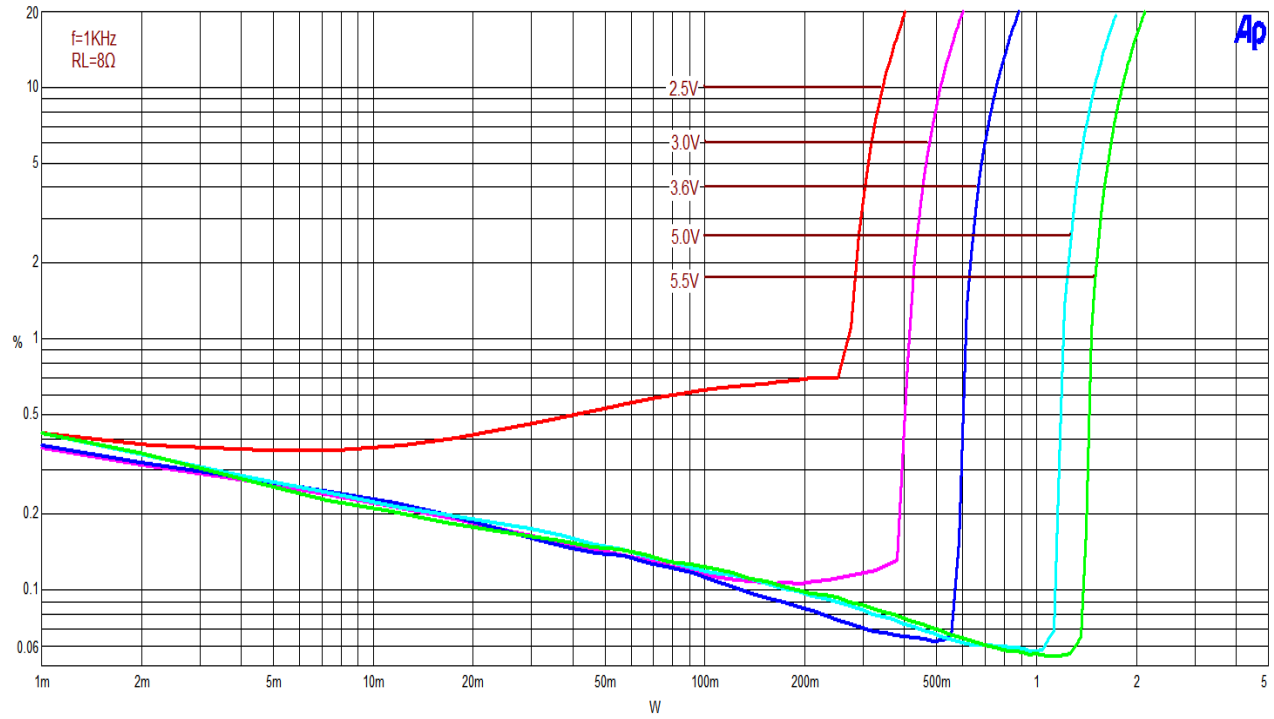


Figure 4
Noise Floor (VDD=5.0V / R_L=8Ω)

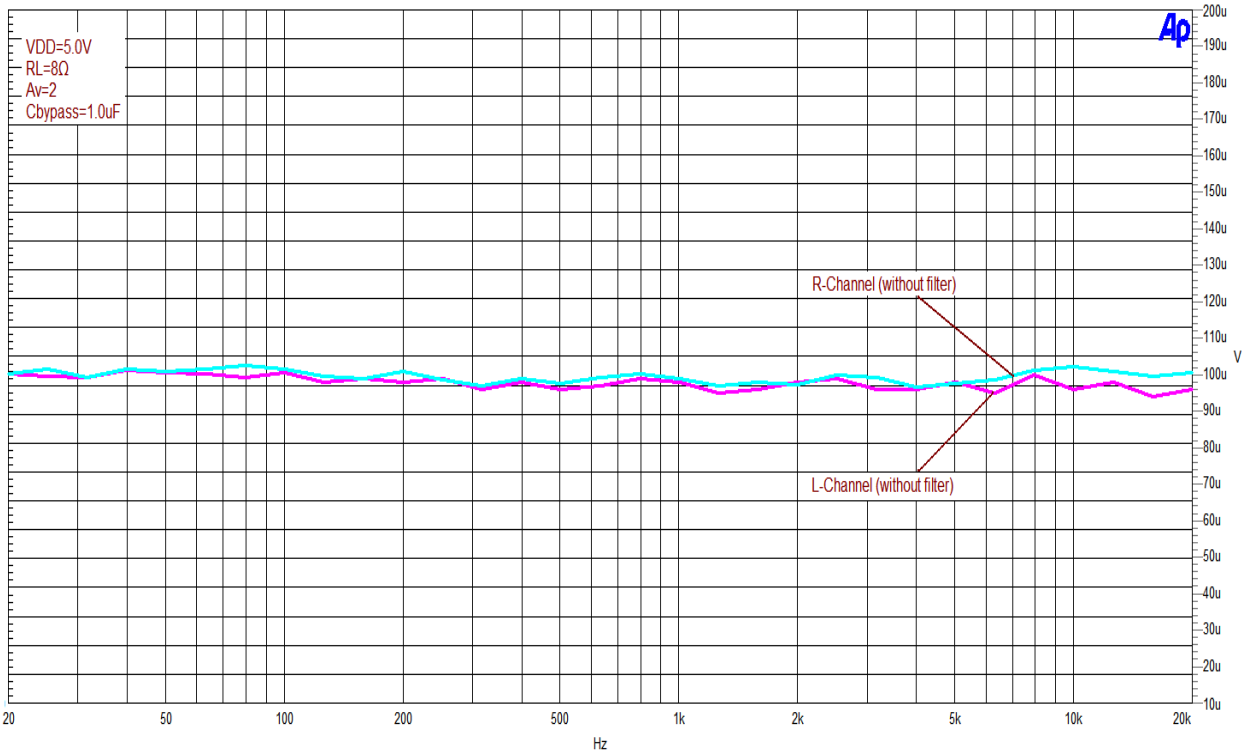
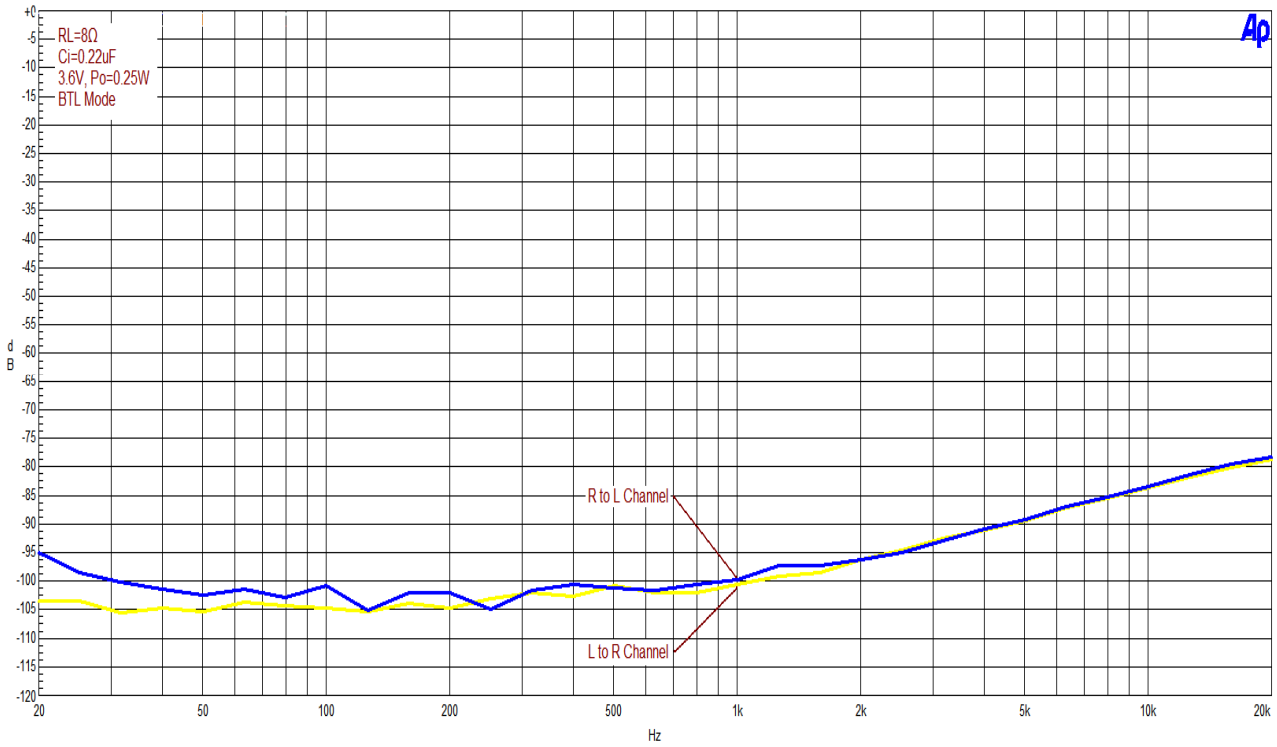
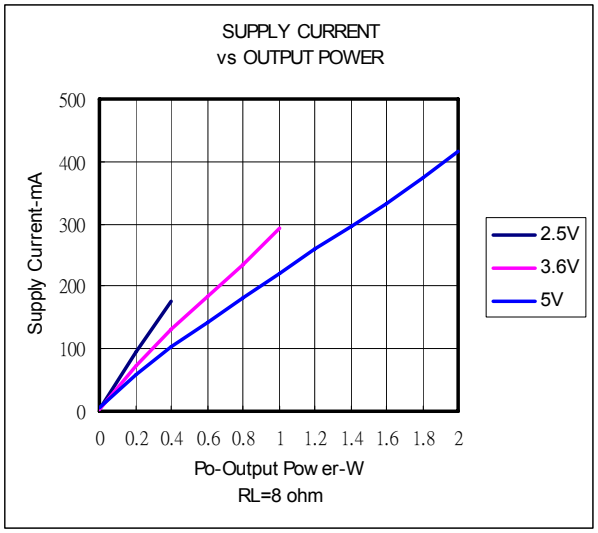


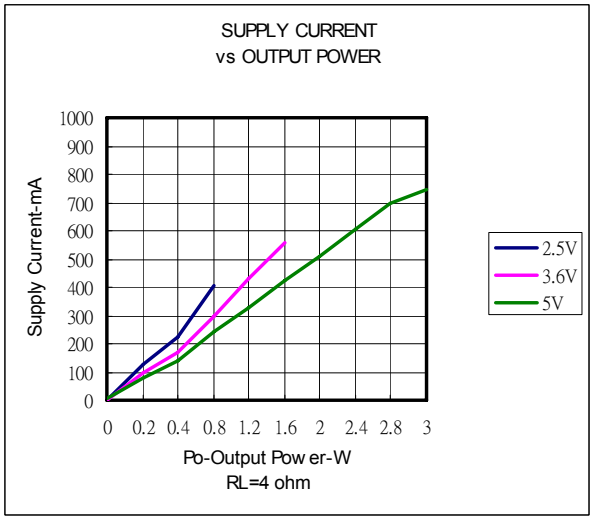
Figure 5
Crosstalk (VDD=3.6V / R_L=8Ω)



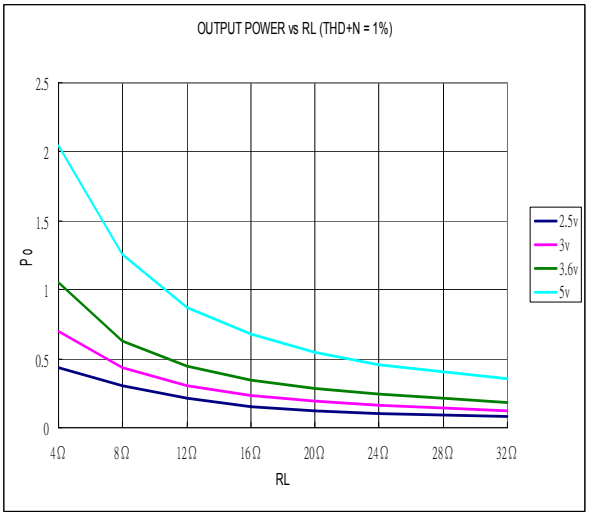
Supply Current vs Output Power (8Ω)



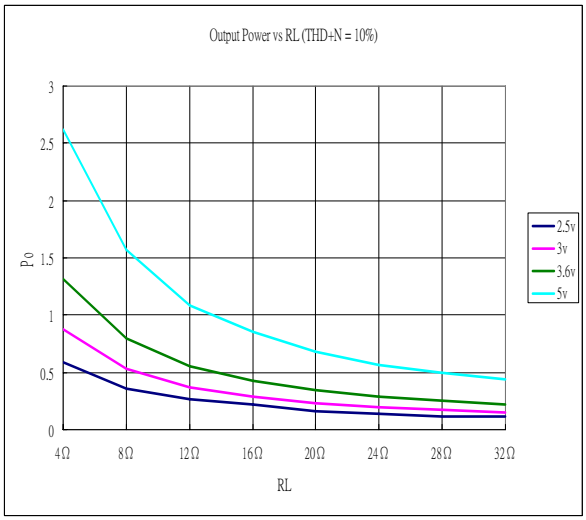
Supply Current vs Output Power (4Ω)



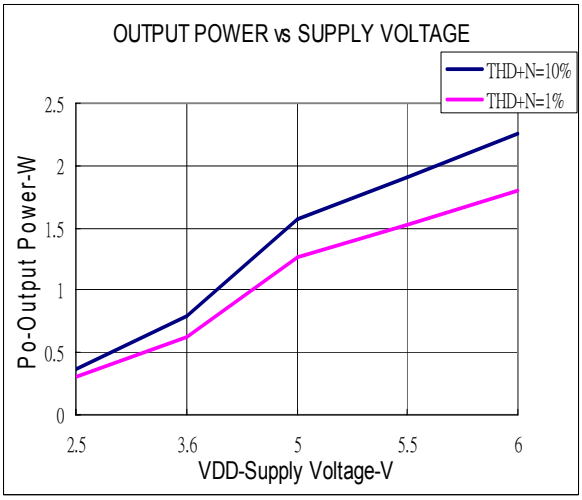
Output Power vs RL (THD+N = 1%)



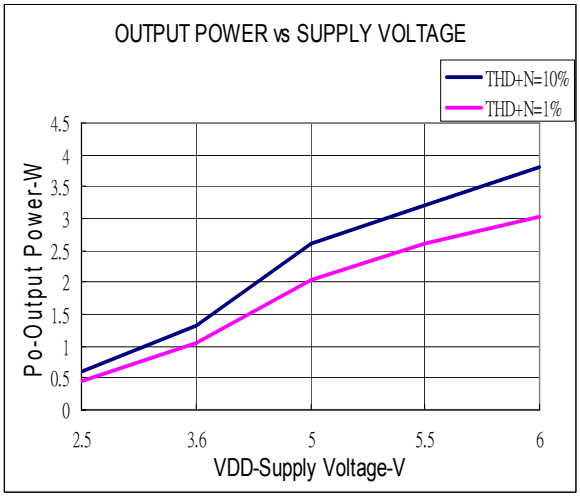
Output Power vs RL (THD+N = 10%)



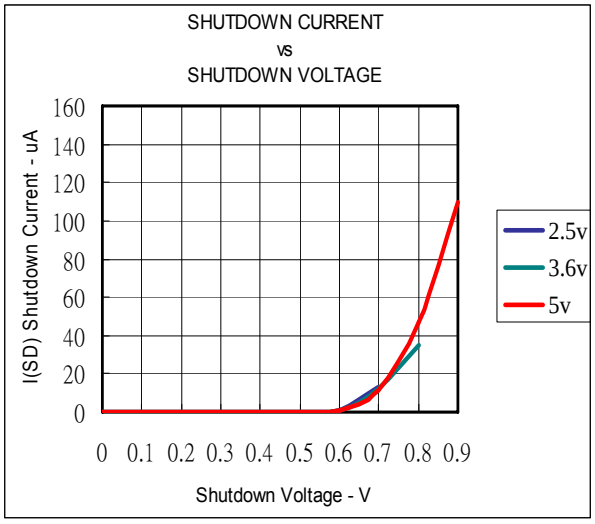
Output Power vs Supply Voltage (8Ω)



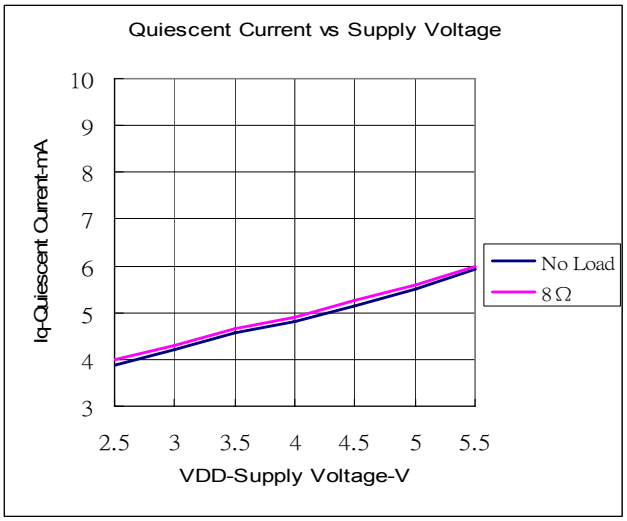
Output Power vs Supply Voltage (4Ω)



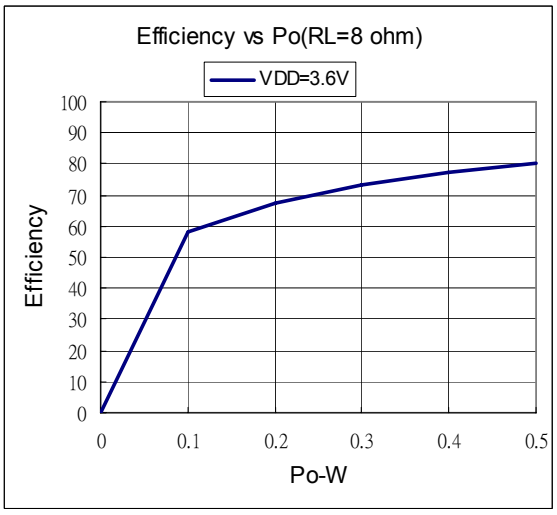
Shutdown vs Shutdown Voltage



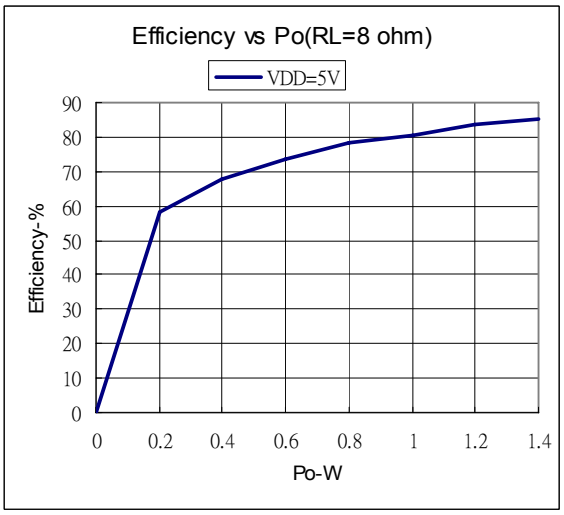
Quiescent Current vs Supply Voltage



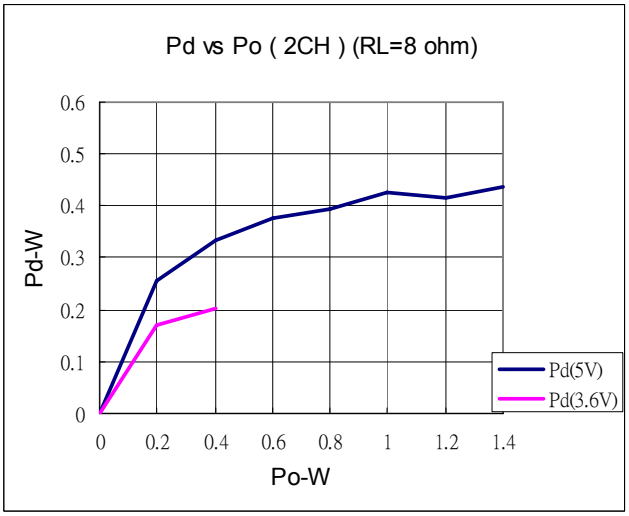
Efficiency vs Po(RL=8 ohm) VDD=3.6V



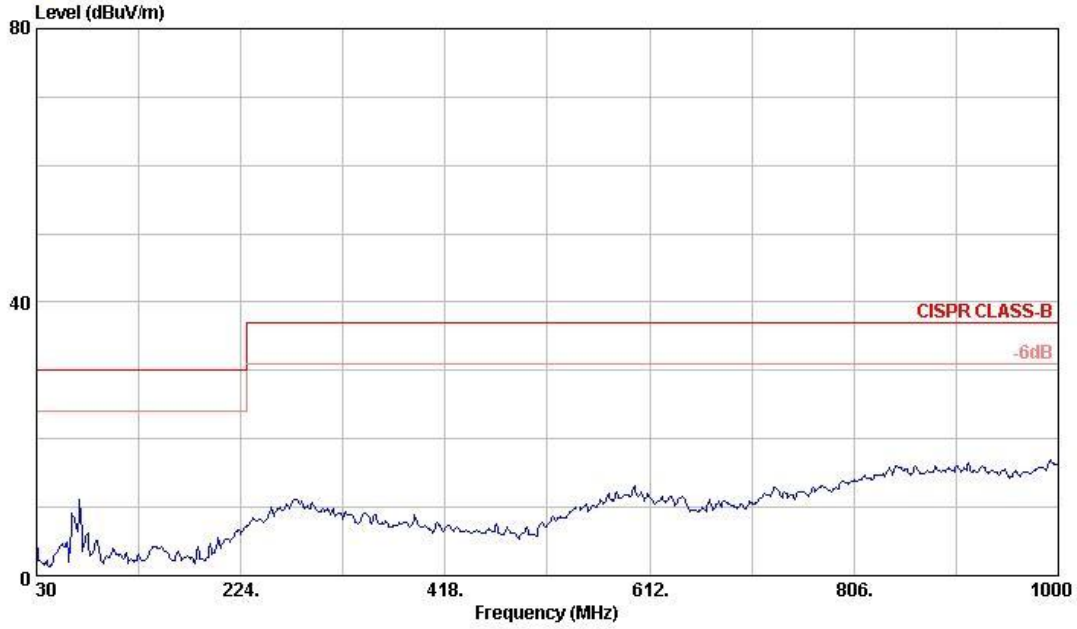
Efficiency vs Po(RL=8 ohm) VDD=5.0V



Power Dissipation vs Output Power

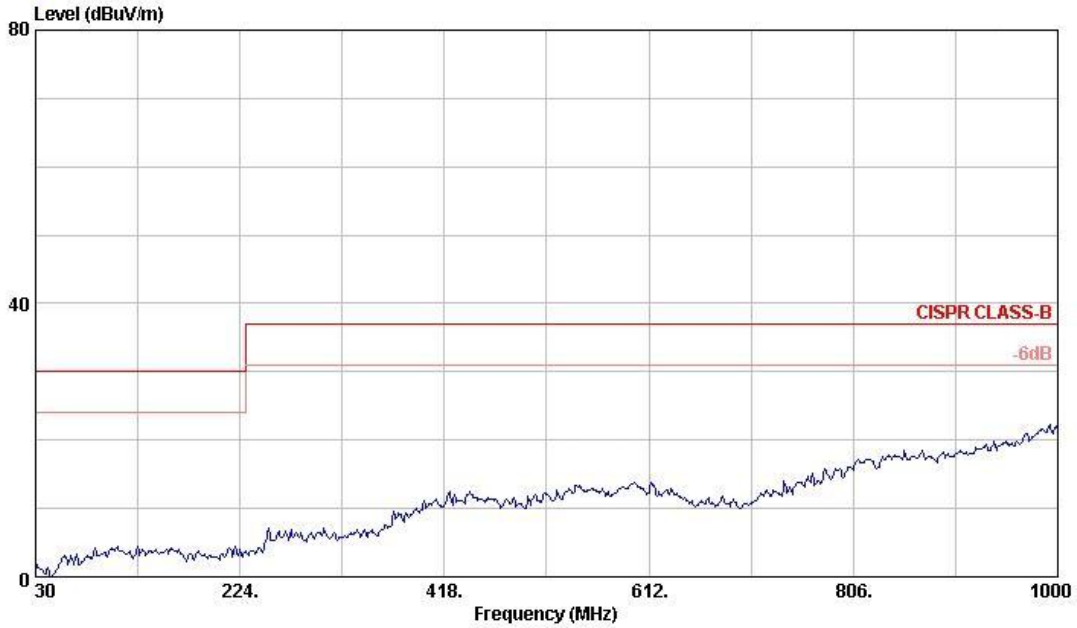


FCC Class-B (Vertical) – Stereo Mode



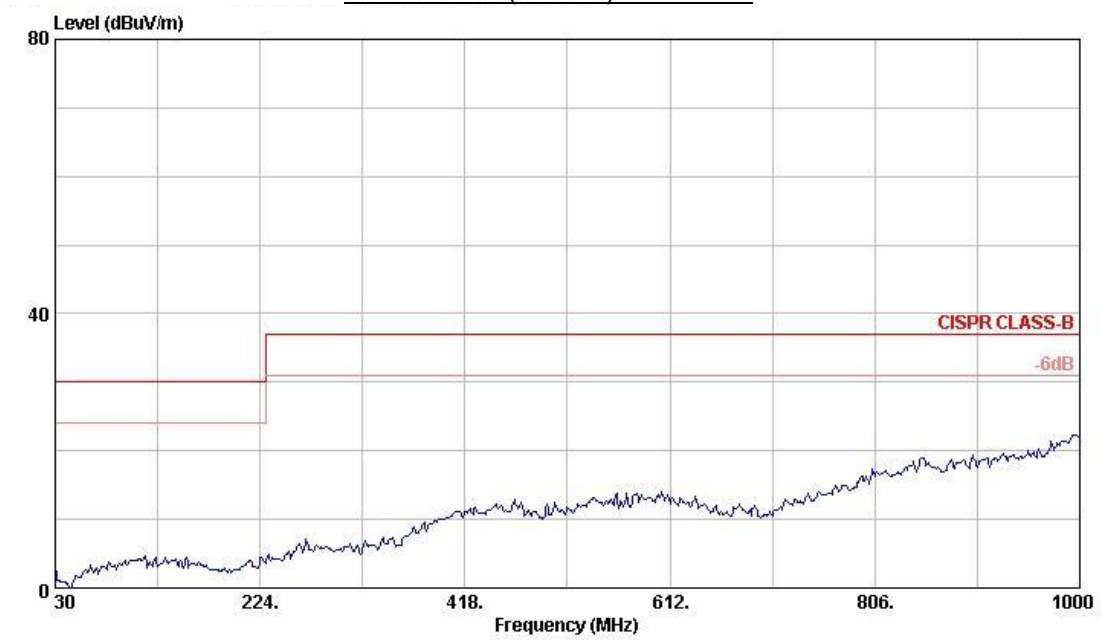

```
Site            : chamber size: 7m X 4m X 3m
Condition       : CISPR CLASS-B 10m WINSUNTEK VERTICAL
eut             : LY8221(LT5115B)
mode            : STRERE
memo            : HTC  DESIRE ;+BEAD ;4.5V
```

FCC Class-B (Horizontal) – Stereo Mode



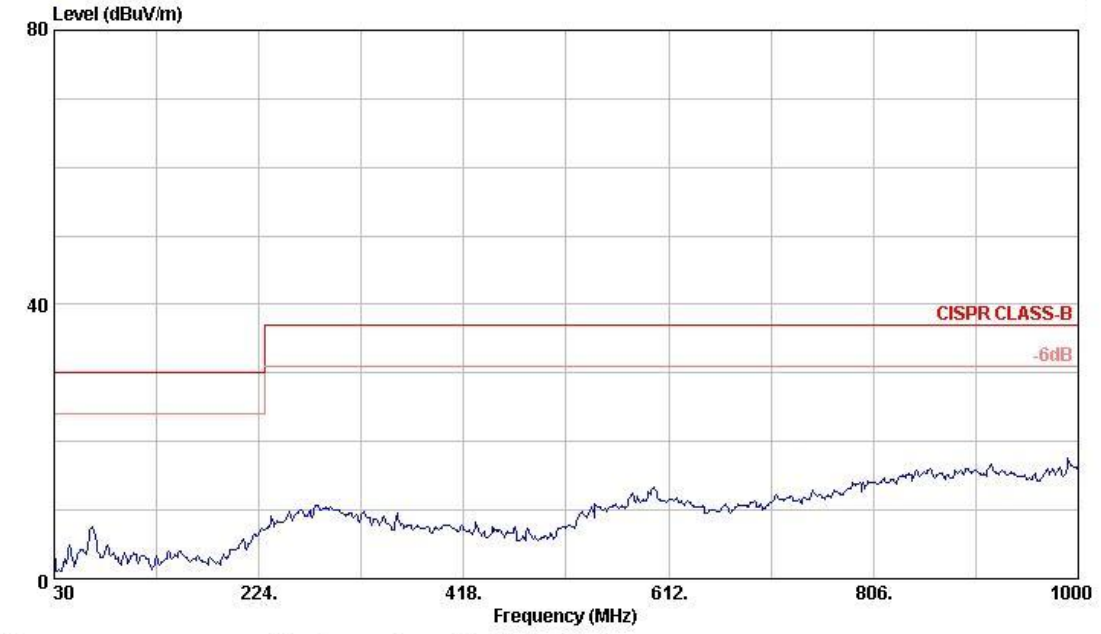

```
Site            : chamber size: 7m X 4m X 3m
Condition       : CISPR CLASS-B 10m WINSUNTEK HORIZONTAL
eut             : LY8221(LT5115B)
mode            : STRERE
memo            : HTC  DESIRE ;+BEAD ;4.5V
```

FCC Class-B (Vertical) – 3D Mode




```
Site            : chamber size: 7m X 4m X 3m
Condition       : CISPR CLASS-B 10m WINSUNTEK HORIZONTAL
eut             : LY8221(LT5115B)
mode            : STRERE ; 3D
memo            : HTC  DESIRE ;+BEAD ;4.5V
```

FCC Class-B (Horizontal) – 3D Mode




```
Site            : chamber size: 7m X 4m X 3m
Condition       : CISPR CLASS-B 10m WINSUNTEK VERTICAL
eut             : LY8221(LT5115B)
mode            : STEREO ; 3D
memo            : HTC  DESIRE ;+BEAD ;4.5V
```

▪ APPLICATION INFORMATION

Input Resistors (Ri) and Gain

The LY8221 has two internal amplifier stages. The pre-amplifier gain is externally configurable, while the total gain is internally fixed. The closed-loop gain of the pre-amplifier gain is set by selecting the Rf to Ri while the total gain is fixed at 2x. So the input resistors (R_i) set the gain of the amplifier according to the equation.

Pre-Amplifier Gain = Rf / Ri

Total Gain = (Rf / Ri) x 2

A_{VD} = 20 x log [2 x (Rf /Ri)]

The resistor matching is very important in the amplifiers. Balance of the output on the reference voltage depends on matched ratio of the resistors. CMRR, PSRR, and cancellation of the second harmonic distortion if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to keep the performance optimized. Matching is more important than overall tolerance.
Resistor arrays with 1% matching can be used with a tolerance greater than 1%.Place the input resistors very close to the LY8221 to limit noise injection on the high-impedance nodes. For optimal performance the gain should be set to 2 V/V or lower. Lower gain allows the LY8221 to operate at its best,

For example

Table 1. Typical Total Gain and A_{VD} Values

Rf (KΩ)	150	150	150	150	150	150
Ri (KΩ)	150	75	50	37.5	25	18.75
Pre AMP. Gain	1	2	3	4	6	8
Total Gain	2	4	6	8	12	16
A_{VD} (db)	6.02	12.04	15.56	18.06	21.58	24.08

Input Capacitors (Ci)

The LY8221 using fully differential source, So the input coupling capacitors are required. The input capacitors and input resistors form a high-pass filter with the corner frequency(f_c), determined in the equation.

fc = 1 / (2πRi Ci)

The value of the input capacitor is important to consider as it directly affects the bass (low frequency) performance of the circuit. Speakers in wireless phones cannot usually respond well to low frequencies, so the corner frequency can be set to block low frequencies in this application. Equation is reconfigured to solve for the input coupling capacitance.

Ci = 1 / (2πRi fc)

If the corner frequency is within the audio band, the capacitors should have a tolerance of ±10% or better, because any mismatch in capacitance causes an impedance mismatch at the corner frequency and below.

For example

In the table 2 shows the external components. Rin in connect with Cin to create a high-pass filter.

Table 2. Typical Component Values

Reference	Description	Note
Ri	150KΩ	1% tolerance resistors
Ci	0.22uF	80%/–20%

Ci = 1 / (2πRi fc)

Ci = 1 / (2π x 150KΩ x 4.8Hz)=0.221uF，Use 0.22uF

Decoupling Capacitor (Cs)

The LY8221 is a high-performance class-D audio amplifier that requires adequate power supply decoupling to ensure the efficiency is high and total harmonic distortion (THD) is low. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1.0uF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the LY8221 is very important for the efficiency of the class-D amplifier, because any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency. For filtering lower-frequency noise signals, a 10.0uF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Over-Heat Protection

The LY8221 has a built-in over-heat protection circuit, it will turn off all power output when the chip temperature over 150℃, the chip will return to normal operation automatically after the temperature cool down to 120℃.

3D Enhance

The LY8221 has a built-in 3D enhance effect that widens the perceived soundstage from the stereo audio signal. The 3D enhance improves the apparent stereo channel separation whenever the left and right speakers are too close, due to system size constraints or equipment limitations.
Activating the 3D effect by applying VDD to pin 1 (3D Control) and external RC network (Shown in figure 1) is required to enable the 3D effect. The amount of the 3D effect is set by the R3 and C3. Decreasing the value of R3 will increase the 3D effect. Increasing the value of the capacitors C3 will decrease the low cutoff frequency at which the 3D effect starts to occur.The amount of perceived 3D is also dependent on many other factors such as speaker placement and the distance to the listener. Therefore,it is recommended that the user try various values of R3 and C3 to get a feel for how the 3D effect works in the application.

PCB Layout

All the external components must place very close to the LY8221. The input resistors need to be very close to the LY8221 input pins so noise does not couple on the high impedance nodes between the input resistors and the input amplifier of the LY8221. Then place the decoupling capacitor Cs, close to the LY8221 is important for the efficiency of the class-D amplifier. Any resistance or inductance in the trace between the device and the capacitor can cause a loss in efficiency.

Making the high current traces going to VDD, GND, V_{O+} and V_{O-} pins of the LY8221 should be as wide as possible to minimize trace resistance. If these traces are too thin, the LY8221's performance and output power will decrease. The input traces do not need to be wide, but do need to run side-by-side to enable common-mode noise cancellation.

▪ DEMO BOARD INFORMATION

Demo Board Application Circuit (BTL)

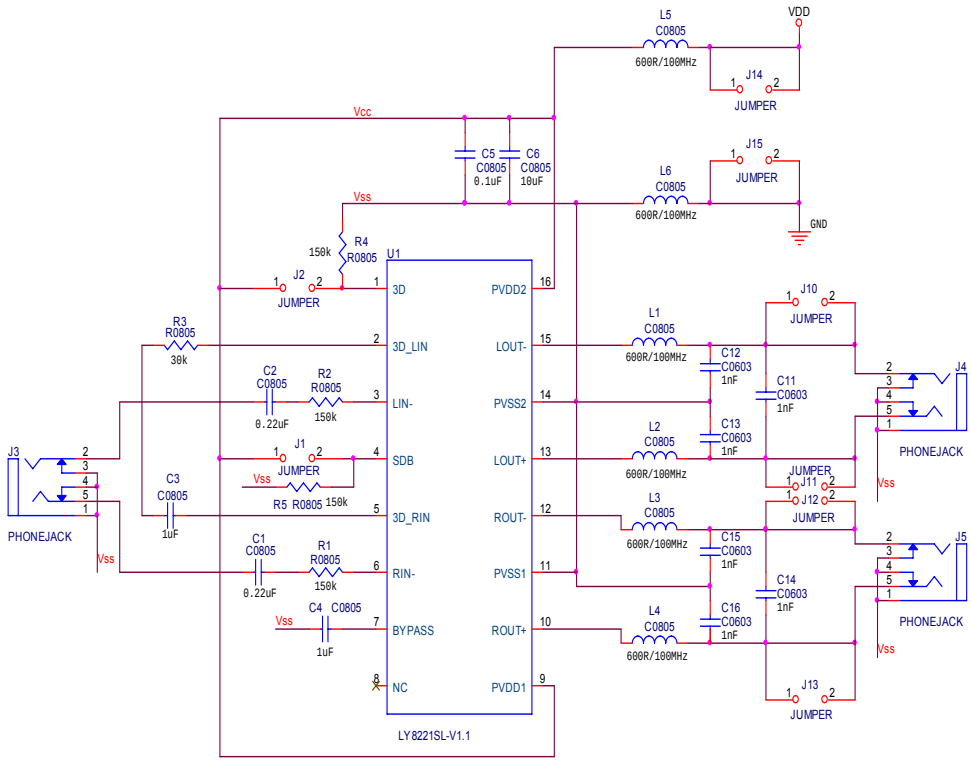


Figure 2 LY8221SL Demo Board Application Circuit

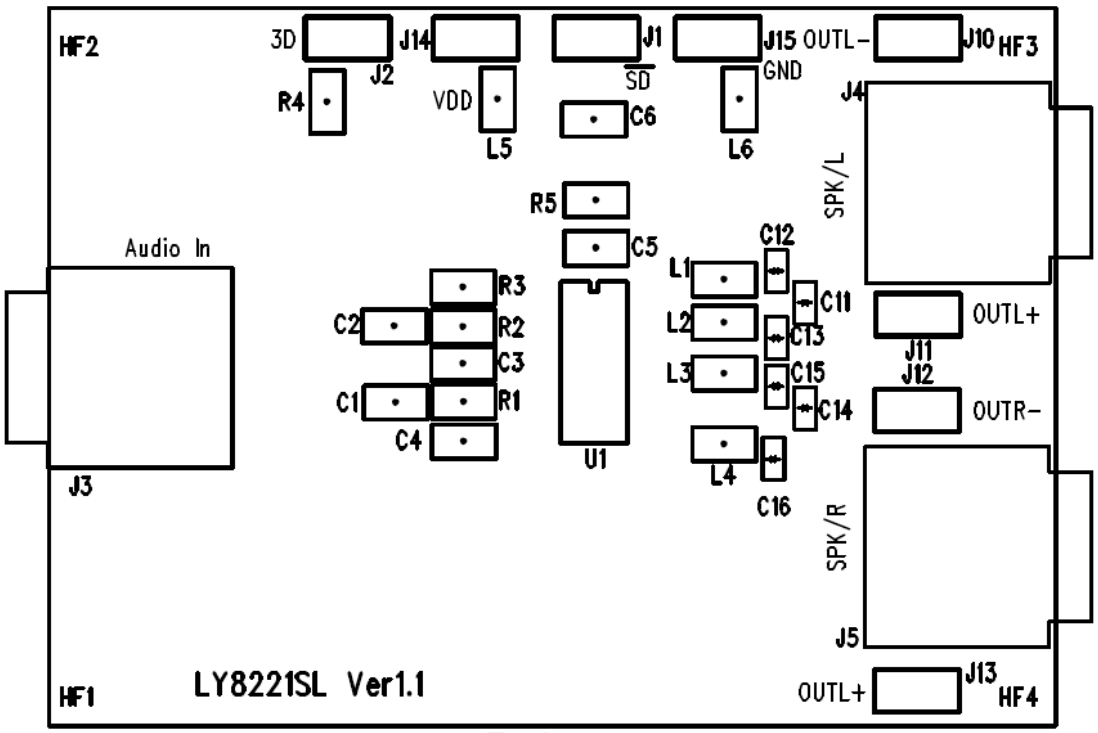
Demo Board BOM List

LY8221SL (BTL) V1.1 BOM List

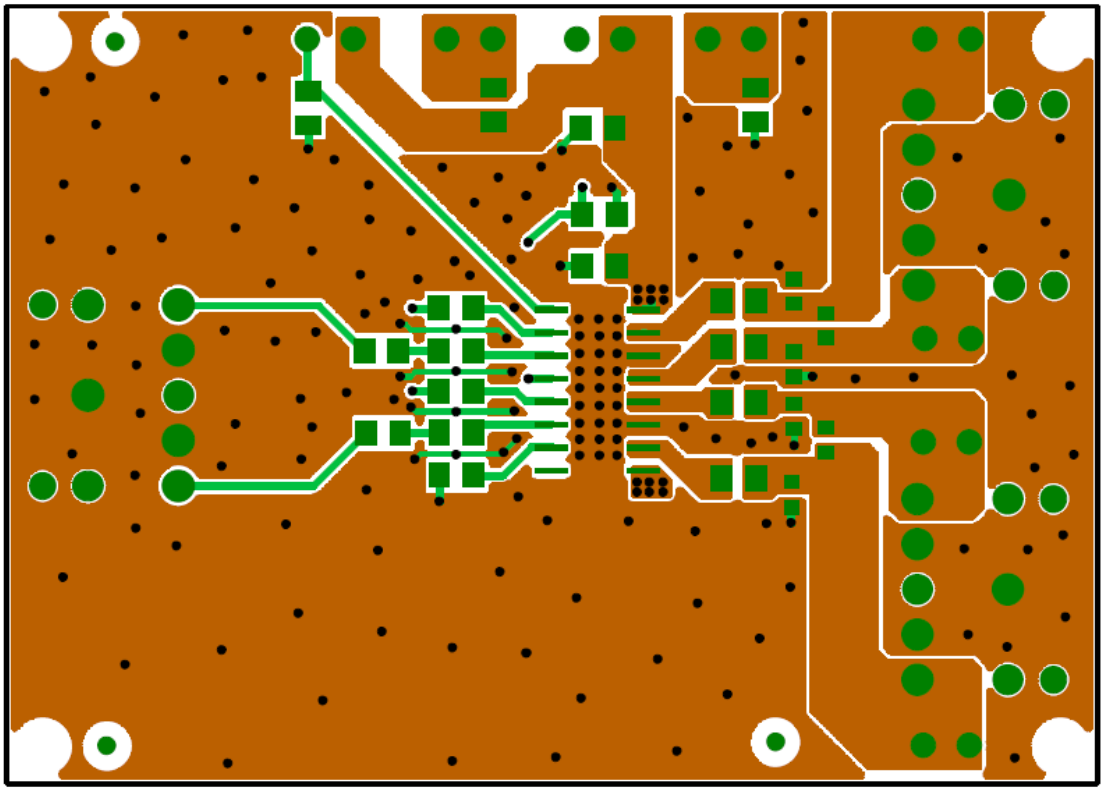
No.	Description	Reference	Note
1	Resistor, 30KΩ	R3	1/16W,1%
2	Resistor, 150KΩ	R1,R2,R4,R5	1/16W,1%
3	Capacitor, 330pF(Option)	C12,C13,C15,C16	80%/−20%, nonpolarized
4	Capacitor, 390pF(Option)	C11,C14	80%/−20%, nonpolarized
5	Capacitor, 0.1uF	C5	80%/−20%, nonpolarized
6	Capacitor, 0.22uF	C1,C2	80%/−20%, nonpolarized
7	Capacitor, 1.0uF	C3,C4	80%/−20%, nonpolarized
8	Capacitor, 10.0uF	C6	80%/−20%, 6.3 V
9	Chip Bead 1KΩ/100MHz(Option)	L1,L2,L3,L4,L5,L6	1000Ω(1KΩ)±25%/100MHz
10	IC	U1	LY8212SL, SOP16
8	1*2 Pin Header	J1,J2	J1 Open → shutdown J2 Short → 3D enable

Demo Board Artwork

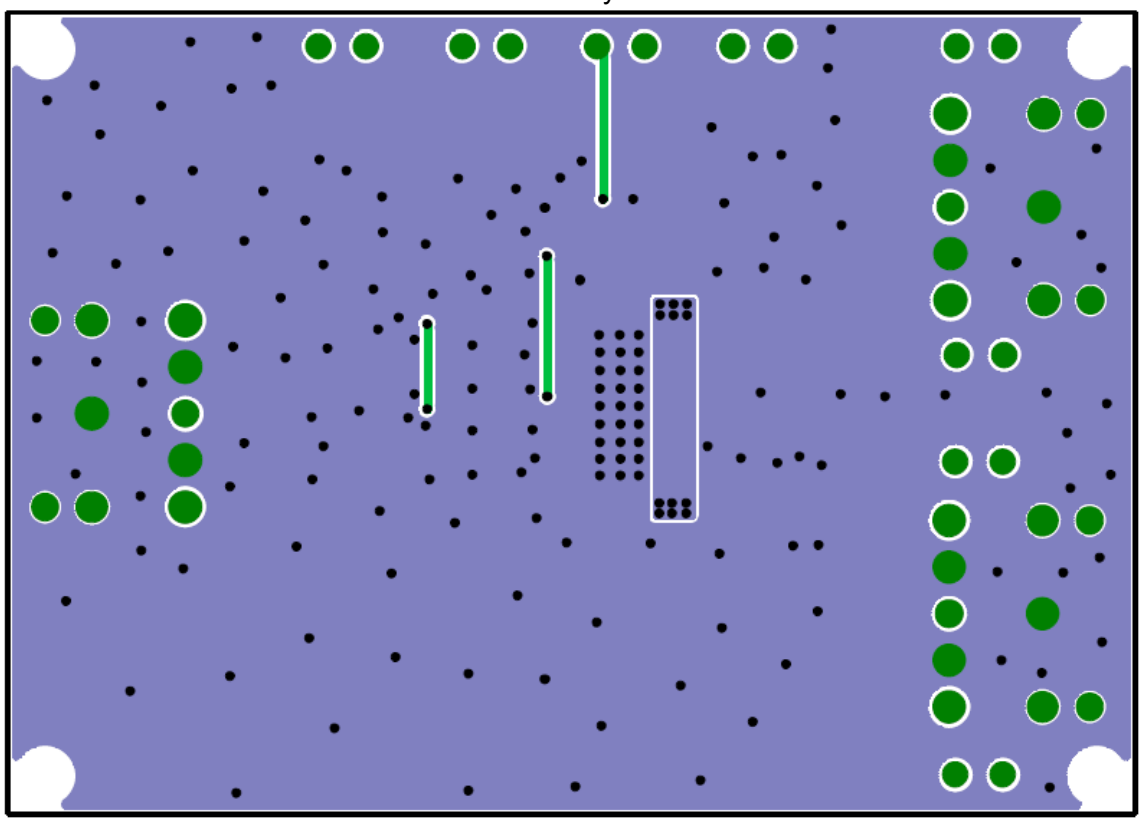
Top Silkscreen



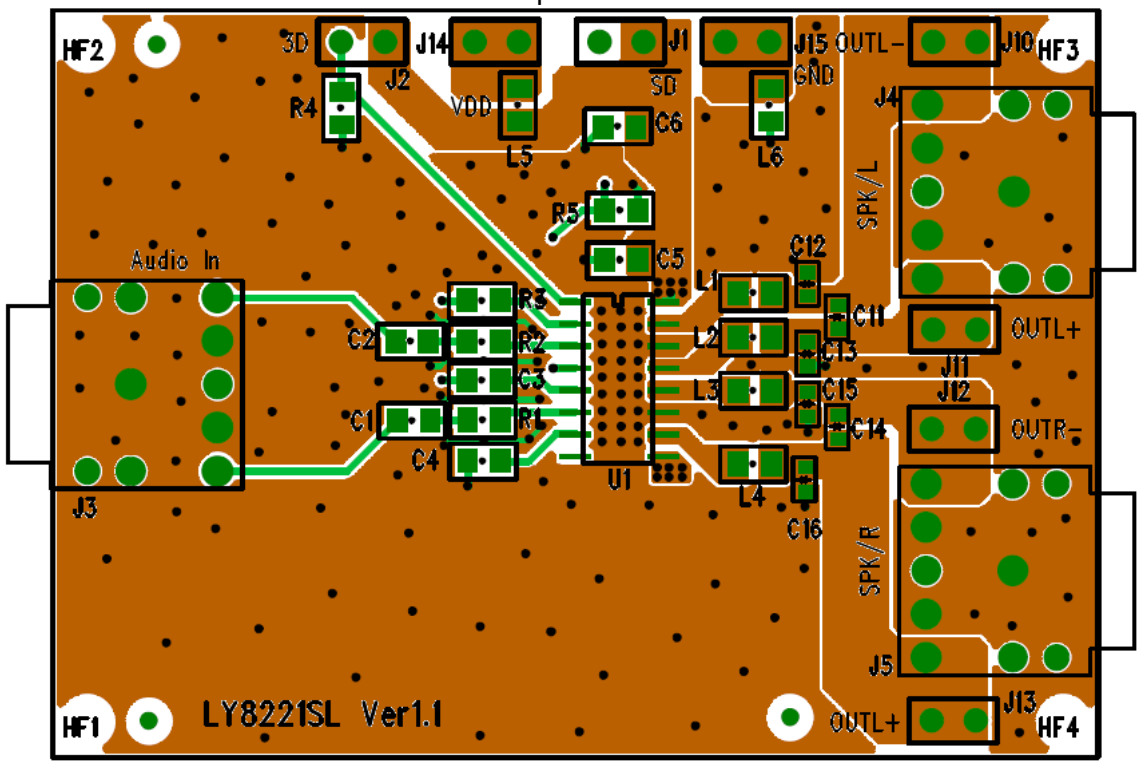
Top Layer



Bottom Layer

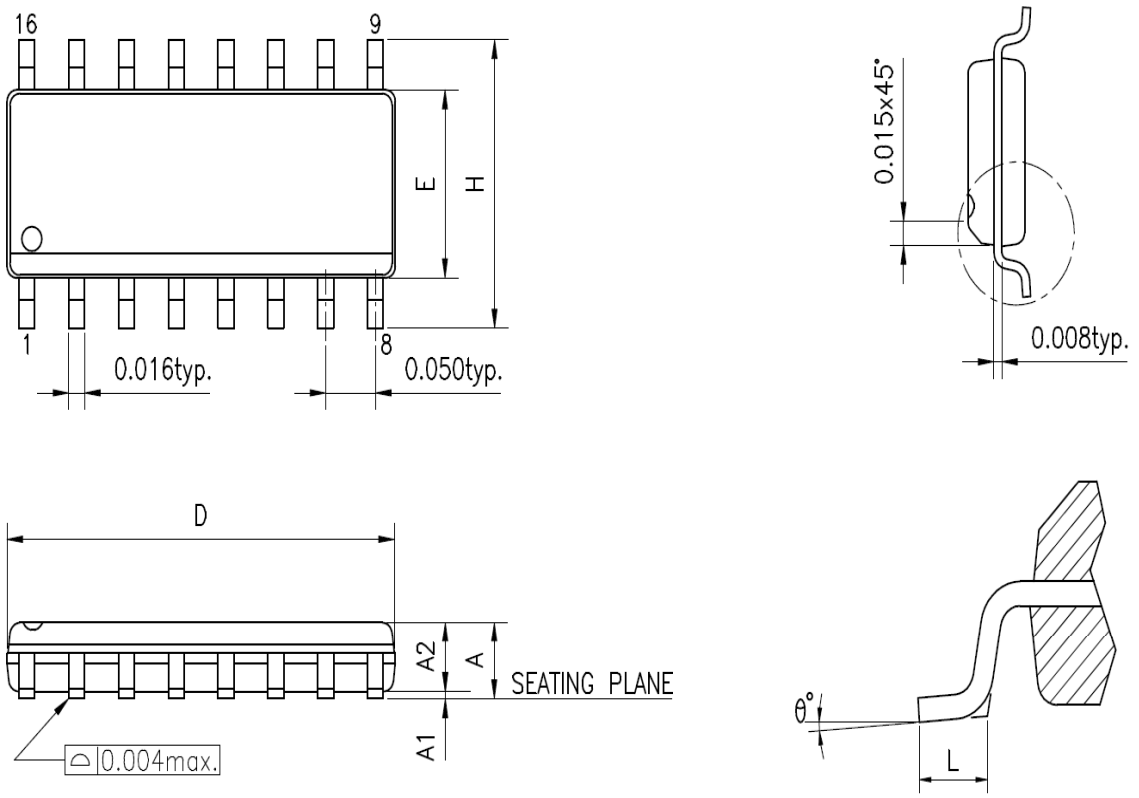


Composite view



PACKAGE OUTLINE DIMENSION

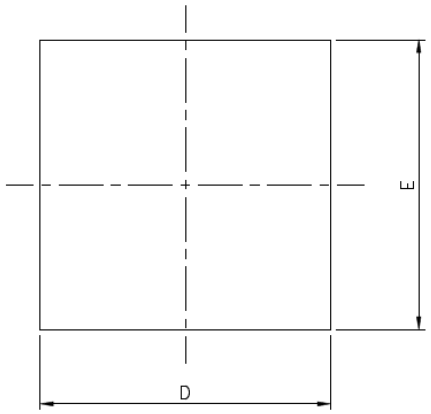
SOP 16 Pin Package Outline Dimension



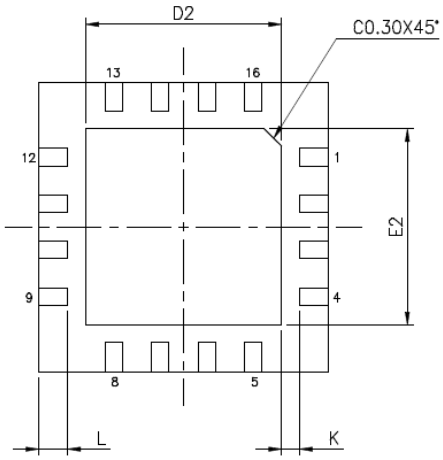
	STANDARD	
SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	0.049	0.065
D	0.386	0.394
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

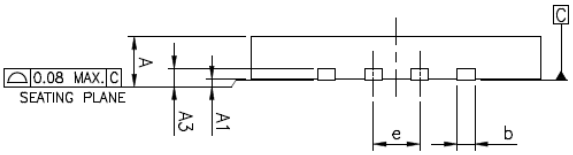
UNIT : INCH

QFN(5x5) 16 Pin Package Outline Dimension



	PACKAGE TYPE					
JEDEC OUTLINE				MO-220		
PKG CODE	WQFN(N/A)			VQFN(Y516)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35
D	4.95	5.00	5.05	4.95	5.00	5.05
E	4.95	5.00	5.05	4.95	5.00	5.05
e	0.80 BSC			0.80 BSC		
L	0.45	0.50	0.55	0.45	0.50	0.55
K	0.20	—	—	0.20	—	—





	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
142X142 MIL	3.28	3.38	3.43	3.28	3.38	3.43	V	X	N/A