United Monolithic Semiconductors

CHK8015-99F

16W Power Transistor

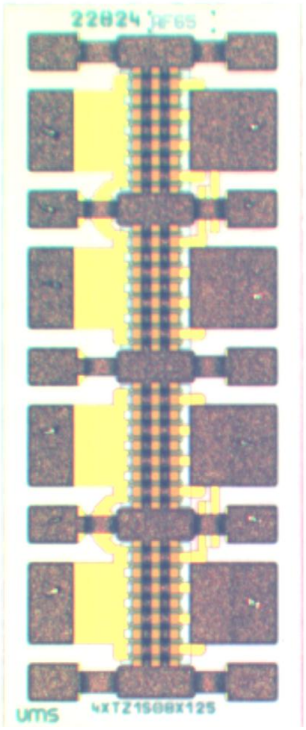
GaN HEMT on SiC

Description

The CHK8015-99F is a 16W Gallium Nitride High Electron Mobility Transistor. This product offers a general purpose and broadband solution for a variety of RF power applications.

The circuit is manufactured with a 0.25µm gate length GaN HEMT technology on SiC substrate.

It is proposed in a bare die form and requires an external matching circuitry.



Main Features

- Wide band capability up to 18GHz
- Pulsed and CW operating modes
- GaN technology: High Pout & High PAE
- DC bias: V_D=30V @I_{D_Q}=200mA
- Chip size 0.88x2x0.1mm
- RoHS N°2011/65
- REACh N°1907/2006

Main Electrical Characteristics

T_{ref} = +25°C, CW mode, Freq = 9GHz, V_{DS} = 30V, I_{D_Q} = 200mA

Symbol	Parameter	Min	Typ	Max	Unit
G_{SS}	Small Signal Gain		17		dB
P_{SAT}	Saturated Output Power		20		W
PAE	Max Power Added Efficiency		68		%
G_{PAE_MAX}	Associated Gain at Max PAE		11		dB

These values are deduced from elementary power cell performances

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Recommended Operating Ratings

T_{ref} = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{DS}	Drain to Source Voltage			30	V	
V_{GS}	Gate to Source Voltage		-3.3		V	V_{DS}=30V, I_{D_Q}=200mA
V_{DG_peak}	Drain-Gate Voltage		80		V	DC+RF
V_{GS_peak}	Gate-Source Voltage		-20		V	DC+RF
I_{D_Q}	Quiescent Drain Current		0.2	0.46	A	V_{DS}=30V
I_{D_MAX}	Drain Current		1	(1)	A	V_{DS}=30V, Compressed mode
I_{G_MAX}	Gate Current in forward mode		0	16	mA	DC or Compressed mode
T_{j_MAX}	Junction temperature			200	°C	(1)

(1) Power dissipation must be considered

DC Characteristics

T_{ref} = +25°C

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_P	Pinch-Off Voltage	-4	-3.4	-2.8	V	V_D=10V,I_D= I_{DSS} /100
I_{D_SAT}	Saturated Drain Current		3.6		A	(1), V_D=10V, V_G=1V
I_{G_leak}	Gate Leakage Current	-0.8			mA	V_D=50V, V_G=-7V
V_{BDG}	Drain-Gate Break-down Voltage		120		V	V_G=-7V, I_D=20mA
R_{TH}	Thermal Resistance		6		°C/W	CW mode, T_{ref}=75°C, (2)

(1) For information, limited by I_{D_MAX} , see on ROR & AMR

(2) The thermal resistance is given for the power bar mounted on carrier plate (20µm Au/Sn soldering + 1.4mm Cu/Mo/Cu). The reference temperature is defined on the carrier back side. Thermal analysis is highly recommended, more details are available on request.

RF Characteristics

T_{ref} = +25°C, CW mode, Freq = 9GHz, V_{DS} = 30V, I_{D_Q} = 200mA

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
G_{SS}	Small Signal Gain		17		dB	
P_{SAT}	Saturated Output Power		20		W	
PAE	Max Power Added Efficiency		68		%	
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Absolute Maximum Ratings

T_{ref} = +25°C[1] [2] [3]

Symbol	Parameter	Rating	Unit	Note
V_{DS_Q}	Drain-Source Biasing Voltage	55	V	
V_{GS_Q}	Gate-Source Biasing Voltage	-10, +2	V	
V_{DG_peak}	Drain-Gate Voltage (DC+RF)	120	V	
V_{GS_peak}	Gate-Source Voltage (DC+RF)	-25	V	
I_{G_MAX}	Maximum Gate Current	32	mA	
I_{G_MIN}	Minimum Gate Current	-2	mA	
I_{D_MAX}	Maximum Drain Current	See note	A	[4]
P_{IN}	Maximum Input Power	See note	dBm	[5]
T_j	Maximum Junction Temperature	230	°C	
T_{STG}	Storage Temperature	-55 to +150	°C	
T_{Case}	Case Operating Temperature	See note	°C	[4]

[1] Operation of this device above anyone of these parameters may cause permanent damage.

[2] Duration < 1s.

[3] The given values must not be exceeded at the same time even momentarily for any parameter, since each parameter is independent from each other, otherwise deterioration or destruction of the device may take place.

[4] Max junction temperature must be considered

[5] Linked to and limited by Ig_max & Ig_min values. Maximum input power depends on frequency and should not exceed 2dB above PAE_max.

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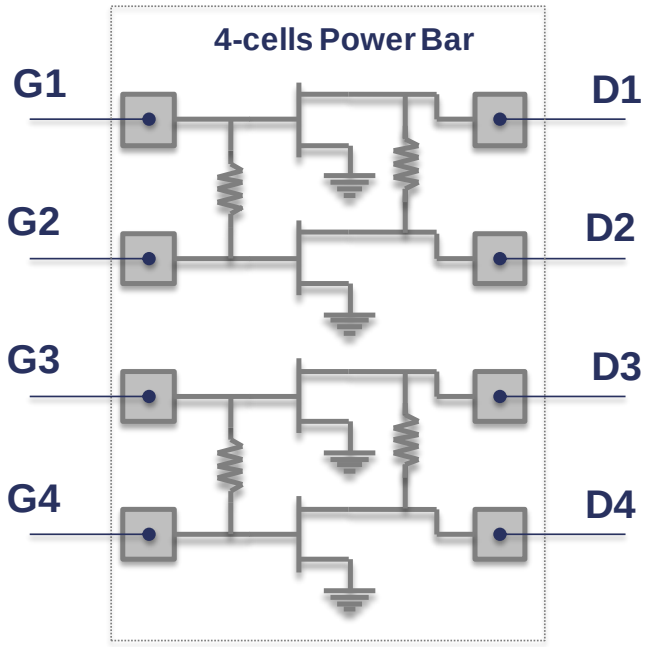
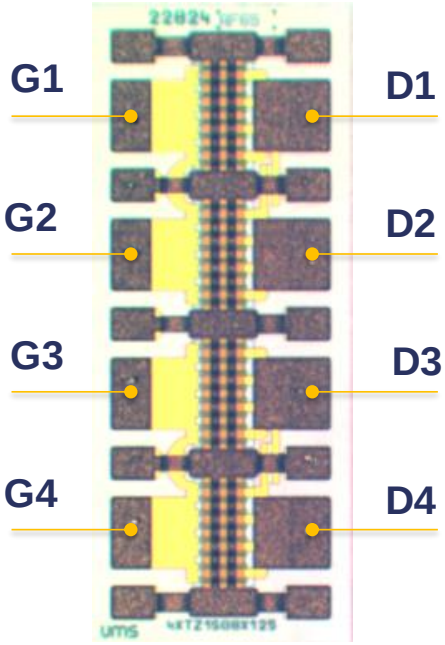
Power Bar Description

The device is composed of 4 elementary 4W cells. These cells are connected together with a specific network providing a good trade-off between performance and stability (resistance between gates and drains as described on the schematic). The reference plans are on the center of the bonding pads.

A multiport non-linear model is available on request.





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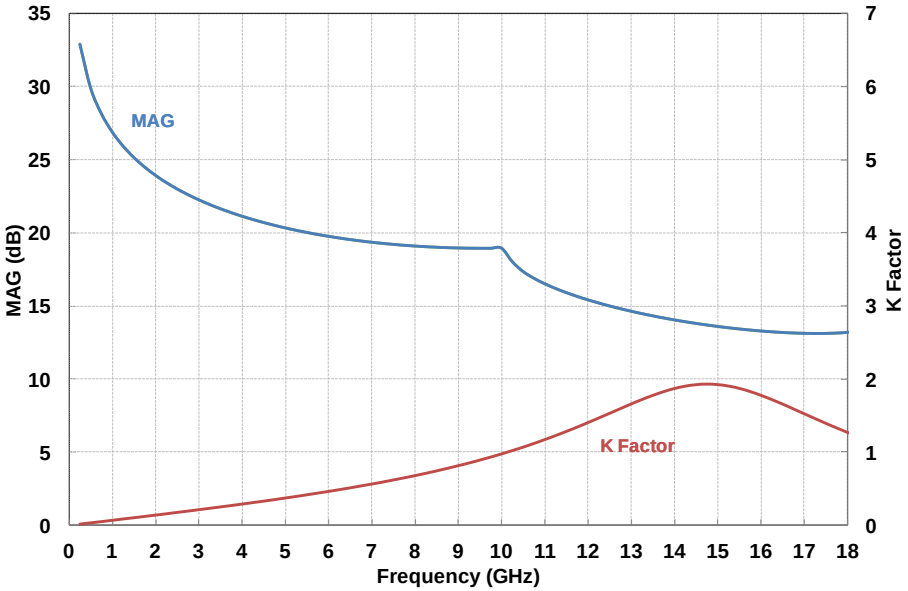
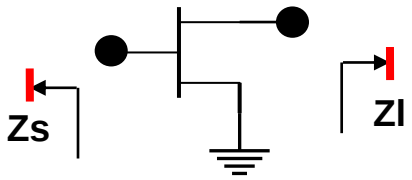
Elementary Cell Maximum Gain & Stability Characteristics

T_{ref} = +25°C, V_{DS} = +30V, I_{D_Q} = 50mA, simulated results



Elementary Cell Load Pull Performances

T_{ref} = +25°C, V_{DS} = +30V, I_{D_Q} = 50mA, simulated results



The impedances are chosen as a trade-off between Output Power, PAE and Stability of the device. Second harmonic of output load has been tuned.
These values are given in the bonding pads reference plan.

Frequency (GHz)	Zs	Zl	Gain (dB) @PAE_{max}	PAE_{max} (%)	Pout (W) @PAE_{max}	$Pout_{max}$ (W)
3	15 + j18	60 + j65	12.8	72	4.9	5.3
6	8.2 + j14.8	24.8 + j51.7	12.4	69	4.4	5
9	2.8 + j6.4	11.7 + j33.7	10.8	68	4.7	5.1
12	2.1 + j3.5	8 + j24	10	52	3.8	4.8
15	1.87 + j0	5 + j17.3	8.6	50	3.6	4.7
18	1.7 – j3.1	4 + j12.7	7.6	46	3.6	4.8

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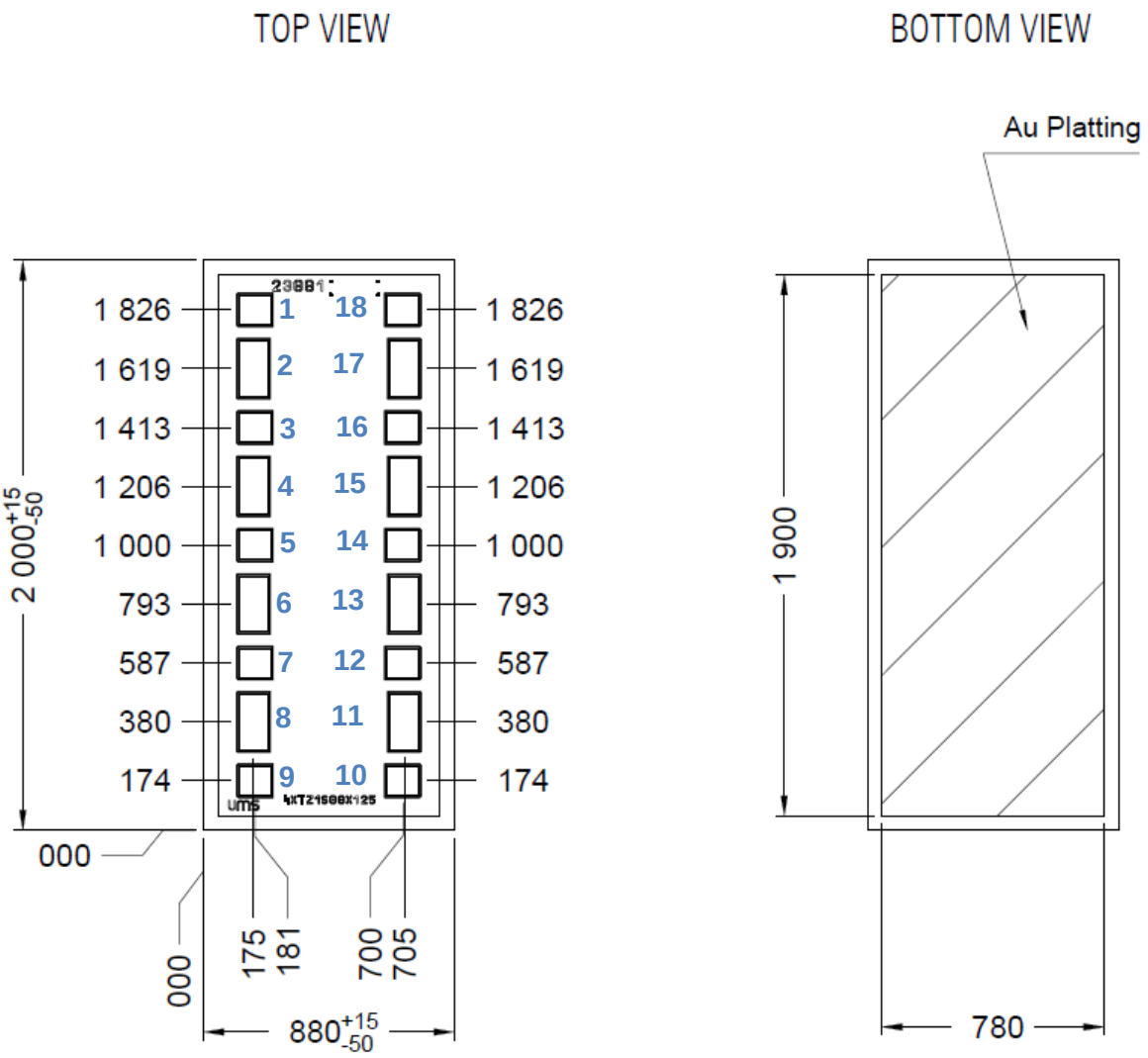
Mechanical data



Chip thickness: 100µm +/- 10 µm
All dimensions are in micrometers

GND pads (1, 3, 5, 7, 9, 10, 12, 14, 16, 18) = 99x130µm²
DC Gate pads (2, 4, 6, 8) = 214 x 120µm²
DC Drain pads (11, 13, 15, 17) = 214 x 120µm²

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Notes

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Qualification domain

This part is qualified according to UMS standards, excluding humid environment.

User guide for MMIC storage, pick & place, die attach, wire bonding

Refer to the application note AN0001 available at http://www.ums-gaas.com for general recommendations on chip handling.

Recommended environmental management

UMS products are compliant with the regulation in particular with the directives RoHS N°2011/65 and REACh N°1907/2006. More environmental data are available in the application note AN0019 also available at http://www.ums-gaas.com.

Recommended ESD management

Refer to the application note AN0020 available at http://www.ums-gaas.com for ESD sensitivity and handling recommendations for the UMS package products.

User guide GaN Power Bars Assembly guide lines

Refer to the application note AN0026 available at http://www.ums-gaas.com for general recommendations on SiC Transistor handling and assembly.

Ordering Information

Chip form:	CHK8015-99F/00

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