AK8456

3 channel input 16bit 30MSPS Video ADC with LED driver

1. General Description

AK8456 is an AFE for three channels contact image sensor (CIS). AK8456 has offset adjusting DAC, digital programmable gain amplifier (PGA) and LED drivers. AK8456 is suitable for multi-function printer and image scanner.

2. Feature

- ☐ Input Block
  - Channel number: 3 channel (1 channel mode is available)
  - Range: 1.3Vpp (min.)
  - Gain: 0dB/6dB
- ☐ ADC
  - Maximum conversion ratio: 30MSPS
    - 10MSPS/ch @ 3-channel mode
    - 30MSPS/ch @ 1-channel mode
  - Resolution: 16bit (Straight binary code/Gray code)
- ☐ Black correction DAC
  - Range: ±369mV (Equivalent input voltage) ＜±250mV(min.)＞
  - Resolution: 6bit
- ☐ Digital PGA
  - Range: 0dB~18dB
  - Resolution: 8bit
- ☐ Output Format: 8bit × 2
- ☐ LED Current: 67.2mA/ch (typ.) @ Maximum setting
  Adjustable by 12.5% resolution channel independently
- ☐ CPU I/F: 3-wire serial interface
- ☐ Supply Voltage: AFE: 3.3V±0.3V, LED driver: 4.5V~5.7V
- ☐ Power Consumption: 190 mW (typ.): Except LED drive current.
- ☐ Operating Temperature: 0°C~70°C
- ☐ Package: 36pin QFN (Exposed Die Pad), 0.4mm pitch, 5mm×5mm

3. Table of Contents

4. Block diagram and Functions

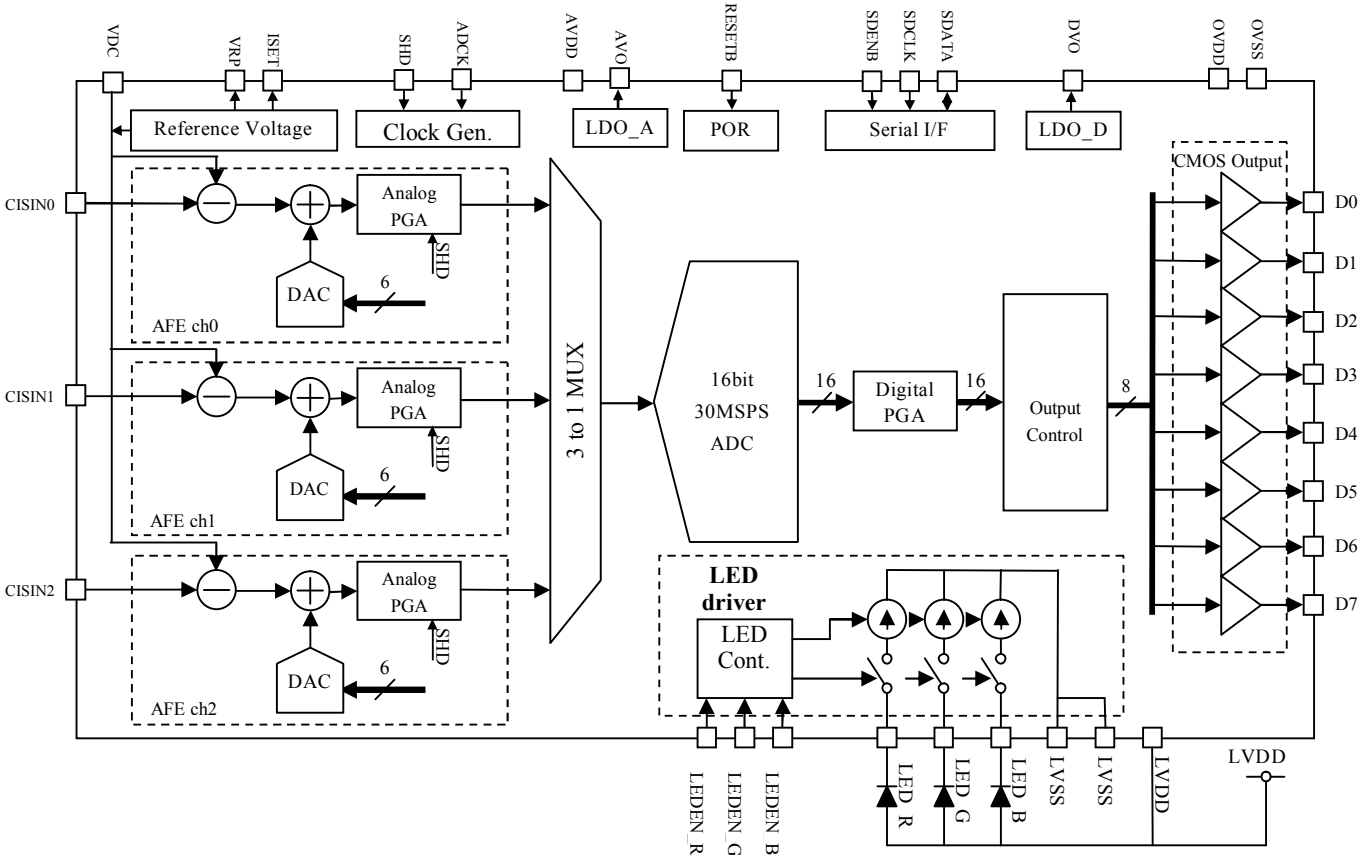


Fig.1 Block diagram

■ Input Block

AK8456 is available for CIS whose polarity is positive. The voltage difference between CISIN0~2 input signal and sensor reference voltage VDC is sampled. VDC is input externally and also is able to generate internally. There are three channel mode and one channel mode. In one channel mode, sensor signal input pin is CISIN0.

■ DAC 6bit DAC

Offset adjust is excused by adding DAC output voltage to input signal. DAC resolution is six bit and output range is ±369mV (typ.). 100mV (max.) out of ±369mV is used to cancel LSI internal offset. Therefore effective range for correcting signal offset is ±269mV (typ.).

■ Sample and Hold Block S/H

The voltage difference between CISIN0~2 input signal and sensor reference voltage VDC is sampled at sample and hold block. Gain at sample and hold block is selected from 0dB and 6dB.

■ Multiplexor MUX

Due to process three channels in a time-division, MUX selects one channel out of three channels in order.

■ ADC

After offset adjust, the ADC convert analog signal level to digital data. The ADC has 16-bit resolution and 30MSPS maximum conversion ratio. The output code is straight binary, 0000h corresponds to black signal and FFFFh corresponds to white signal.

■ Digital PGA

The digital PGA amplifies A/D data. Its gain range is 0dB~18dB and gain resolution is 8bit.

■ Output Control Block

The output control block converts 16-bit width data to two 8-bit width data. Higher 8-bit is output at ADCK rising edge and lower 8-bit is output at ADCK falling edge. Gray code output is possible too by register setting.

■ Reference Voltage Generation Block Reference Voltage

This block generates internal reference voltage VRP, sensor reference voltage VDC and LDO reference voltage.

■ Internal Clock Generation Block Clock Gen

This block generates internal pulses using A/D clock ADCK and sampling pulse SHD.

■ LED Driver Control Block LED Control

This block controls LED switching and LED current. LED current is adjustable from 100% to12.5% by 12.5% step channel independently. 100% current is 67.2mA per channel.

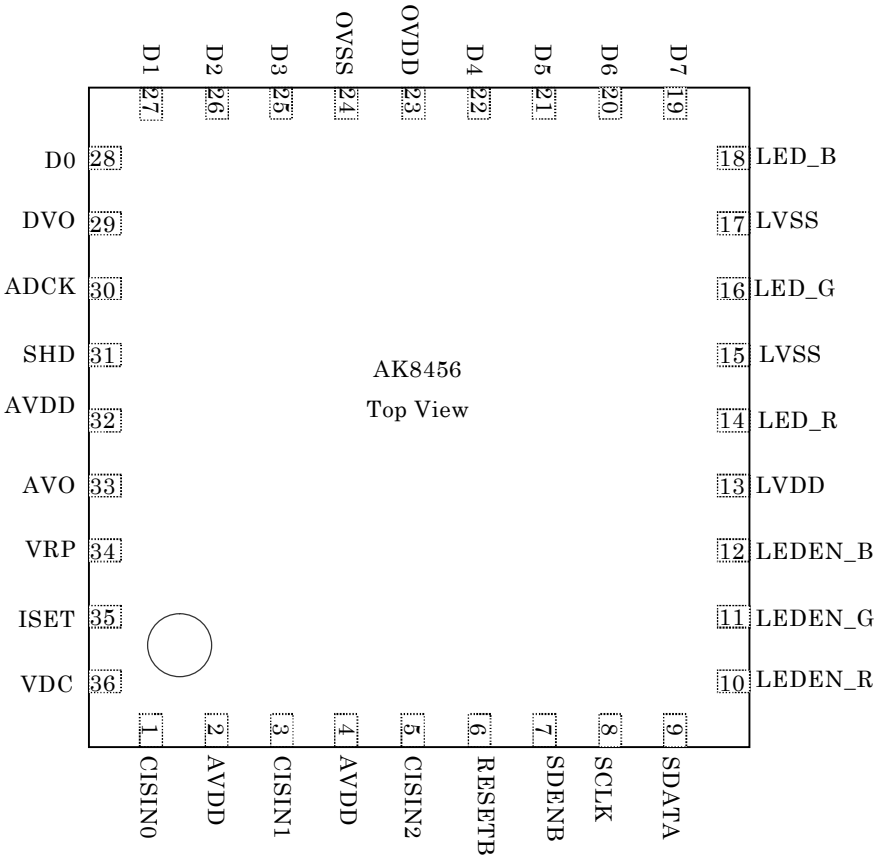
■ Serial Interface Block Serial I/F

Control registers are written and read through 3-wire serial interface.

■ Low Dropout Voltage Regulator LDO

The LDO generate 1.8V supply from 3.3V of AVDD. The 1.8V is used for internal circuit. There are two LDO for analog circuit and digital circuit.

5. Pin allocation and Functions



Note) Connect under side thermal exposed PAD with AVSS.

Fig.2 Pin Layout

■ Pin Functions

No.	Name	IO	Standby (note 2)	Description
1	CISIN0	I	---	Sensor Signal Input
2	AVDD	P	---	Analog Supply
3	CISIN1	I	---	Sensor Signal Input
4	AVDD	P	---	Analog Supply
5	CISIN2	I	---	Sensor Signal Input
6	RESETB	I	---	Reset Input, Active Low Include Pull-up Resistance 100kΩ (typ.)
7	SDENB	I	---	Serial Interface Data Enable
8	SCLK	I	---	Serial Interface Clock Input
9	SDATA	IO	High-Z	Serial Interface Data Input and Output
10	LEDEN_R	I	---	LED_R Control Signal Input Include Pull-down Resistance 50kΩ (typ.)

11	LEDEN_G	I	---	LED_G Control Signal Input Include Pull-down Resistance 50kΩ (typ.)
12	LEDEN_B	I	---	LED_B Control Signal Input Include Pull-down Resistance 50kΩ (typ.)
13	LVDD	P	---	LED Driver Supply (5V)
14	LED_R	O	High-Z	LED Driver Output R
15	LVSS	P	---	LED Driver Ground
16	LED_G	O	High-Z	LED Driver Output G
17	LVSS	P	---	LED Driver Ground
18	LED_B	O	High-Z	LED Driver Output B
19	D7	O	Low	A/D Data Output (note 1) (Upper bit)
20	D6	O	Low	A/D Data Output (note 1)
21	D5	O	Low	A/D Data Output (note 1)
22	D4	O	Low	A/D Data Output (note 1)
23	OVDD	P	---	A/D Data Output Buffer Supply (3.3V)
24	OVSS	P	---	A/D Data Output Buffer Ground
25	D3	O	Low	A/D Data Output (note 1)
26	D2	O	Low	A/D Data Output (note 1)
27	D1	O	Low	A/D Data Output (note 1)
28	D0	O	Low	A/D Data Output (note 1) (Lower bit)
29	DVO	O	1.8V	Digital LDO Output pin (1.8V) Keep DVO open.
30	ADCK	I	---	ADC Clock
31	SHD	I	---	Sampling Clock
32	AVDD	P	---	Analog Supply (LDO Supply)
33	AVO	O	Low	Analog Block LDO Output Voltage Monitor (1.8V) Connect 1μF capacitor between AVO and AVSS.
34	VRP	O	Low	ADC Reference Voltage Connect stabilize capacitor 1μF via AVSS
35	ISET	I	---	Resistance for Reference Current Setting
36	VDC	IO	High-Z	CIS Reference Voltage Connect stabilize capacitor 1μF via AVSS
Tab	AVSS	P	---	Analog Ground

(note 1) Open drain output in cascade output mode

(note 2) Standby is defined as the condition that power down bit NPD=0 after reset.

(note 3) I:Input / O:Output / P:Power supply

6. Absolute Maximum Ratings

AVSS=OVSS=LVSS=0V. All voltages are based on ground.

Item	Symbol	Min.	Max.	Unit	Remarks
Analog Supply	AVDD	−0.3	4.6	V	
Digital Output Buffer Supply	OVDD	−0.3	4.6	V	
LED Driver Supply	LVDD	−0.3	6.2	V	
Input Voltage	VINA	−0.3	AVDD+0.3	V	
Storage Temperature	Tstg	−65	150	°C	

Operation at or beyond these limits may result in permanent damage to the device.

Normal operation is not guaranteed at these extremes.

7. Recommended Operating Conditions

AVSS=OVSS=LVSS=0V. All voltages are based on ground.

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Analog Supply	AVDD	3.0	3.3	3.6	V	
Digital Output Buffer Supply	OVDD	3.0	3.3	3.6	V	
LED Driver Supply	LVDD	4.5	5.0	5.7	V	
Operational Temperature	Ta	0		70	°C	

Normal operation is guaranteed at AVDD voltage = OVDD voltage.

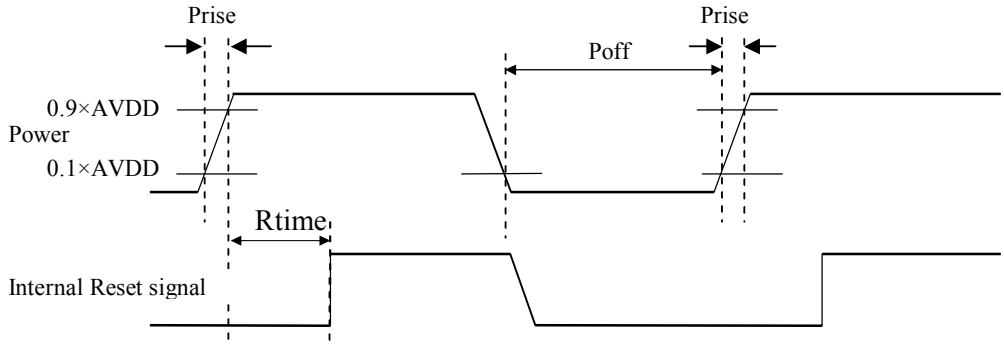
All supplies must be power-up. Don't power off partial supplies for saving consumption.

If LEDD function is unnecessary. LVDD pins can connect VSS level.

8. Electrical Characteristics

■ Reset timing

Fig.3 In case of internal power on reset



(note) When using a power on reset circuit, the RESETB pin must connect the capacity of 0.33µF to AVSS.

(VDD: AVDD=OVDD =3.0~3.6V, Ta=0~70°C)

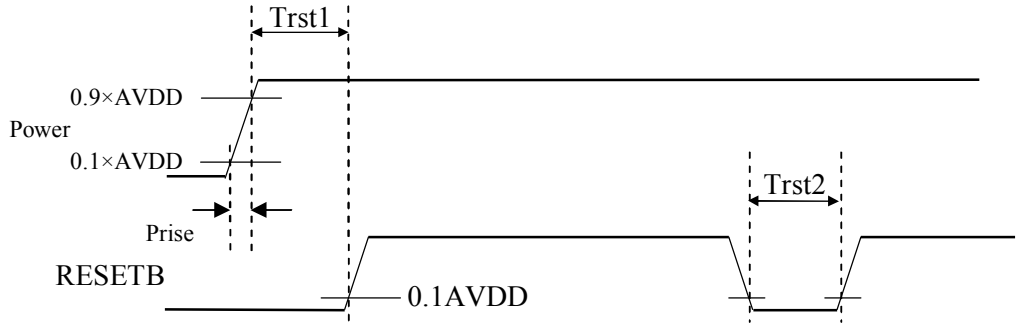
Item	Symbol	Min.	Typ.	Max.	unit	Condition
VDD rise time	Prise	0.01		10	ms	
VDD 0V period	Poff	300			ms	0V peripd
The waiting time of the reset cancellation	Rtime			100	ms	

* Start all powers at the same time.

* When VDD_0V_period can not meet this condition, Because a register isn't reset, this

doesn't work normally. And the over-current may flow through VDD. It is same when using an external reset pin, too.

Fig.4 In case of external power on reset pin



(VDD : AVDD=OVDD=3.0~3.6V, Ta=0~70°C)

Item	Symbol	Min.	Typ.	Max.	unit	Condition
VDD rise time	Prise	0.01			ms	
Reset period 1	Trst1	100			µs	
Reset period2	Trst2	100			µs	

*When RESETB:Low, LDO for AFE power and LDO for digital power are power downed. The time of digital LDO power-off is 6µs. (The time which becomes lower than 20% of 1.8 V)

■ DC Characteristics

(AVDD=OVDD=3.0V~3.6V, Ta= 0~70°C)

Item	Symbol	Pin	Min.	Max.	Unit	Remarks
High Input Voltage	VIH	Note 1,2,3	0.7×AVDD		V	
Low Input Voltage	VIL	Note 1,2,3		0.3×AVDD	V	
High Level output resister	ROH1	Note 4		100	Ω	
Low Level output resister	ROL1	Note 4		100	Ω	
High Output Voltage	VOH	Note 5	0.8×AVDD		V	IOH=−1mA
Low Output Voltage	VOL	Note 5		0.2×AVDD	V	IOL=1mA
Input Leakage	ILKG1	Note 1	−10	10	µA	
Input Leakage	ILKG2	Note 2	−45	10	µA	
Input Leakage	ILKG3	Note 3	−10	90	µA	
Input Leakage	ILKG4	Note 4	−10	10	µA	High-Z
Input Leakage	ILKG5	Note 6	−10	10	µA	
Output Leakage	OLKG	Note 7	−10	10	µA	

(Note1) ADCK, SHD, SCLK, SDATA (Input), SDENB,
(Note2) RESETB
(Note3) LEDEN_R, LEDEN_G, LEDEN_B
(Note4) D0~D7
(Note5) SDATA (Output)

(Note6) CISIN0~2
(Note7) LED_R/G/B (LED Driver OFF)

■ AFE Block Analog Characteristics 1

(Unless other specified, AVDD=OVDD=3.3V, LVDD=5.0V, Ta=25°C, ADCK=30MHz)

Item	Symbol	Conditions	min	typ	max	Unit
Reference Voltage						
Sensor Reference Level	VDCE	External Input Range	0.8		1.2	V
	VDCI1	Internal Voltage	0.9	1.0	1.1	V
	VDCI2	Internal Voltage	1.0	1.1	1.2	V
ADC Reference Voltage	VRP		1.4	1.5	1.6	V
Sample and Hold						
Input Range	VI	S/H Gain=0dB Digital PGA Gain=0dB	1.3	1.5		Vpp
Gain	GSH	S/H Gain=6dB setting	5.5	6.0	6.5	dB
Offset Adjust DAC						
Resolution	DRES				6	bit
Range	DRNG	Equivalent Input Level Positive Direction Negative Direction	 300 −440	 369 −369	 440 −300	 mV mV
Differential nonlinearity	DDNL	DAC code conversion	-1		+1	LSB
Digital PGA						
Maximum Gain	GMAX	Relative to 0dB setting		18		dB
Step Width	GSTA	Monotonicity Guaranteed	0.001	0.07		dB
ADC						
Resolution	RES				16	bit
Differential Non-Linearity	DNL	CISIN~ADC No missing code guaranteed at 12bit accuracy (PGA=0dB)	-1		+1	LSB
Integral Non-linearity	INL	CISIN~ADC 12bit accuracy	−16		16	LSB
Noise, Internal Offset, Cross Talk						
No Signal Noise (Note 1)	NI	Gain=0dB Gain=18dB (S/H=6dB, PGA=12dB)		14 67		LSB_{rms}
Internal Offset (Note 2)	VOFST	Gain=0dB	−50		50	mV
Cross Talk	XTALK	(Note 3) PGA=0dB	-256	±32	256	LSB

■ AFE Block Analog Characteristics 2

These specifications are defined under the condition external parts and their constants are in External Circuit Example. (AVDD=OVDD=3.0～3.6V, LVDD=4.5～5.7V, Ta=25°C, ADCK=30MHz)

Current consumption						
Normal operation	AVDD OVDD LVDD	(note 4) (note 5) (note 6)		37.4 8.6 6.2	51.2 25.5 8.4	mA mA mA
Stand By	ISTB			2.2	3	mA

These specifications are defined under the condition external parts and their constants are in External Circuit Example.

(Note1) No signal noise is defined as sigma(σ) of ADC code deviation under no input signal.

(Note2) When no input signal is applied, ADC code changes from 0000h to 0001h between offset DAC −50mV and offset DAC 50mV. The offset DAC cancels this internal offset as well as signal offset. Thus adjust range for input signal offset is reduced by the internal offset.

(Note3) ADCK=30MHz, 3ch, PGA Gain of all channel is minimum. Cross talk is defined, as change of output code when measured channel input is fixed and all other channel inputs is full-scale – 2dB step signal.

(Note4) ADCK=30MHz, Input -2dB of 1.5Vpp sine wave, 1MHz signal to three channels.

(Note5) Load Capacitance10pF

(Note6) @ LED_R=100%, LED_G=25%, LED_B=25% setting (except LED drive current)

■ LED Driver Analog Characteristics

(Unless otherwise specified, AVDD=OVDD=3.3V, LVDD=5.0V, Ta=0°C~70°C, ADCK=30MHz)

Item	Min.	Typ.	Max.	Unit	Remarks
Maximum LED Current per Channel	60.5	67.2	73.9	mA/ch	ISET Resistance=8.2kΩ LED_R/G/B Pin Voltage=2.0V
Total Maximum LED Current		100.8		mA	
LED Current Setting Accuracy	−5		5	%	LED_R/G/B Pin Voltage=2.0V
Dependence of LED Current on LED_R/G/B Pin Voltage	−2.5		2.5	%	LED_R/G/B Pin's Reference Voltage = 2.0V
LED_R/G/B Pin Voltage	0.3		LVDD −1.1	V	Driving Current

■ Switching Characteristics

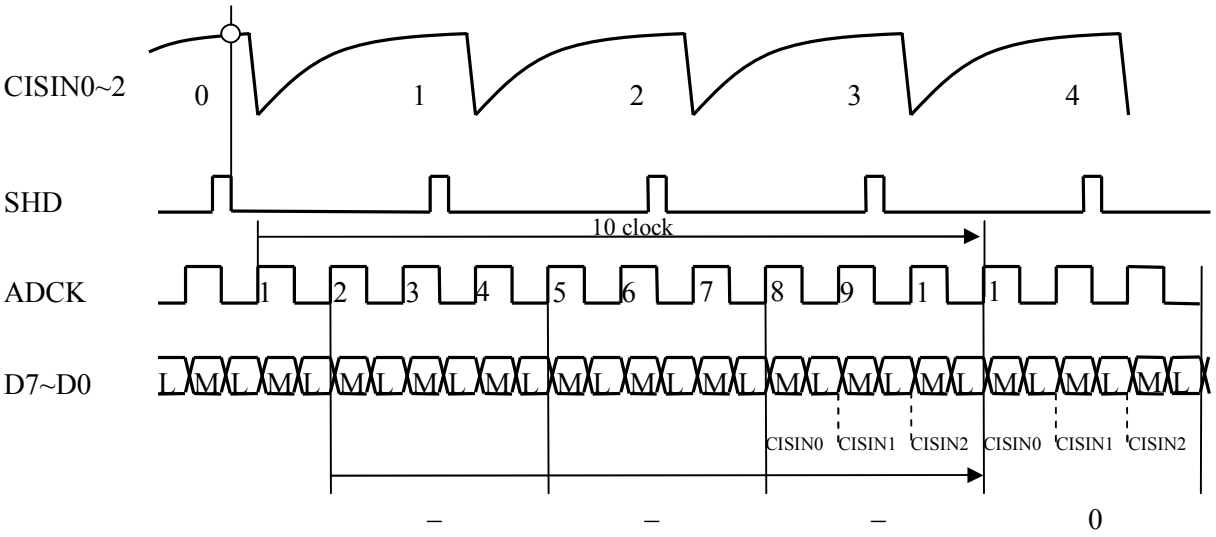
(Unless otherwise specified, AVDD=OVDD=3.0V~3.6V, Ta=0~70°C)

No.	Item	Pin	Min.	Typ.	Max.	Unit	Remarks
1	ADCK Cycle (T)	ADCK	33.3		2000	ns	
2	ADCK Low Width	ADCK	15			ns	
3	ADCK High Width	ADCK	15			ns	
4	SHD Cycle	SHD		3 6 1		clocks	3ch Normal Output 3ch Cascade Output 1ch Mode
5	SHD Pulse Width	SHD	8			ns	
6	SHD Setup Time (to ADCK↑)	SHD	2			ns	
7	SHD Delay Time (to ADCK↓)	SHD	10			ns	
8	SHD Aperture Delay	SHD		2.5		ns	
9	D0~7 Delay (to ADCK↑↓)	D7~D0	2		10	ns	Hold, Setup C_L=10pF (Note 1)
10	Pipeline Delay (ADCK unit)	D7~D0		11		clocks	3ch Mode 1ch Mode
11	SHD="H" Prohibited Region (to First ADCK↑ after SHD↓)	SHD	1T+10 4T+10 10			ns	3ch Normal Output 3ch Cascade Output 1ch Mode
12	D0~7 Enable Time	D7~D0	0		8.2	ns	Cascade Output
13	D0~7 Disable Time	D7~D0	2.4		7.2	ns	Cascade Output

These specifications refer to point crossing levels that defined in DC characteristics.

(Note1) Refer to points ADCK, D7~D0 cross 50% of supply voltage. This delay is under ADCK rise time tr and fall time tf are 1.65ns.

3ch Input, Normal Output



In D7~D0, L means lower 8 bits, M means upper 8bits.

Fig. 5 Whole Timing

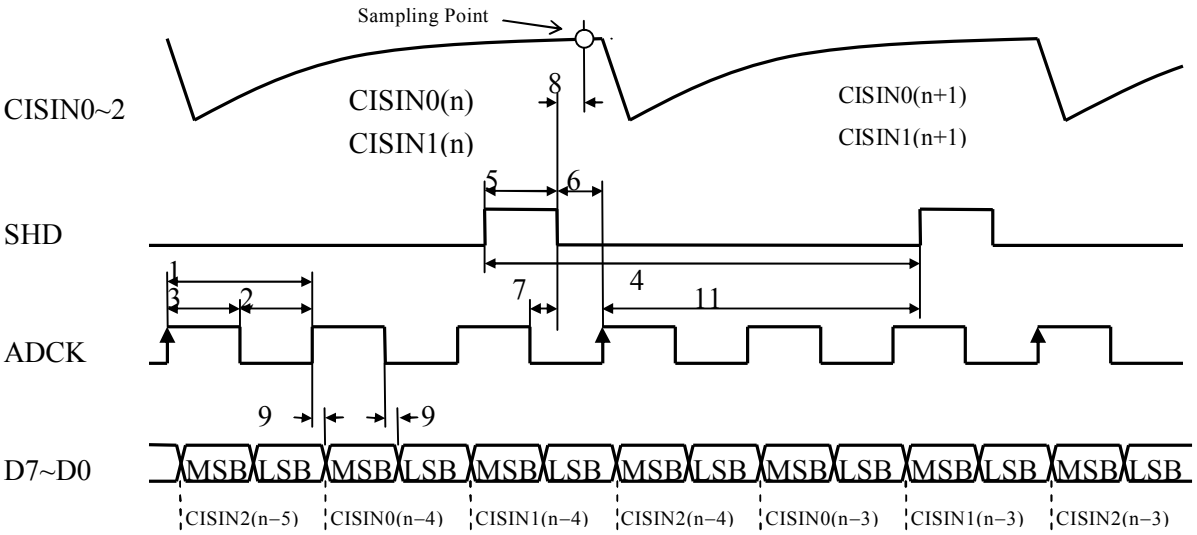


Fig.6 Details

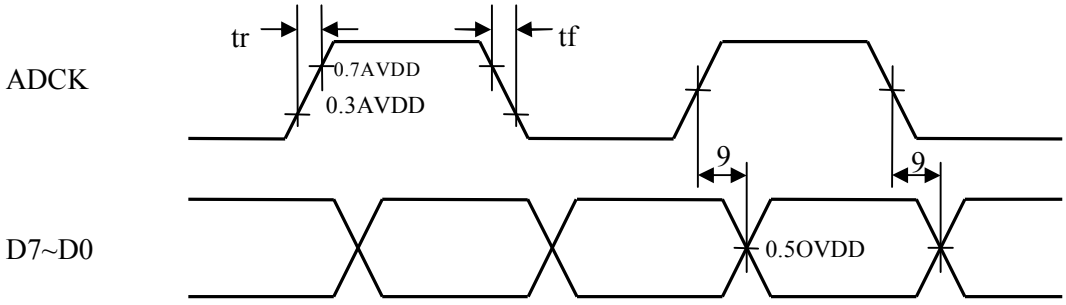
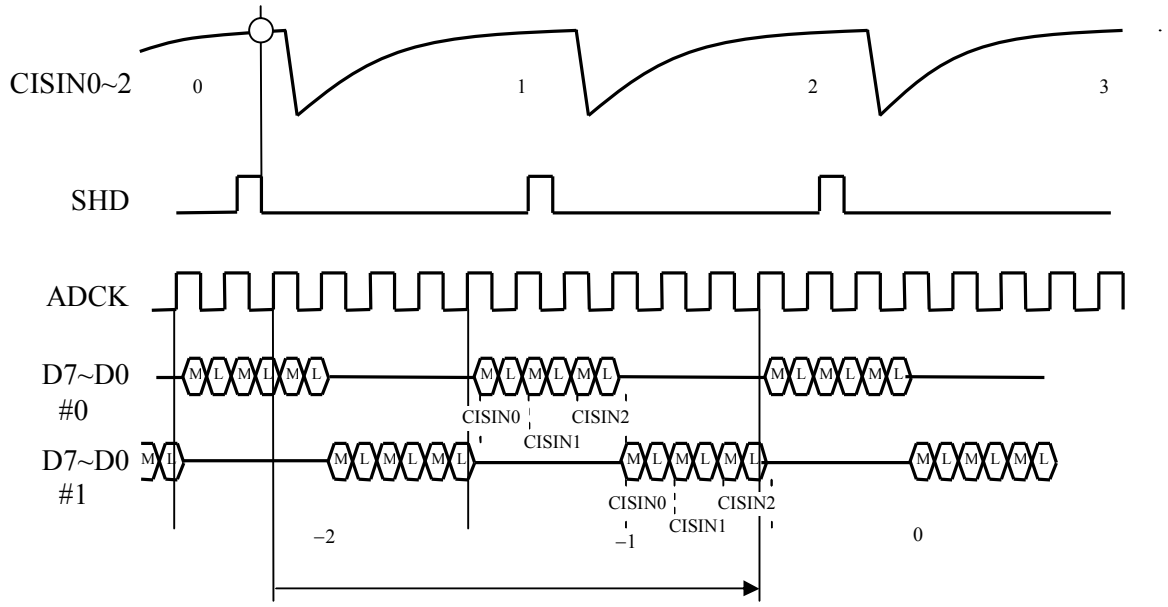


Fig.7 D0~D7 Delay

3ch Input, Cascade Output



In D7~D0, L means lower 8 bits, M means upper 8bits.

Fig.8 Whole Timing

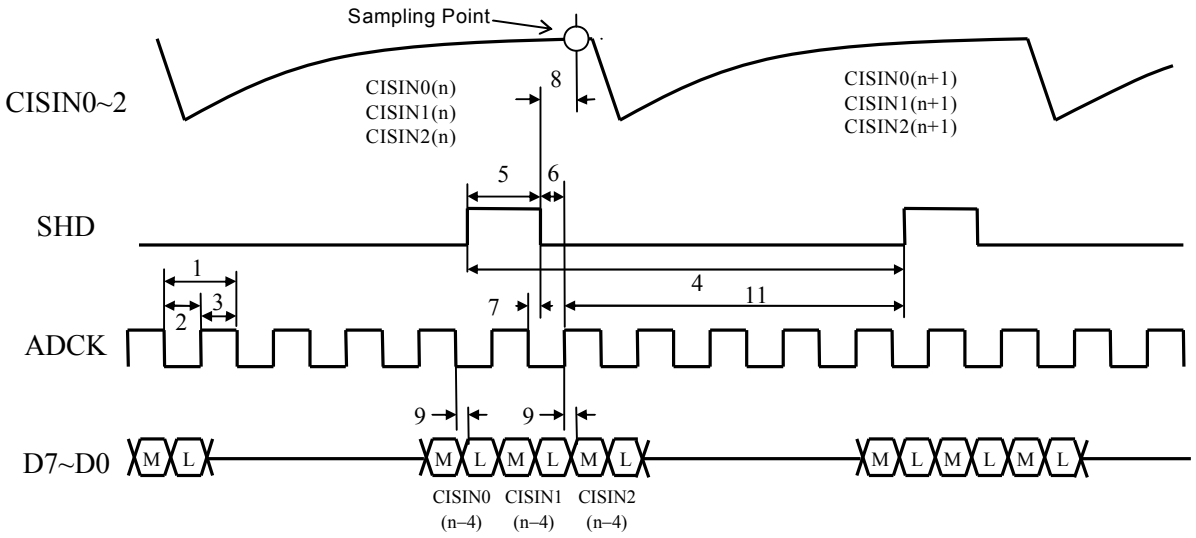


Fig.9 Details

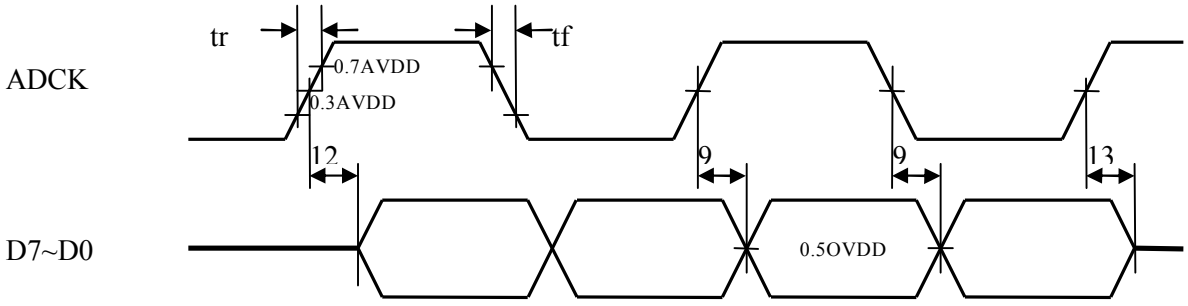
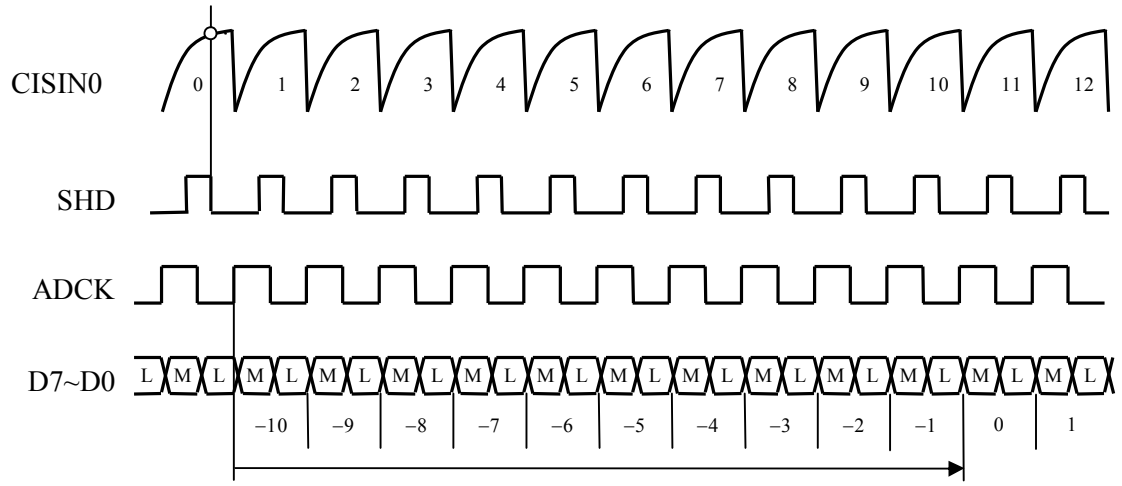


Fig.10 D0~D7 Delay

1ch Input



In D7~D0, L means lower 8 bits, M means upper 8bits.

Fig.11 Whole Timing

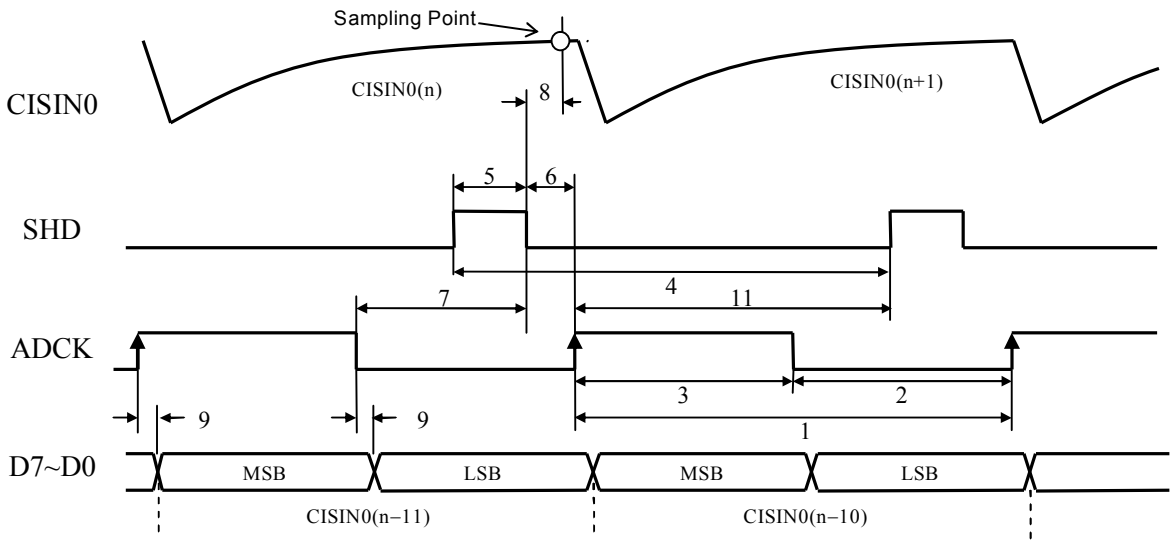


Fig.12 Details

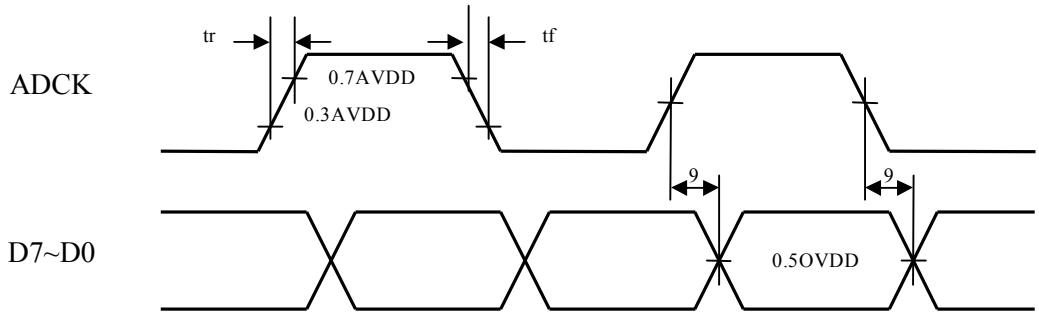


Fig.13 D0~D7 Delay

■ Serial Interface Switching Characteristics

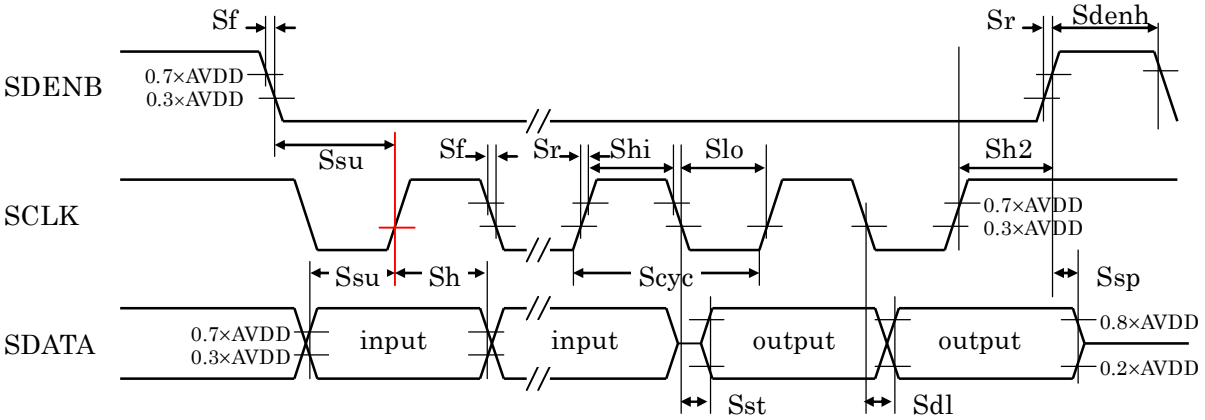


Fig.14 Serial Interface Timing

(Unless otherwise specified, AVDD=OVDD=3.0V~3.6V, Ta=0~70°C, C_L=10pF)

Item	Symbol	Condition	min.	typ.	max.	Unit
Clock Cycle	Scyc				10	MHz
Clock High Width	Shi	Above 70% of AVDD	40			ns
Clock Low Width	Slo	Under 30% of AVDD	40			ns
Setup Time (to SCLK↑)	Ssu		40			ns
Hold Time (to SCLK↑)	Sh		40			ns
SDENB Hold Time (to SCLK↑)	Sh2		80			ns
Data Enable Delay (to SCLK↓)	Sst	High-Z→Data Out	0		30	ns
Data Output Delay (to SCLK↓)	Sdl		0		30	ns
Data Disable Delay (to SDENB↑)	Ssp	Data Out→High-Z	0		30	ns
SDENB High Width	Sdenh	Above 70% of AVDD	40			ns
Rise Time	Sr	30%→70% of AVDD			10	ns
Fall Time	Sf	70%→30% of AVDD			10	ns

■ LED Driver Switching Characteristics

(Unless otherwise specified, AVDD=OVDD=3.0V~3.6V, LVDD=4.5V~5.7V, Ta=0~70°C)

Item	Symbol	Conditions	min.	typ.	max.	Unit
LEDEN_R/G/B Setup Time (to SHD↓)	tlens		15			ns
LEDED_R/G/B Hold Time (to SHD↓)	tlenh		15			ns

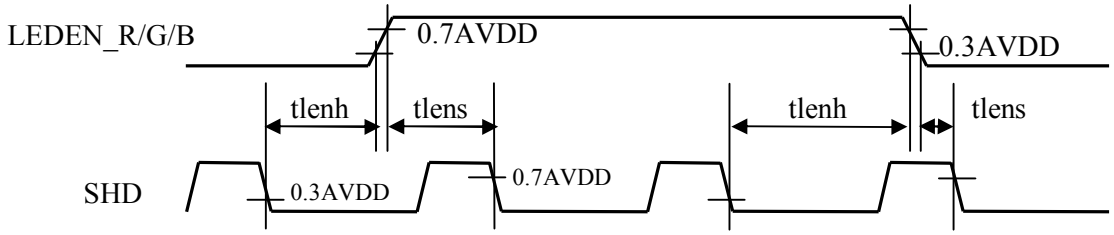


Fig. 15 LED driver switching characteristics

(Unless otherwise specified, AVDD=OVDD=3.0V~3.6V, LVDD=4.5V~5.7V, Ta=0~70°C)

Item	Symbol	Conditions	min.	typ.	max.	Unit
LED Current Rise Time	tlon			10		μs
LED Current Fall Time	tloff			10		μs

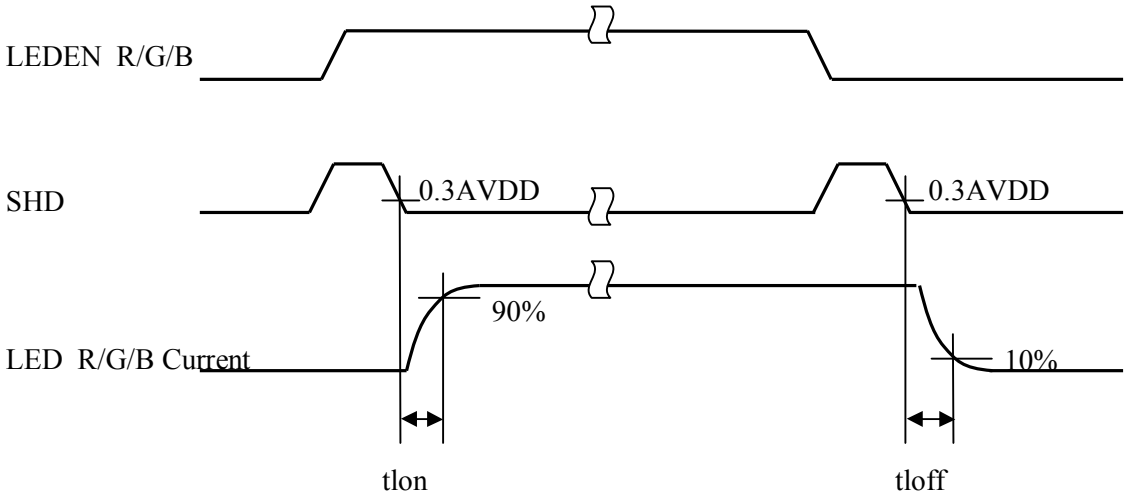


Fig. 16 LED current timing

LED drivers are switched in LEDEN_R/G/B those are synchronized with SHD falling edge. Therefore, if it can't meet setup time or hold time of LEDEN_R/G/B, LED lighting time will be 1~2 pixels change.

■

9. Functional Description

■ Start Up

There is no restriction on order of turning on AVDD, OVDD and LVDD.

Please take a reset by hold RESETB low level when the power AVDD is turned on. LEDEN_R/G/B must be low level during RESETB rises. User can access to the registers after wait time that are shown in followed figures from power-up.

Fig.17 Not Use Power on Reset

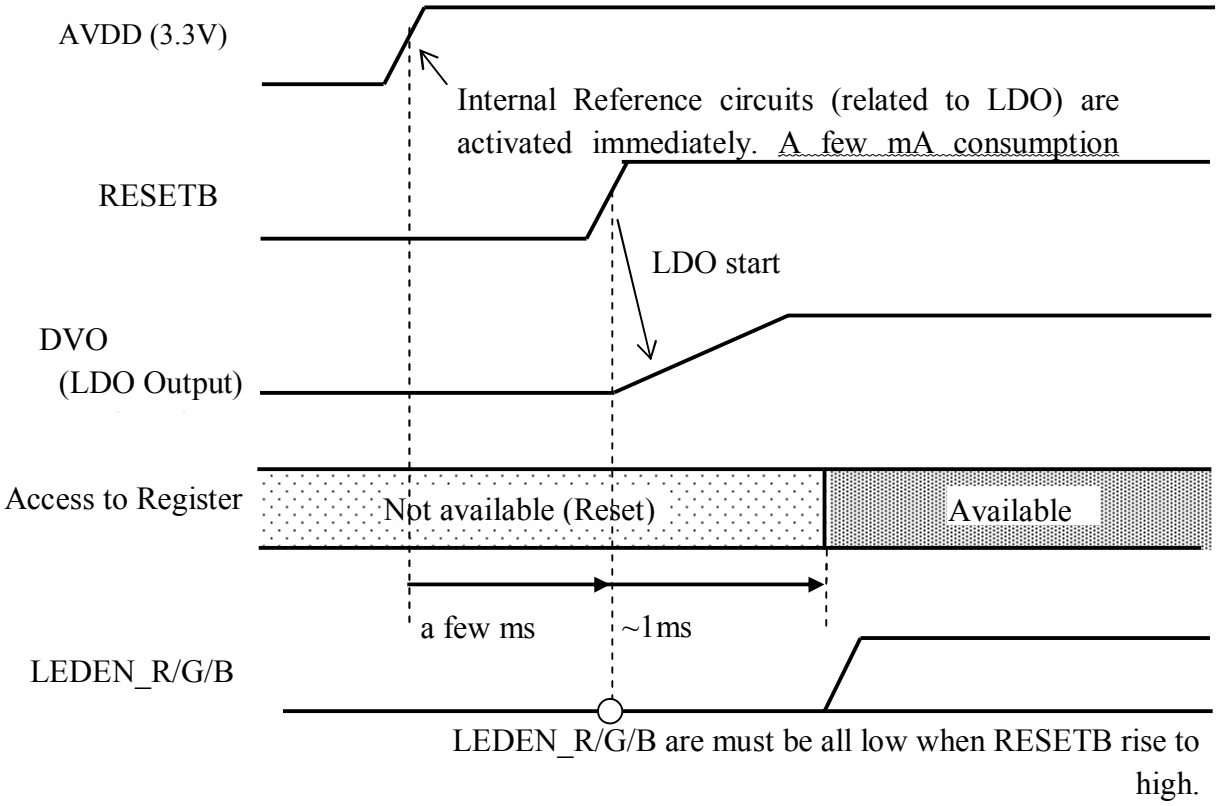
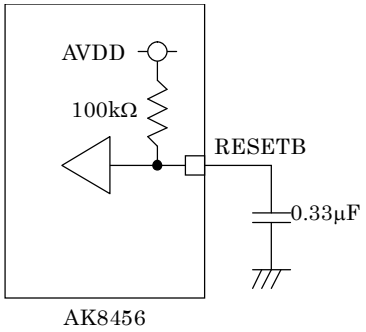
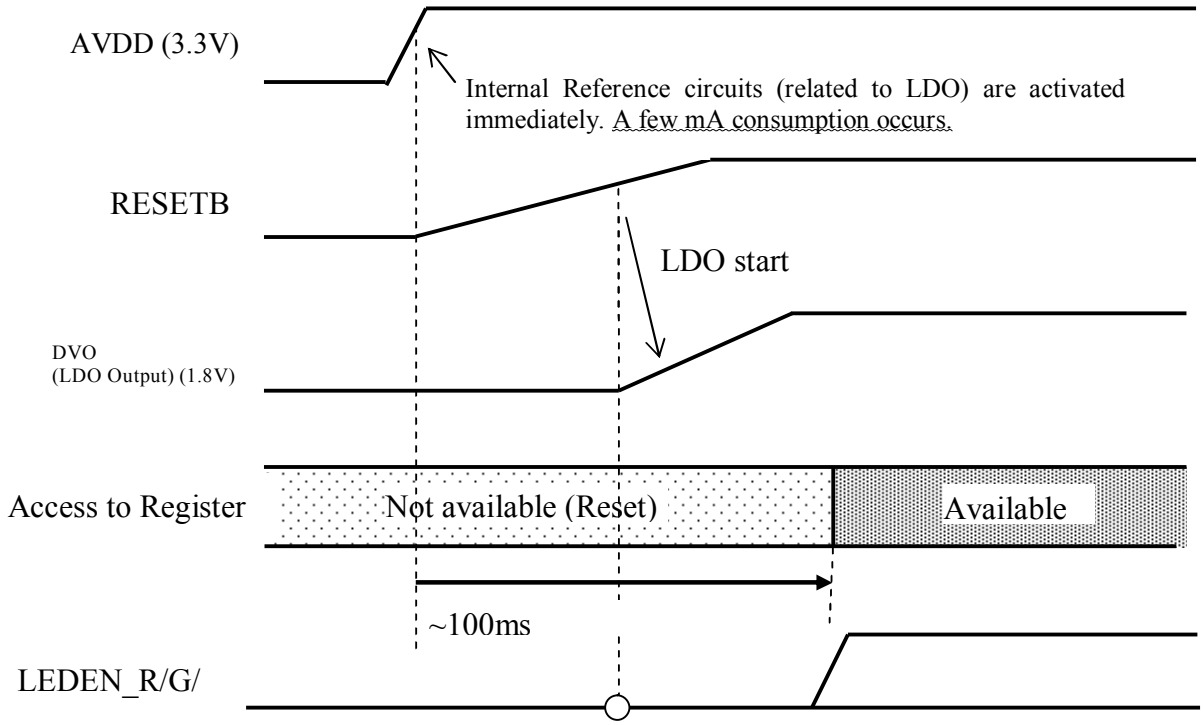


Fig.18 Use Power on Reset



Power on reset circuit is composed by pull-up resistance of RESETB and external capacitor. When external capacitor is 0.33μF, AVDD rise time must be less than 10ms to reset exactly. Staircase-like supply voltage rising is not allowed.

Fig.19 Power on Reset timing



LEDEN_R/G/B are must be all low when RESETB rise to high.

When down AVDD to 0V, RESETB level does not became 0V immediately because of charge remaining in RESETB external capacitor. If up AVDD again before RESETB becoming 0V, power on reset does not carry out. The time AVDD is 0V must be longer than 300ms for exact power on reset at re-power up AVDD.

Please control the RESETB from outside without the use of a power-on reset if the above conditions are not met. During power up AVDD, hold RESETB low level. Then raise RESETB to high level.

■ Serial Interface

Control registers are accessed through serial interface. The control registers are readable.
If SDENB is low, it is possible to access registers. Input address and data into SDATA. SDATA is captured by SCLK rising edge.

Write

The first bit of SDATA is 0, data is written to register. From second bit to fourth bit must be 0. From fifth bit to eighth bit are address bits. The fifth bit is most significant bit of address. From ninth bit to sixteenth bit are data bit.

Data is written into register by rising edge of SDENB. If rising edge of SCLK is less than sixteen, data isn't written into register. If rising edge of SCLK is more than seventeen, front sixteen bits are effective.

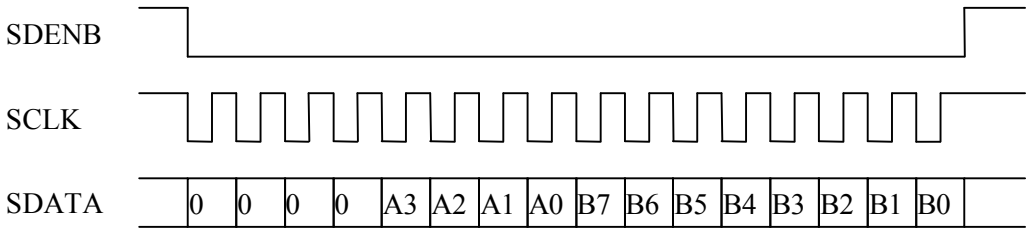


Fig.20 Write to Register

Read

The first bit of SDATA is 1, data is read from register. From second bit to fourth bit must be 0. From fifth bit to eighth bit are address bits. The fifth bit is most significant bit of address. Data is output from the SCLK falling after SCLK rising incorporating an eighth bit. SDATA pin is used as an input again if SDENB become high level. If there is a SCLK 17 or more times, read data after the B0 is output is 0.

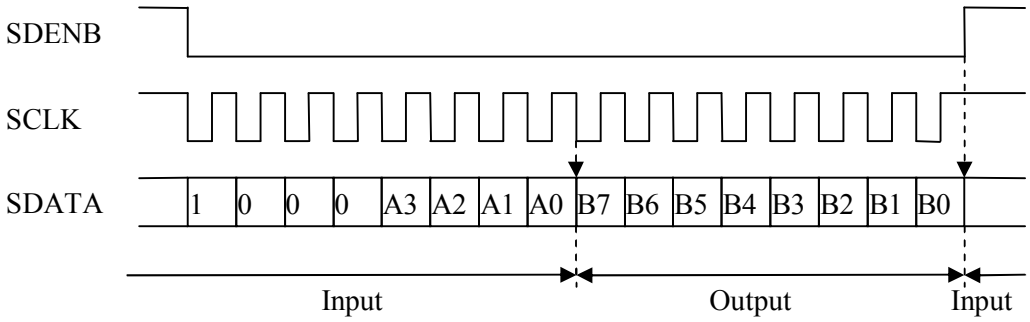


Fig.21 Read from Register

■ CIS Signal Input Channel Number Select

There are 3-channel mode and 1-channel mode as input channel number. Input channel number is selected by register. In 1-channel mode, signal is input to CISIN0. At this time, CISIN1 and CISIN2 can be connected to AVSS, or opened, or input dummy signal. Sample and hold circuit and DAC of not used channels are power down.

Frequency of ADCK in 3-channel mode is three times the pixel frequency per channel. In 1-channel mode, ADCK frequency is equal the pixel frequency.

■ CIS Reference Voltage

It is able to select to use internal voltage or to use externally input voltage as sensor reference voltage by register. Input range of external voltage is from 0.8V to 1.2V. Internal voltage is 1.0V (typ.) or 1.1V (typ.).

■ Offset Adjustment

Offset adjustment is done by adding DAC output voltage to sensor signal. Resolution of DAC is six bit, range is ±369mV(typ.)/300mV(min.) in equivalent input voltage. 50mV (max.) out of ±369mV is used to cancel LSI internal offset. Therefore effective range for correcting signal offset is ±319mV(typ.)/250mv(min.).

The equivalent input voltage does not change even if set 6dB gain at sample and hold block.

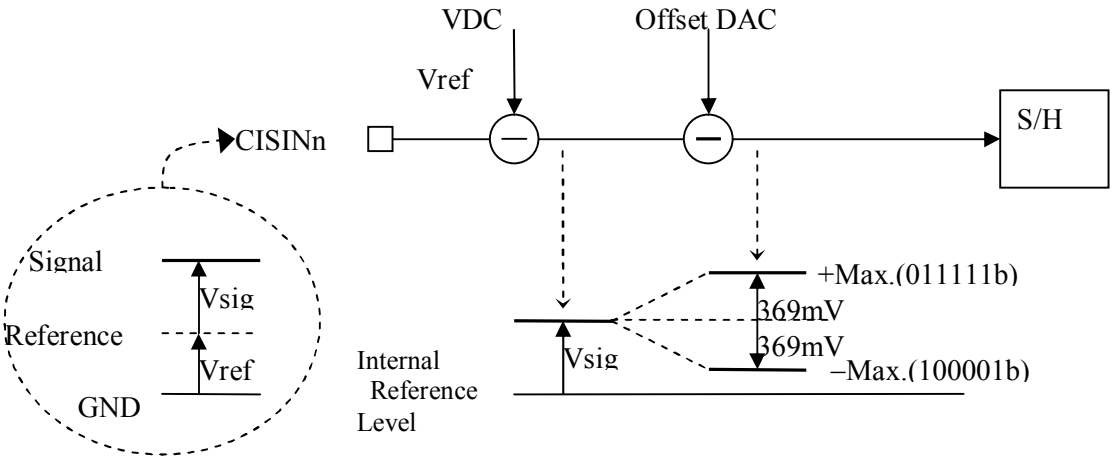


Fig.22 Offset adjustment

■ Sampling

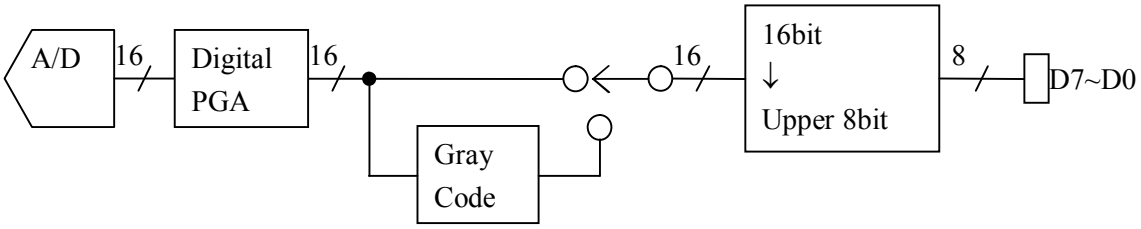
Sensor signal are sampled at SHD falling edge.

■ Gain Adjustment

It is possible to amplify signals at sample and hold block. And it is possible to amplify A/D output code by digital PGA. Gain of digital PGA is from 0dB to 18dB. Its resolution is 8bit.

■ Output Format

Output Formal is straight binary. Gray code output is possible too.



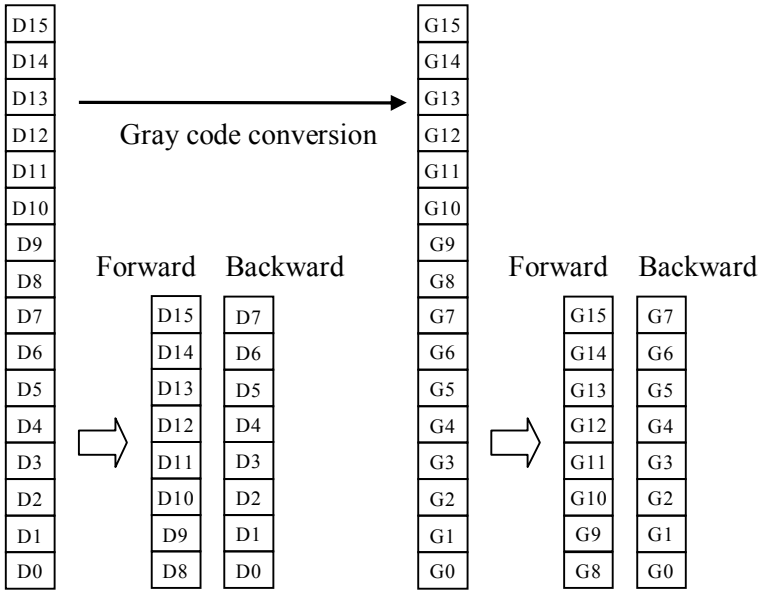


Fig.23 Output format

■ LED Driver

LED Driver controls LED current RGB independently. LED must be connected as anode common. If LEDEN_R/G/B are high level, LED current are driven. If LEDEN_R/G/B are low level, LED current are stopped. LEDEN_R/G/B are synchronized once by SHD internally. Therefore if SHD is not input, LEDEN_R/G/B are not effective.

■ LED Current Adjustment

The LED current can be adjusted in increments of 8.4mA to 67.2mA from 8.4mA channel independently.

■ LED Current Limit

AK8456 LED driver current limitation is 100.8mA (total:150% setting). With the combination with "LEDEN_R/G/B pin logic" and LED drive current setting register value, in case of the combination that the total of the current amount to flow through at the same time exceeds 150%(100.8 mA), the LED drive current doesn't flow. For example, when making "LEDEN_R/G/B" active at the same time and when the total of the LED drive current set value exceeds 150%(100.8 mA), the LED drive current doesn't flow. On the other hand, when making "LEDEN_R/G/B" active individually, the current flows.

■ Cascade Output Mode

It is possible that connect two AK8456's output pins to same 8bit bus by cascade output mode. The cascade output mode is available only in 3-channle input mode. It becomes the normal output regardless of the cascade mode register setting when the channel 1 input. If use cascade mode, please release the power-down after setting the device ID and cascade mode register.

Select the cascade mode in the register and set 0 in ID register of one and set 1 in ID register of the other. Device of ID0 outputs the data before, ID1 devices will output the data then refer to SHD pulse. D7~D0 become high impedance when these pins don't output A/D data. D7~D0 are open drain output in cascade mode. Please connect pull-up resistance to each data output pin. Maximum sampling rate in cascade mode is 5MSPS/ch.

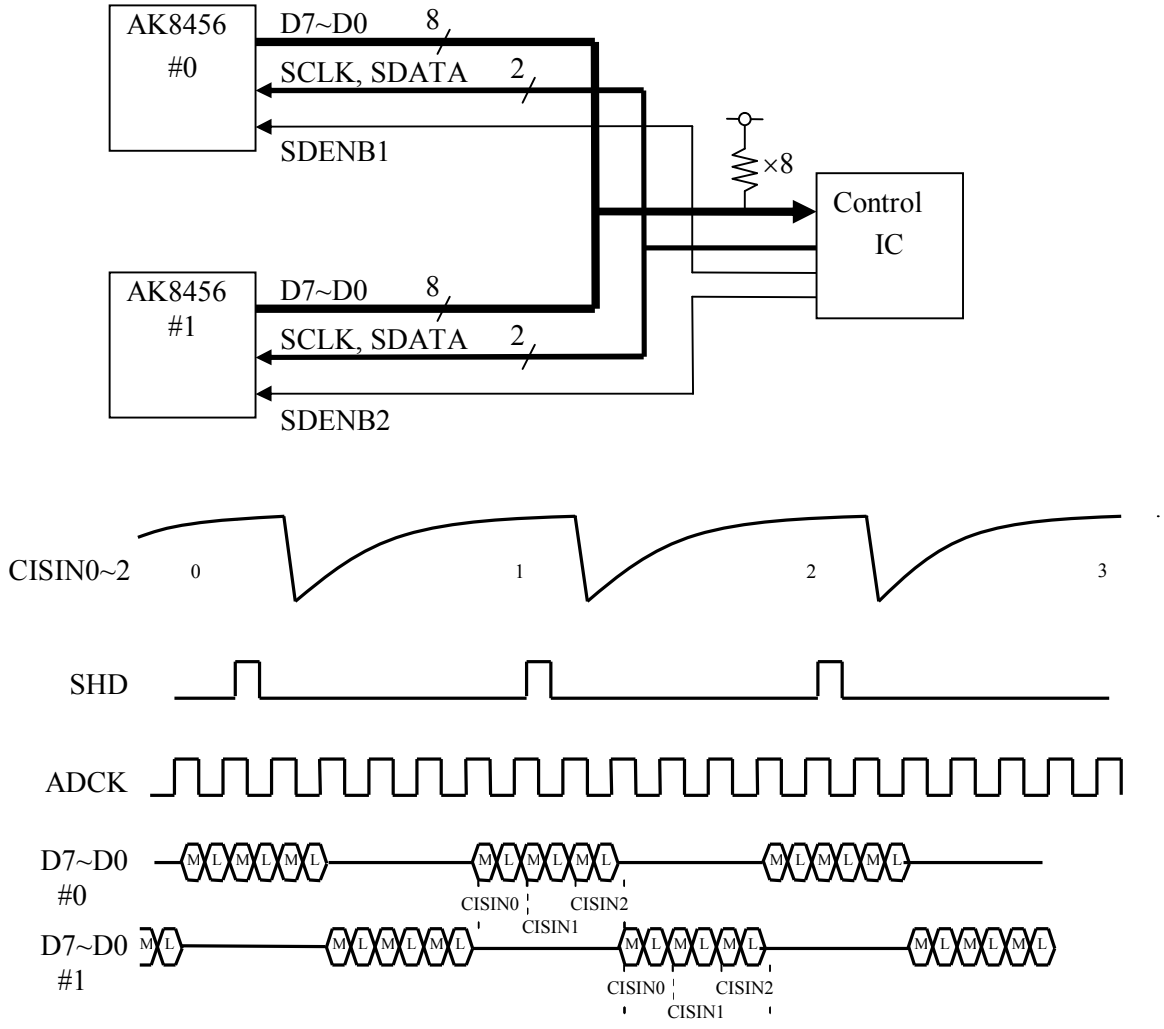


Fig.24 Cascade mode explanation

10. Register Map

Adrs	Register Name	Function
0h	CNTRL1	Operation Control 1 (Related to Input Stage)
1h	OFST0	CISIN0 Offset Setting
2h	OFST1	CISIN1 Offset Setting
3h	OFST2	CISIN2 Offset Setting
4h	GAIN0	CISIN0 Gain Setting
5h	GAIN1	CISIN1 Gain Setting
6h	GAIN2	CISIN2 Gain Setting
7h	CNTRL2	Operation Control 2 (Related to Output Stage)
8h	ISELR	LED_R Current Setting
9h	ISELG	LED_G Current Setting
0Ah	ISELB	LED_B Current Setting

** Register-address 0Bh-0Fh is an access-inhibit.

** When writing an undefined bit, write 0.

Adrs	Name	B7	B6	B5	B4	B3	B2	B1	B0
0h	CNTRL1	NPD	SHG0	SHG1	SHG2	---	VDCO	VDCSEL	CHN
	Default	0	0	0	0	0	0	0	0

■ Address 0h B7 Power-down Setting

NPD	Operation
0	Power-down
1	Normal Operation

Both of AFE block and LED driver power-down. LDO for analog block does not power –down.

■ Address 0h B6 CISIN0 Sample and Hold Gain

■ Address 0h B5 CISIN1 Sample and Hold Gain

■ Address 0h B4 CISIN2 Sample and Hold Gain

SHG0/1/2	Gain at Sample and Hold Block
0	0dB
1	6dB

■ Address 0h B2 CIS Reference Voltage Source Select

VDCO	CIS Reference Voltage Source
0	External
1	Internal (Output to VDC pin)

■ Address 0h B1 CIS Internal Reference Voltage Select

VDCSEL	CIS Reference Voltage
0	1.0V
1	1.1V

■ Address 0h B0 Input Channel Number Select

CHN	Channel Number
0	3 Channels
1	1 Channel (Input to CISIN0)

** When writing an undefined bit, write 0.

Adrs	Name	B7	B6	B5	B4	B3	B2	B1	B0
1h	Offset 0	−	−	OFST0					
2h	Offset 1	−	−	OFST1					
3h	Offset 2	−	−	OFST2					
	Default	0	0	0	0	0	0	0	0

■ Address 1h B5~B0 CISIN0 Offset Setting

■ Address 2h B5~B0 CISIN1 Offset Setting

■ Address 3h B5~B0 CISIN2 Offset Setting

OFST0/1/2	Offset Voltage
01 1111	+369mV
01 1110	+357.1mV
:	
00 0001	+11.9mV
00 0000	±0mV
11 1111	−11.9mV
:	
10 0010	−357.1mV
10 0001	−369mV
10 0000	Inhibit

When set minus value, signal magnitude becomes smaller. When set plus value, signal magnitude becomes larger.

When −11.9mV setting, image signal decrease 11.9mV.

** When writing an undefined bit, write 0.

Adrs	Name	B7	B6	B5	B4	B3	B2	B1	B0
4h	DPGA 0	DGAIN0							
5h	DPGA 1	DGAIN1							
6h	DPGA 2	DGAIN2							
	Default	0	0	0	0	0	0	0	0

- Address 4h B7~B0 CISIN0 Digital PGA Gain Setting
- Address 5h B7~B0 CISIN1 Digital PGA Gain Setting
- Address 6h B7~B0 CISIN2 Digital PGA Gain Setting

DGAIN0/1/2	Digital PGA Gain
0000 0000	0dB
0000 0001	
:	
1111 1110	18dB
1111 1111	Inhibit

$$Gain(x) = 18x / 254 \text{ [dB]} \quad x=0\sim254$$

Adrs	Name	B7	B6	B5	B4	B3	B2	B1	B0
7h	CNTRL2	---	---	CASC	DEVID	---	DRV	---	FORMAT
	Default	0	0	0	0	0	0	0	0

■ Address 7h B5 Cascade Output Mode Select

CASC	Data Output
0	Normal Output
1	Cascade Output

If use cascade output mode, power down mode must be released after setting cascade output mode select register and device ID select register.

■ Address 7h B4 Device ID for Cascade Output Mode

DEVID	Device ID
0	0
1	1

■ Address 7h B2 Output Buffer Ability Select

DRV	Output Buffer Ability
0	Normal
1	1/3

If set DRV=1 then output buffer ability of D7~D0 became 1/3 of normal.

■ Address 7h B0 Output Format Select

FORMAT	Output Format
0	Straight Binary Code
1	Gray Code

** When writing an undefined bit, write 0.

Adrs	Name	B7	B6	B5	B4	B3	B2	B1	B0
8h	Current R	---	---	---	---	---	ISELR		
9h	Current G	---	---	---	---	---	ISELG		
Ah	Current B	---	---	---	---	---	ISELB		
	Default	0	0	0	0	0	0	0	0

- Address 8h B2~B0 LED_R Current Setting
- Address 9h B2~B0 LED_G Current Setting
- Address Ah B2~B0 LED_B Current Setting

ISELR/G/B	LED Current
000	8.4mA
001	16.8mA
:	:
110	58.8mA
111	67.2mA

$$I(x) = 8.4(x+1)\,[\mathrm{mA}] \qquad x=0\sim7$$

** When writing an undefined bit, write 0.

11. External Circuit Example

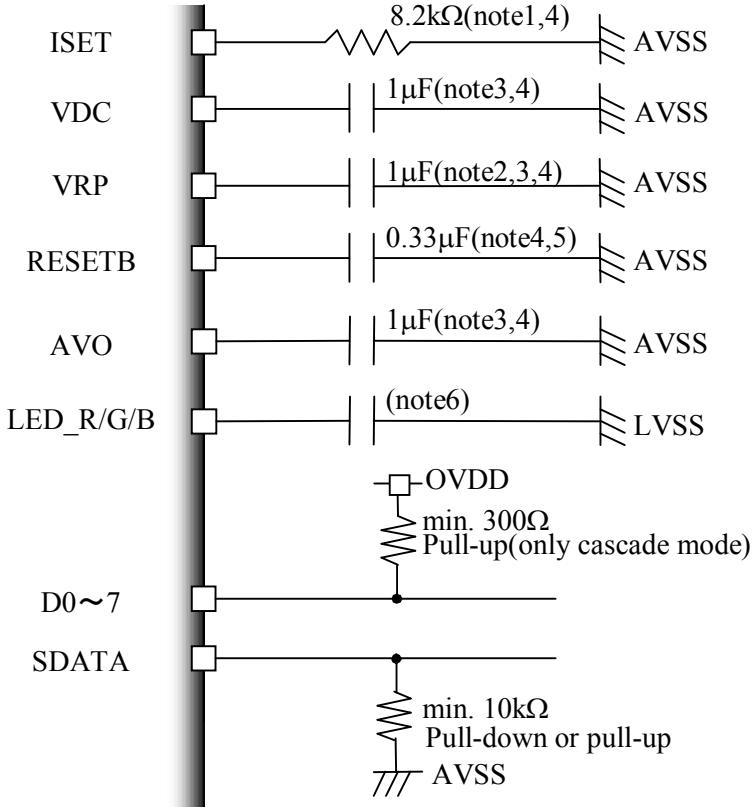


Fig.25 Reference voltage:D0~ 7,SDOUT,AVO,LED_R/G/B

note1）The resistance precision is ±3 % (including thermal-characteristic)
note2）The capacitance precision is ±50 % (including thermal-characteristic)
note3）Connect them near the pin.
note4）Keep off them from clock line(noise source) and so on.
note5）When not using a power on reset, it is unnecessary, connecting.
note6) Be careful that the voltage of the LED_R/G/B-pin doesn't exceed "LVDD+0.3V" , by the influence of the overshoot. In case of ,the overshoot is big and the LED wiring is long, put a capacitor between " the LED_R/G/B terminal " and the grand.

*VDD：OVDD, AVDD, LVDD
*VSS：OVSS, AVSS, LVSS
Note7） Each power pin need this Cap.

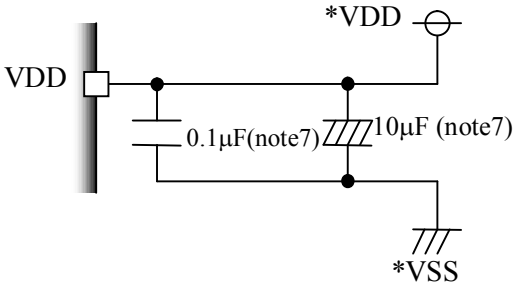


Fig.26 Power pins

■ Connection of Cascade Output Mode

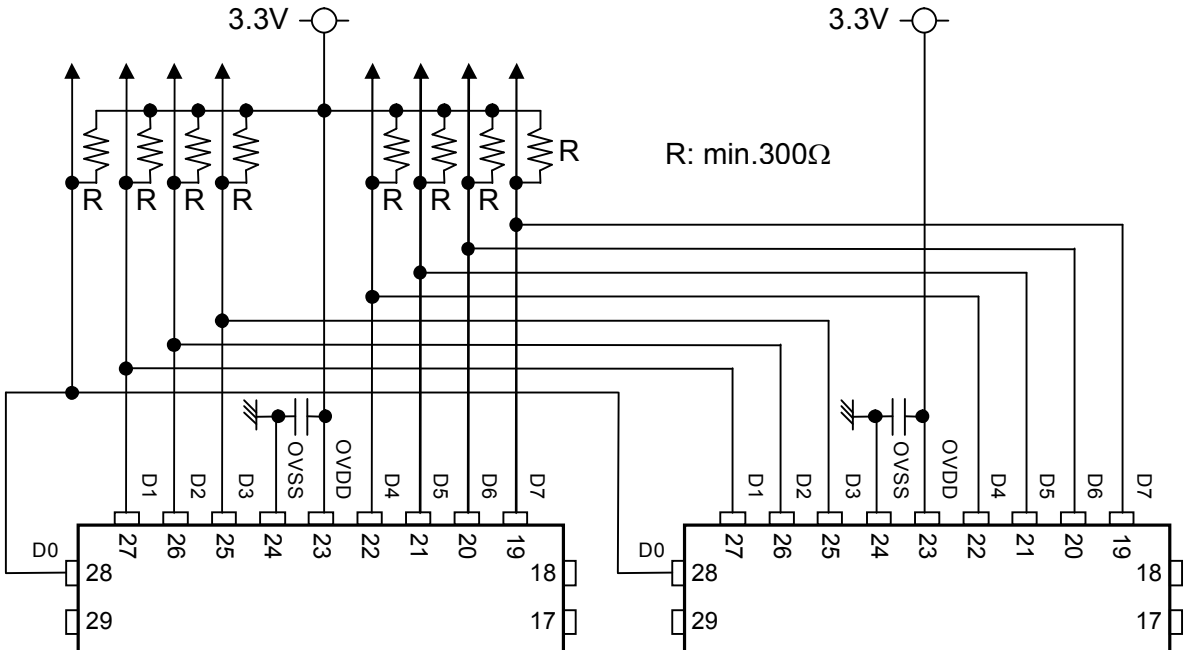


Fig.27 Cascade mode connection example

12. Package

■ Dimensions

(36pin QFN 5mm×5mm, Pin Pitch 0.4mm)

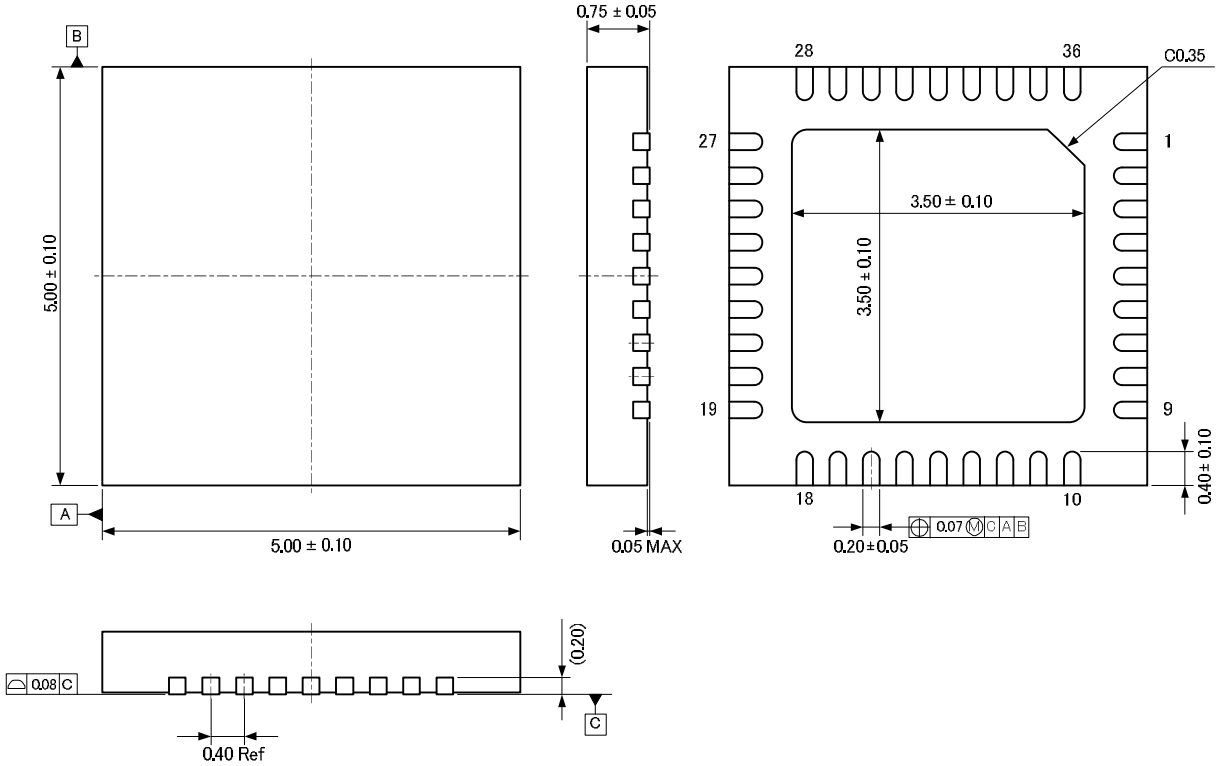
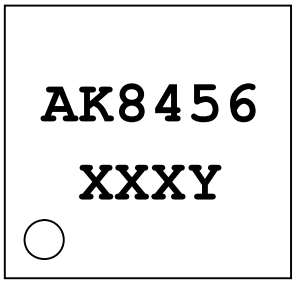


Fig.28 Package dimensions

■ Marking

1. Marketing Code :AK8456
2. Date Code :XXX Week Number
   :Y Control Code



Note) Marking is preliminary

Fig.29 AK8456 Marking

13. Important Notice

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