



FTSM104A

OPERATIONAL AMPLIFIERS

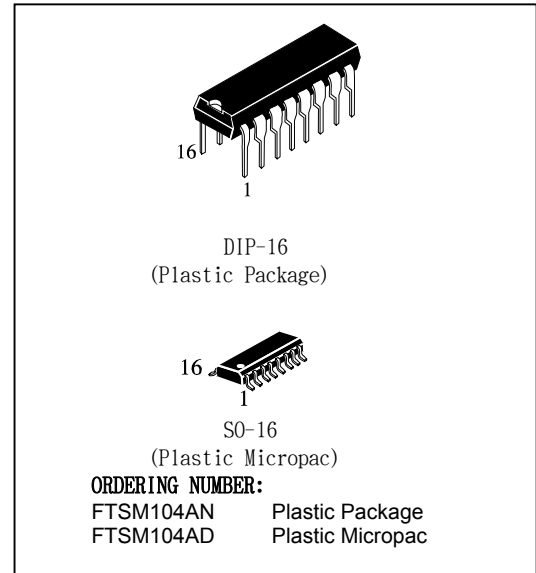
- LOW SUPPLY CURRENT : 375 μ A/op. (@ $V_{CC} = 5V$)
- LOW INPUT BIAS CURRENT : 20nA
- MEDIUM SPEED : 0.9MHz
- LOW INPUT OFFSET VOLTAGE : 0.5mV typ
- WIDE POWER SUPPLY RANGE : $\pm 1.5V$ to $\pm 15V$

VOLTAGE REFERENCE

- ADJUSTABLE OUTPUT VOLTAGE : V_{ref} to 36V
- 0.4% AND 1% VOLTAGE PRECISION
- SINK CURRENT CAPABILITY : 1 to 100mA
- TYPICAL OUTPUT IMPEDANCE : 0.2 Ω

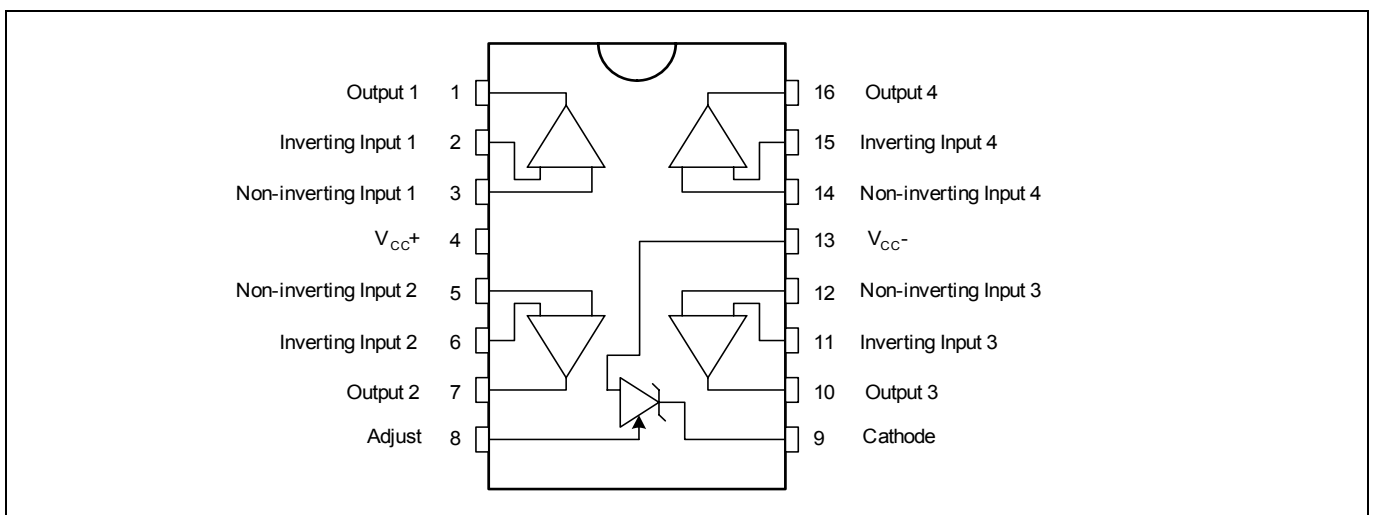
DESCRIPTION

The FTSM104A is a monolithic IC that includes four op-amps and an adjustable shunt voltage reference. This device is offering space and cost saving in many applications like power supply management or data acquisition systems.



Part number	Temperature Range		
		N	D
FTSM104A	-40 °C, +105°C	•	•

PIN CONNECTIONS





Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _{cc}	Supply Voltage	36	V
V _{id}	Differential Input Voltage	36	V
V _i	Input Voltage	-0.3 to +36	V
T _j	Maximum Junction Temperature	150	°C

Electrical Characteristics

V_{cc}⁺ = 5V, V_{cc}⁻ = 0V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
I _{cc}	Total Supply Current, excluding Current in the Voltage Reference V _{cc} ⁺ = 5 V, no load T _{min} < T _{amb} < T _{max} V _{cc} ⁺ = 30 V, no load T _{min} < T _{amb} < T _{max}		1.4	2.4 4	mA



Quad Operational Amplifier and Programmable Voltage Reference

OPERATIONAL AMPLIFIERS

$V_{cc}^+ = 5\text{ V}$, $V_{cc}^- = \text{Ground}$, $V_o = 1.4\text{ V}$, $T_{amb} = 25\text{ }^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
V_{io}	Input Offset Voltage $T_{amb} = 25\text{ }^\circ\text{C}$ $T_{min} \leq T_{amb} \leq T_{max}$		0.5	3 4	mV
DV_{io}	Input Offset Voltage Drift			7	$\mu\text{V}/^\circ\text{C}$
I_{io}	Input Offset Current $T_{min} \leq T_{amb} \leq T_{max}$		2	30 50	nA
I_{ib}	Input Bias Current $T_{min} \leq T_{amb} \leq T_{max}$		20	150 200	nA
A_{vd}	Large Signal Voltage Gain $V_{cc} = 15\text{V}$, $R_L = 2\text{k}$, $V_o = 1.4\text{V}$ to 11.4V $T_{min} \leq T_{amb} \leq T_{max}$	50 25	100		V/mV
SVR	Supply Voltage Rejection Ratio $V_{cc} = 5\text{V}$ to 30V	65	100		dB
V_{icm}	Input Common Mode Voltage Range $V_{cc} = +30\text{V}$ – see note ¹⁾ $T_{min} \leq T_{amb} \leq T_{max}$	0 0		$(V_{cc}^+) - 1.5$ $(V_{cc}^+) - 2$	V
CMR	Common Mode Rejection Ratio $T_{min} \leq T_{amb} \leq T_{max}$	70 60	85		dB
I_{source}	Output Current Source $V_{cc} = +15\text{V}$, $V_o = 2\text{V}$, $V_{id} = +1\text{V}$	20	40		mA
I_o	Short Circuit to Ground $V_{cc} = +15\text{V}$		40	60	mA
I_{sink}	Output Current Sink $V_{id} = -1\text{V}$, $V_{cc} = +15\text{V}$, $V_o = +2\text{V}$	10	20		mA
V_{OH}	High Level Output Voltage $V_{cc}^+ = 30\text{V}$, $R_L = 10\text{k}$ $T_{amb} = 25^\circ\text{C}$, $T_{min} \leq T_{amb} \leq T_{max}$	27 27	28		V
V_{OL}	Low Level Output Voltage $R_L = 10\text{k}$ $T_{min} \leq T_{amb} \leq T_{max}$		5	20 20	mV
SR	Slew Rate at Unity Gain $V_i = 0.5$ to 3V , $V_{cc} = 15\text{V}$ $R_L = 2\text{k}$, $C_L = 100\text{pF}$, unity gain	0.1	0.3		$\text{V}/\mu\text{s}$
GBP	Gain Bandwidth Product $V_{cc} = 30\text{V}$, $R_L = 2\text{k}$, $C_L = 100\text{pF}$ $f = 100\text{kHz}$, $V_{in} = 10\text{mV}$	0.5	0.9		MHz
THD	Total Harmonic Distortion $f = 1\text{kHz}$ $A_v = 20\text{dB}$, $R_L = 2\text{k}$, $V_{cc} = 30\text{V}$ $C_L = 100\text{pF}$, $V_o = 2V_{pp}$		0.02		%
e_n	Equivalent Input Noise Voltage $f = 1\text{kHz}$, $V_{cc} = 30\text{V}$, $R_s = 100\Omega$		50		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
cs	Channel Separation $1\text{kHz} < f < 20\text{kHz}$		120		dB

Note1: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V_{cc}^+ - 1.5\text{V}$. But either of both inputs can go to $+36\text{V}$ without damage.



VOLTAGE REFERENCE

Symbol	Parameter	Value	Unit
I_k	Cathode Current	1 to 100	mA

Symbol	Parameter	Min	Typ	Max	Unit
V_{ref}	Reference Input Voltage $T_{amb} = 25\text{ }^{\circ}\text{C}$ $T_{min} \leq T_{amb} \leq T_{max}$	2.49 2.48	2.5	2.51 2.52	V
ΔV_{ref}	Reference Input Voltage Deviation Over Temperature Range $V_{KA} = V_{ref}, I_k = 10\text{mA}$ $T_{min} \leq T_{amb} \leq T_{max}$		7	30	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage $I_k = 10\text{mA}, \Delta V_{KA} = 36\text{V to } 3\text{V}$	-2	-1.1		mV/V
I_{ref}	Reference Input Current $I_k = 10\text{mA}$ $T_{min} \leq T_{amb} \leq T_{max}$		1.5	2.5 3	μA
ΔI_{ref}	Reference Input Current Deviation over T° Range		0.8	1.2	μA
I_{min}	Minimum Cathode Current for Regulation $V_{KA} = V_{ref}$		0.5	1	mA
I_{off}	Off-State Cathode Current		180	500	nA
$ Z_{KA} $	Dynamic Impedance – (note 1) $V_{KA} = V_{ref}, \Delta I_k = 1\text{ to } 100\text{mA}, f < 1\text{kHz}$		0.2	0.5	Ω

Note 1: The Dynamic impedance is defined as $|Z_{KA}| = \Delta V_{KA} / \Delta I_k$



Typical Performance Characteristics

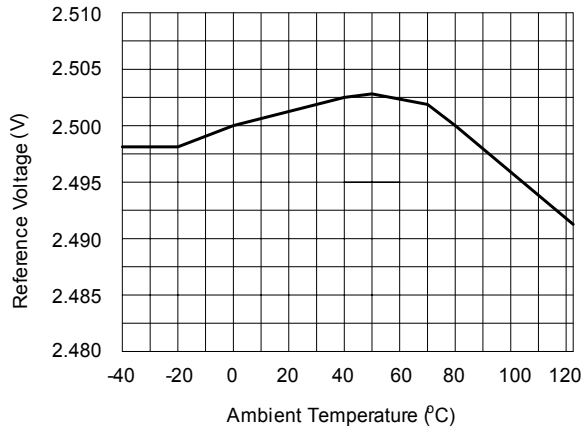


Figure 1. Reference Voltage vs. Ambient Temperature

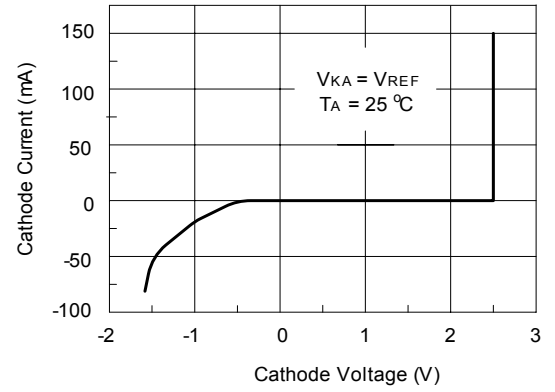


Figure 2. Cathode Current vs. Cathode Voltage

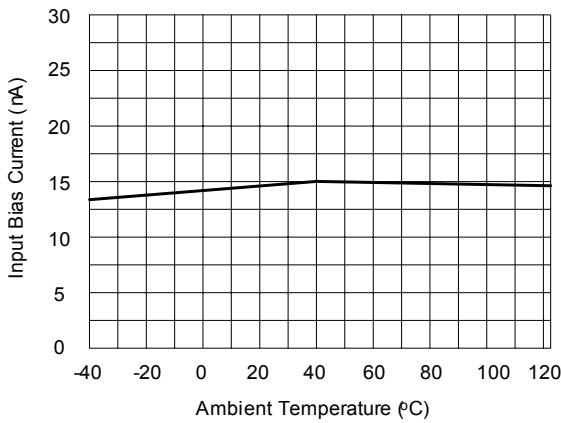


Figure 3. Input Bias Current vs. Ambient Temperature

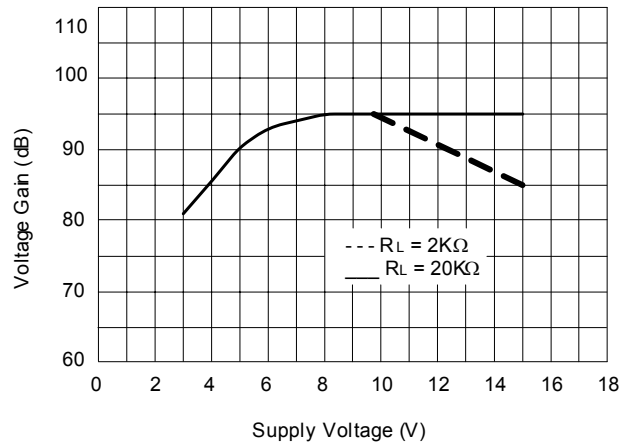
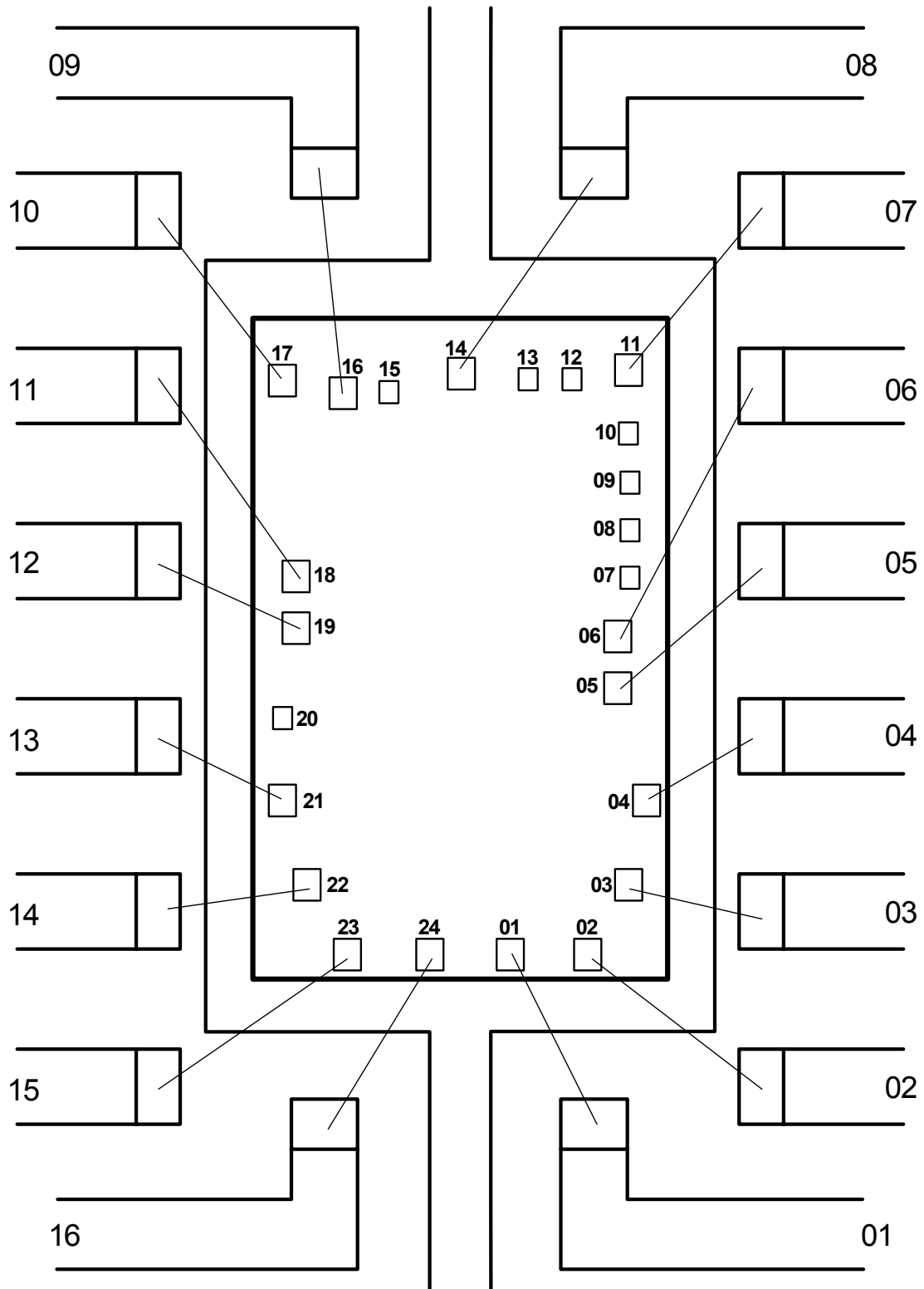
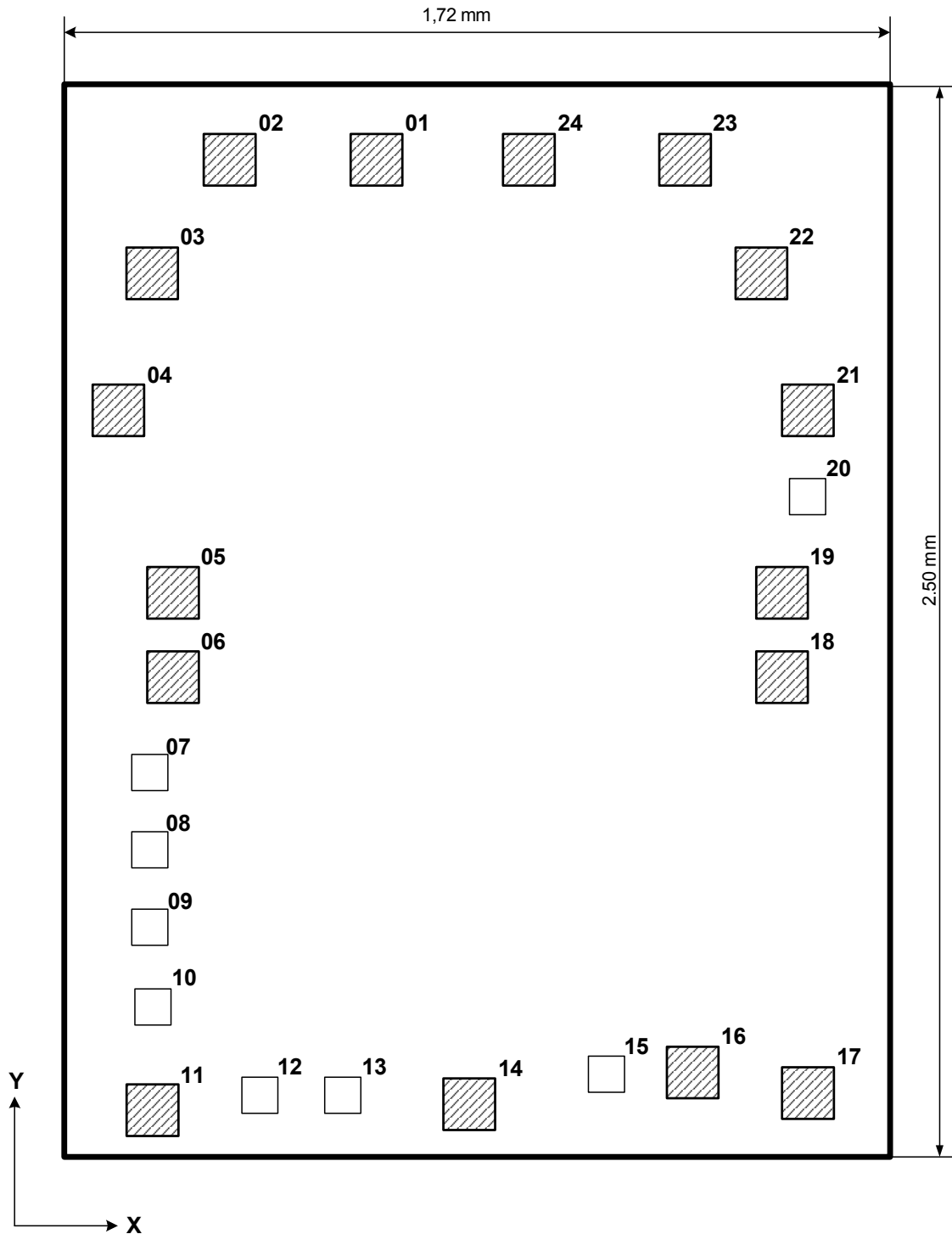


Figure 4. Operational Amplifier Voltage Gain



Bonding diagram of FTSM104A



Pad size 01 - 06, 11, 14, 16 - 19, 21 - 24 - have been bounded
Pad size 07 - 10, 12, 13, 15, 20 - have not been bounded

Pads location of FTSM104A



Quad Operational Amplifier and Programmable Voltage Reference

Die size $X_r=1.72\text{mm}$, $Y_r=2.50\text{mm}$ (pad size measured by layer "passivation")

Coordinates of pads

No of pad (by layer "passivation")	Coordinates left bottom, mkm		pad size, mkm
	X	Y	
01	691	2307	100×100
02	353	2307	100×100
03	139	2137	100×100
04	93	1664	100×100
05	139	1200	100×100
06	139	1040	100×100
07	121	855	70×70
08	121	667	70×70
09	121	479	70×70
10	121	291	70×70
11	99	131	100×100
12	256	145	70×70
13	378	145	70×70
14	732	132	100×100
15	1189	183	70×70
16	1305	172	100×100
17	1525	143	100×100
18	1377	1040	100×100
19	1377	1200	100×100
20	1550	1453	70×70
21	1520	1664	100×100
22	1479	2137	100×100
23	1265	2307	100×100
24	927	2307	100×100



No of pad	Pin	Function
01	01	Output 1
02	02	Inverting input 1
03	03	Non-inverting input 1
04	04	Vcc ⁺
05	05	Non-inverting input 2
06	06	Inverting input 2
11	07	Output 2
14	08	Adjust
16	09	Cathode
17	10	Output 3
18	11	Inverting input 3
19	12	Non-inverting input 3
21	13	Vcc ⁻
22	14	Non-inverting input 4
23	15	Inverting input 4
24	16	Output 4