

VOLTAGE RANGE: 20 - 40V
CURRENT: 1.0 A
Features

- Metal-Semiconductor junction with guard ring
- Epitaxial construction
- Low forward voltage drop, low switching losses
- High surge capability
- For use in low voltage, high frequency inverters free
- Wheeling, and polarity protection applications
- The plastic material carries U/L recognition 94V-0

Mechanical Data

- Case: JEDEC R-1 molded plastic
- Terminals: Axial lead, solderable per
- MIL-STD-202 Method 208
- Polarity: Color band denotes cathode
- Weight: 0.007 ounces, 0.20 grams


Maximum Ratings and Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise specified

Single phase, half wave, 60Hz, resistive or inductive load. For capacitive load, derate current by 20%.

Characteristic	Symbol	1N17	1N18	1N19	Unit
Maximum recurrent peak reverse voltage	V_{RRM}	20	30	40	V
Maximum RMS voltage	V_{RMS}	14	21	28	V
Maximum DC blocking voltage	V_{DC}	20	30	40	V
Maximum average forward rectified current 9.5mm lead length, $@T_A=75^\circ\text{C}$	$I_{F(AV)}$	1.0			A
Peak forward surge current 8.3ms single half-sine-wave superimposed on rated load $@T_J=70^\circ\text{C}$	I_{FSM}	25.0			A
Maximum instantaneous forward voltage @ 1.0A (Note 1) $@ 3.0A$	V_F	0.45 0.75	0.55 0.875	0.60 0.90	V
Maximum reverse current $@T_A=25^\circ\text{C}$ at rated DC blocking voltage $@T_A=100^\circ\text{C}$	I_R	1.0 10.0			mA
Typical junction capacitance (Note 2)	C_J	110			pF
Typical thermal resistance (Note 3)	$R_{\theta JA}$	50			$^\circ\text{C}/\text{W}$
Operating junction temperature range	T_J	-55 ---- +125			$^\circ\text{C}$
Storage temperature range	T_{STG}	-55 ---- +150			$^\circ\text{C}$

NOTE: 1. Pulse test : 300 μs pulse width, 1% duty cycle.

2. Measured at 1.0MHz and applied reverse voltage of 4.0V DC.

3. Thermal resistance junction to ambient

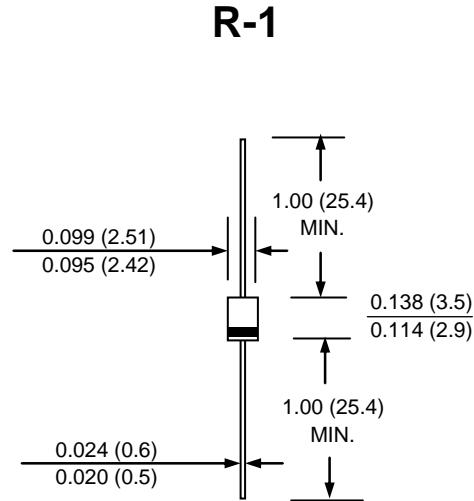
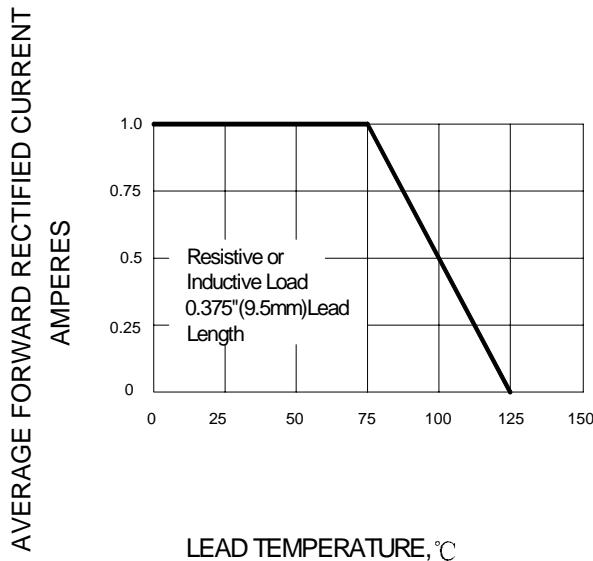
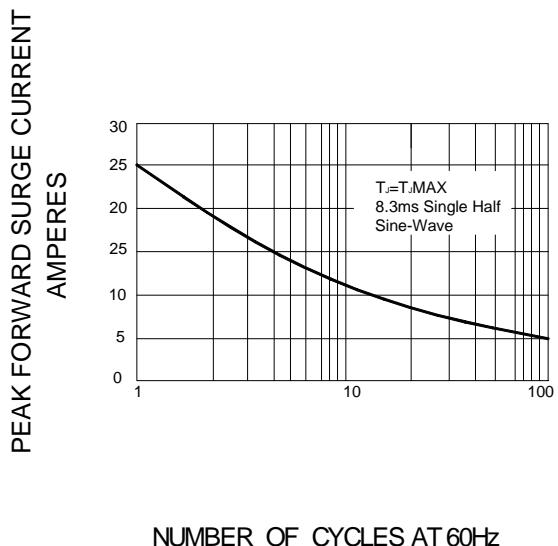
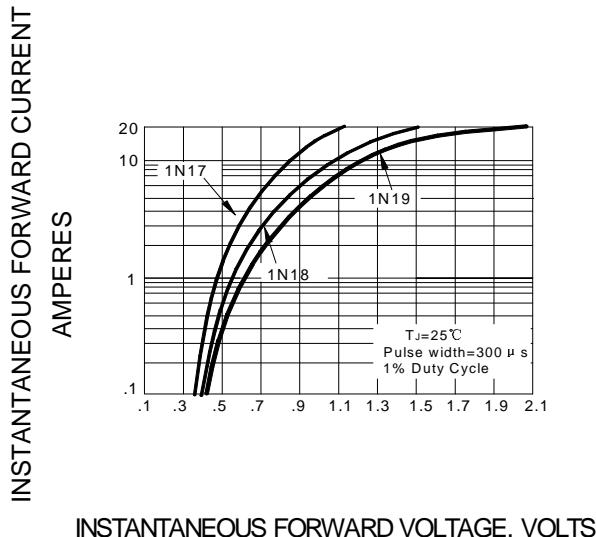

Dimensions in inches and (millimeters)

FIG.1 – FORWARD DERATING CURVE

FIG.2 – PEAK FORWARD SURGE CURRENT

FIG.3 – TYPICAL INSTANTANEOUS FORWARD CHARACTERISTICS

FIG.4 – TYPICAL JUNCTION CAPACITANCE
