

# TVS8501V12

## Product Preview Transient Voltage Suppressors

### Features

- Protection for the following IEC Standards:
  - IEC61000–4–2 Level 4:  $\pm 30$  kV Contact Discharge
  - IEC61000–4–5 (Lightning) 40 A (8/20  $\mu$ s)
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS

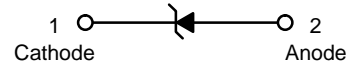
Rating	Symbol	Value	Unit
IEC 61000–4–2 (ESD) Contact Air		$\pm 30$ $\pm 30$	kV
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	–65 to +150	$^{\circ}$ C
Maximum Peak Pulse Current 8/20 $\mu$ s @ $T_A = 25^{\circ}$ C	$I_{PP}$	40	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



**ON Semiconductor**<sup>®</sup>

<http://onsemi.com>



**UDFN2  
CASE 517CZ**

### MARKING DIAGRAM



XX = Specific Device Code  
M = Date Code

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
TVS8501V12MUT5G	UDFN2 (Pb-Free)	8000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.



# TVS8501V12

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

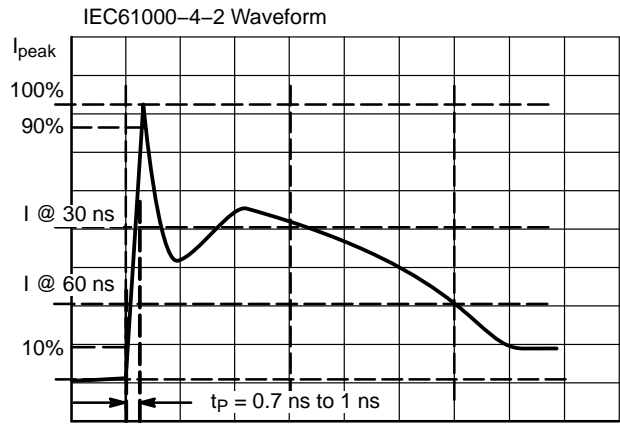


Figure 2. IEC61000-4-2 Spec

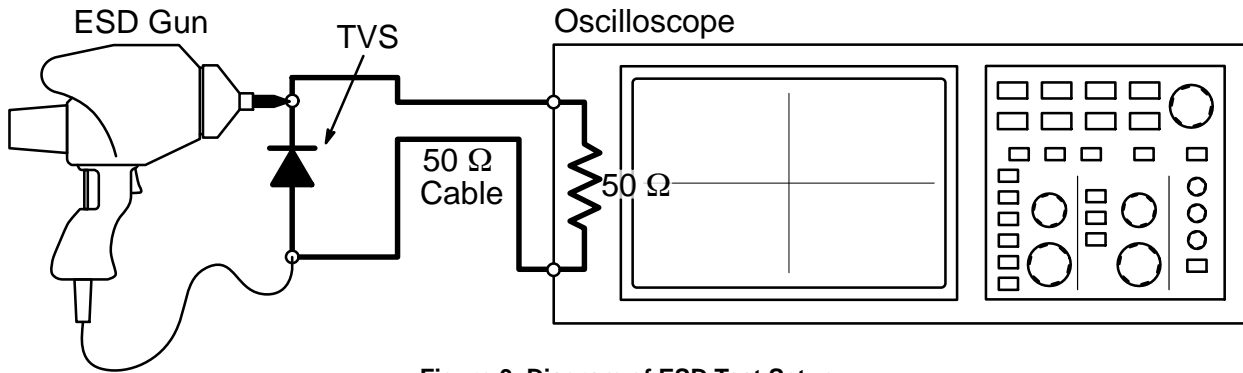


Figure 3. Diagram of ESD Test Setup

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage

at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

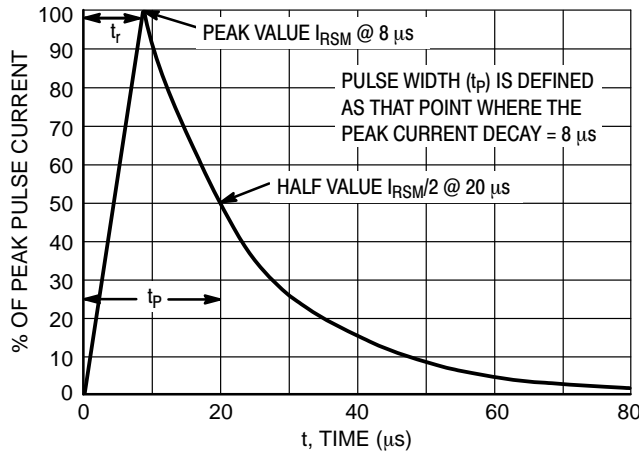
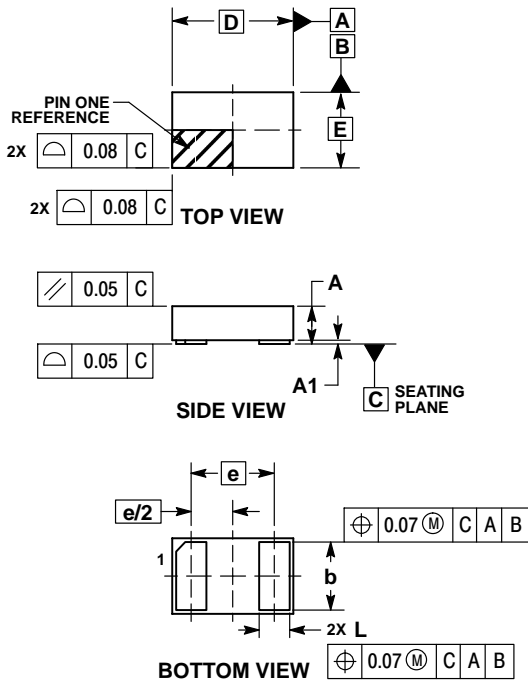


Figure 4. 8 X 20 μs Pulse Waveform

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## PACKAGE DIMENSIONS

UDFN2 1.6x1.0, 1.1P  
CASE 517CZ  
ISSUE A

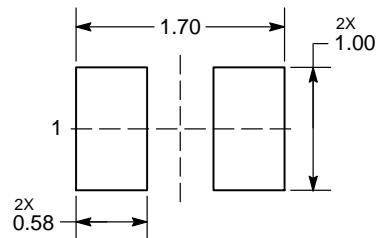


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

MILLIMETERS		
DIM	MIN	MAX
A	0.45	0.55
A1	—	0.05
b	0.85	0.95
D	1.60	BSC
E	1.00	BSC
e	1.10	BSC
L	0.35	0.45

**RECOMMENDED SOLDERING FOOTPRINT\***



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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