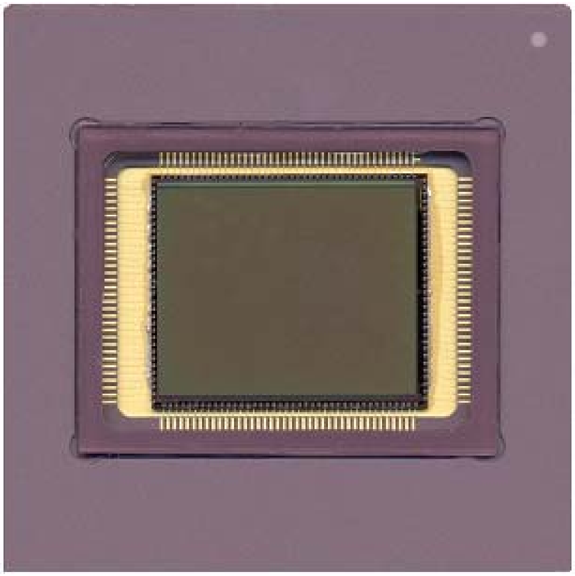
LUPA-1300

1.3 M Pixel
High Speed CMOS Image Sensor



Datasheet

Document history record

Issue	Date	Description of changes
2.1	April, 2003	First draft.
3.0	March, 2004	Updated timing diagrams Updated layout Updated package drawings Disclaimer Soldering and handling conditions Updated specifications
3.1	December, 2004	Added equivalent Cypress part numbers, ordering information. Added Cypress Document # 38-05711 Rev ** in the document footer.

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1 Preamble

1.1 Overview

This document describes the interfacing and the driving of the image sensor LUPA1300, which is a 1280 by 1024 CMOS pixel array working at 450 frames/sec. The sensor is an active pixel sensor with synchronous shutter. The pixel size is 14 * 14 µm and the sensor is designed to achieve a fame rate of 450 frames/sec at full resolution. This high frame rate can be achieved by 16 parallel output amplifiers each working at 40MHz pixel rate.

The readout speed can be boosted by means of windowed Region Of Interest (ROI) readout. High dynamic range scenes can be captured using the double slope functionality.

The sensor uses a 3-wire Serial-Parallel (SPI) interface. It is housed in a 145-pin ceramic PGA package.

In the following sections the different modules of the image sensor are discussed more into detail. This datasheet allows the user to develop a camera-system based on the described timing and interfacing.

1.2 Main features

The main features of the image sensor are identified as:

- SXGA resolution: 1280 x 1024 active pixels.
- 14 μm^2 square pixels (based on the high-fill factor active pixel sensor technology of FillFactory (US patent No. 6,225,670 and others)).
- Pixel rate of 40 MHz using 16 parallel outputs.
- Random programmable windowing.
- Dual slope integration possible
- 145-pin PGA package
- Peak QE x FF of 15%.
- Optical format: 1,43” (17.9 mm x 14.3 mm)
- Optical dynamic range: 62 dB (1330:1) in single slope operation and 80…100 dB in double slope operation.
- 16 parallel analog output amplifiers.
- Synchronous pipelined shutter.
- Processing is done in a CMOS 0.50 µm triple metal process.

1.3 Part Number

Name	Package	Monochrome / color
LUPA-1300-M CYIL1SM1300AA-GBC (preliminary)	145-pins PGA package.	Monochrome.
LUPA-1300-C CYIL1SC1300AA-GAC (preliminary)	145-pins PGA package.	RGB Bayer pattern.

2 Specifications

2.1 General specifications

Parameter	Specification	Remarks
Pixel architecture	*6T-pixel*	*Based on the high-fill factor active pixel sensor technology of FillFactory*
Pixel size	*14 µm x 14 µm*	*The resolution and pixel size results in a 17.9 mm x 14.3 mm optical active area.*
Resolution	*1280 x1024*	
Pixel rate	*640 MHz*	*Using a 20 MHz system clock and 16 parallel outputs.*
Shutter type	*Pipelined snapshot shutter*	*Full snapshot shutter with variable integration time*
Full frame rate	*450 frames/second*	*Frame rate increase possible with ROI read out and/or sub sampling.*
Package	*Pin grid array 145 pins*	

Table 1: general specifications of the LUPA sensor

2.2 Electro-optical characteristics

2.2.1 Overview

Parameter	Specification	Remarks
FPN	*<2 % RMS*	<10 % p/p.
PRNU	*20 % RMS*	Half saturation.
Conversion gain	*16 uV/electron*	
Output signal amplitude	*1V*	Unity gain.
Saturation charge	*62.500 e-*	Is more then 60.000 (=1V/16uV/e-) due to non-linearity in saturated region.
Sensitivity	*1500 V.m2/W.s*	Average white light.
	8.33 V/lux.s	Visible band only (180 lx = 1 W/m2).
	21.43 V/lux.s	Visible + NIR (70 lx = 1 W/m2).
Fill Factor	*50%*	100%-metal and polycide coverage.
Peak QE * FF **Peak SR * FF**	*15%* *0.08 A/W*	See spectral response curve.
MTF	*X: 67 %* *Y: 66%*	@ Nyquist
Temporal Noise	*45e-*	Dark environment, measured at T=21°C.

S/N ratio	*1330*	1330 = 60000:45 = 62 dB.
Spectral sensitivity range	*400 – 1000 nm*	
Parasitic light sensitivity	*< 0.5 %*	I.e. sensitivity of the storage node compared to the sensitivity of photodiode
Power dissipation	*900 mWatt*	Typical.
Output impedance	*200-300 Ohms*	Typical

Table 2: electrical-optical specifications of the LUPA-1300 sensor

2.2.2 Features and general specifications

Feature	**Specification/Description**
Electronic shutter type	Synchronous pipelined shutter with variable integration time.
Windowing (ROI)	Programmable via SPI.
Read out sequence	Progressive scan.
Extended dynamic range	Double slope extended dynamic range.
X clock	20 MHz (pixel rate of 40 MHz)
Number of outputs	16.
Supply voltage VDD	Image core supply: Range from 3V to 6 V. Analog supply: Nominal 5 V. Digital: Nominal 5 V.
Logic levels	5V (digital supply)
Operational temperature range	0°C to 60°C, with degradation of dark current.
Package	145-pins Pin Grid Array (PGA).

Table 3: Features and general specifications

2.2.3 Spectral response curve

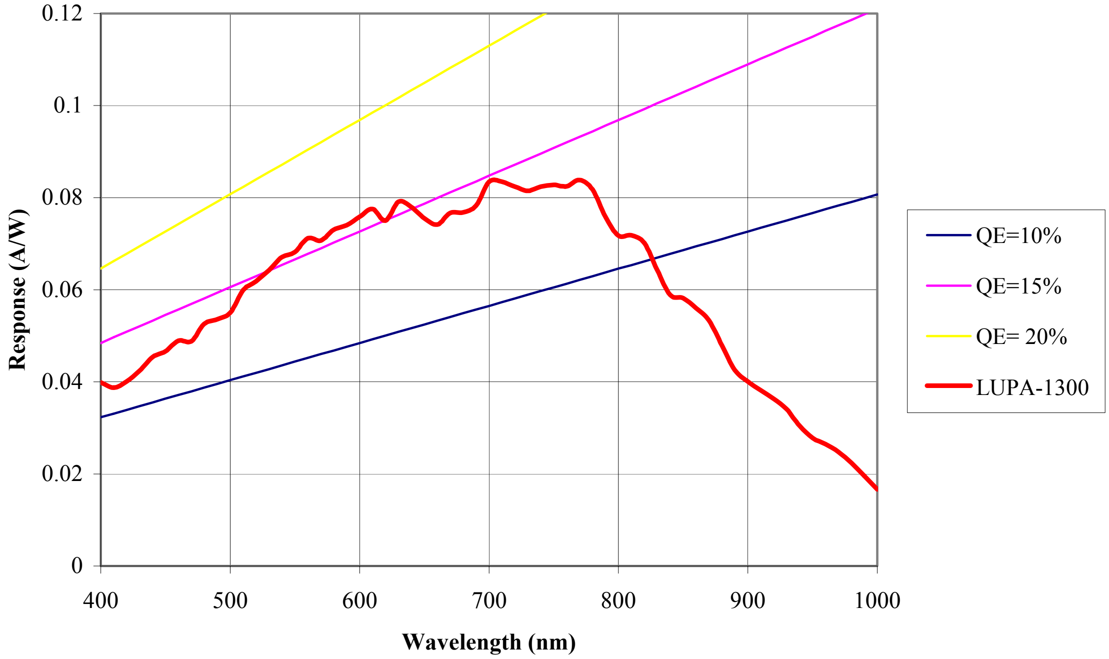

Figure 1: Spectral response curve

Figure 1 shows the spectral response characteristic. The curve is measured directly on the pixels. It includes effects of non-sensitive areas in the pixel, e.g. interconnection lines. The sensor is light sensitive between 400 and 1000 nm. The peak QE * FF is 15% approximately between 500 and 700 nm.

2.2.4 Photo-voltaic response curve

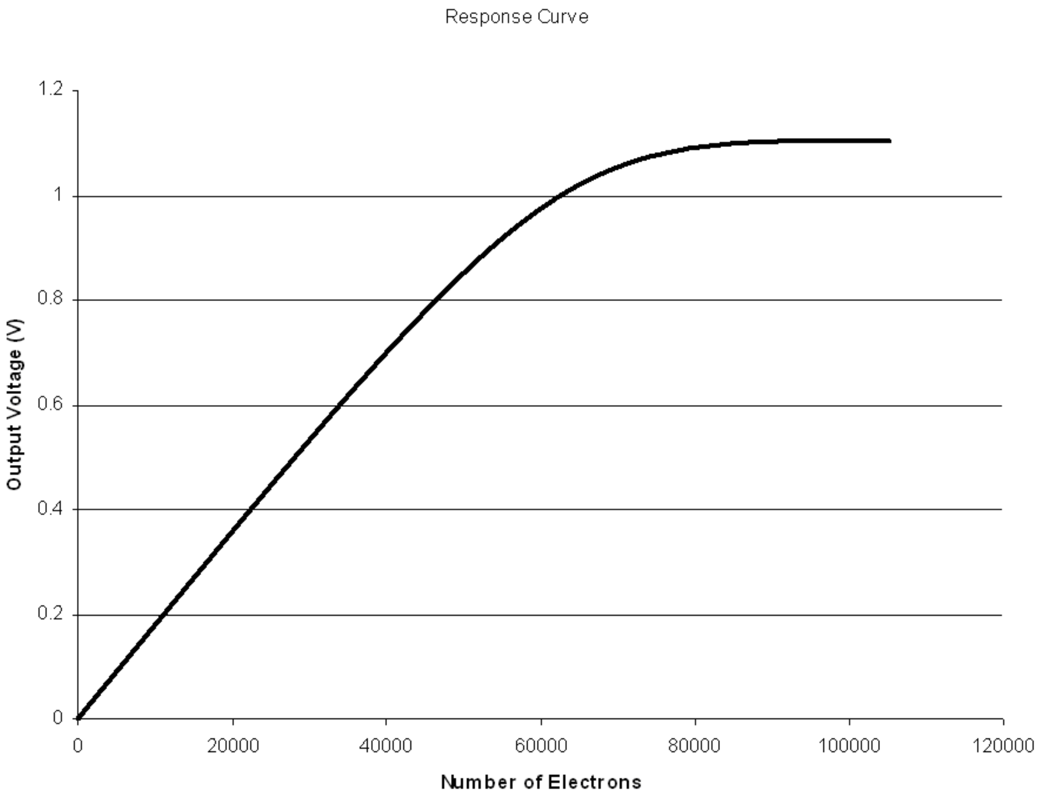

*Figure 2: Output voltage as a function of the number of electrons***.**

As one can see from Figure 2, the output signal ranges between 1.1 V (dark) to 0 V (saturation) and is linear until around 800mV. Note that the upper part of the curve (near saturation) is actually a logarithmic response.

2.3 Electrical specifications

2.3.1 Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DC}	DC supply voltage	-0.5 to +7	V
V_{IN}	DC input voltage	0.5 to V_{DC} + 0.5	V
V_{OUT}	DC output voltage	-0.5 to V_{DC} + 0.5	V
I	DC current per pin; any single input or output. (see table 7 for more exceptions)	± 50	mA
T_{STG}	Storage temperature range.	-40 to 100	°C
T_L	Lead temperature (10 seconds soldering).	300	°C

Table 4: Absolute maximum ratings

Note: Absolute Ratings are those values beyond which damage to the device may occur.

2.3.2 Recommended operating conditions

Symbol	Parameter	Typ	Unit
Vdda	*Power supply column read out module.*	*5*	*V*
Vdd	*Power supply digital modules*	*5*	*V*
Vddr	*Power supply logic for drivers*	*5*	*V*
Voo	*Power supply output stages*	*5*	*V*
Vres	*Power supply reset drivers*	*6*	*V*
Vres_ds	*Power supply multiple slope reset driver*	*4.5*	*V*
Vmem_h	*Power supply memory element (high level)*	*6*	*V*
Vmem_l	*Power supply memory element (low level)*	*4.5*	*V*
Vpix	*Power supply pixel array*	*4.5*	*V*
Vstable	*Power supply output stages. Decouples noise on the Voo supply from the output signal.*	*5.5*	*V*

Table 5: Recommended operation conditions

Note:

1. All parameters are characterized for DC conditions after thermal equilibrium has been established.
2. Unused inputs must always be tied to an appropriate logic level, e.g. either VDD or GND.
3. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.

3 Sensor architecture

The image sensor consists of the pixel array, the column readout electronics, X-and Y addressing, on chip drivers, the output amplifiers and some logic.

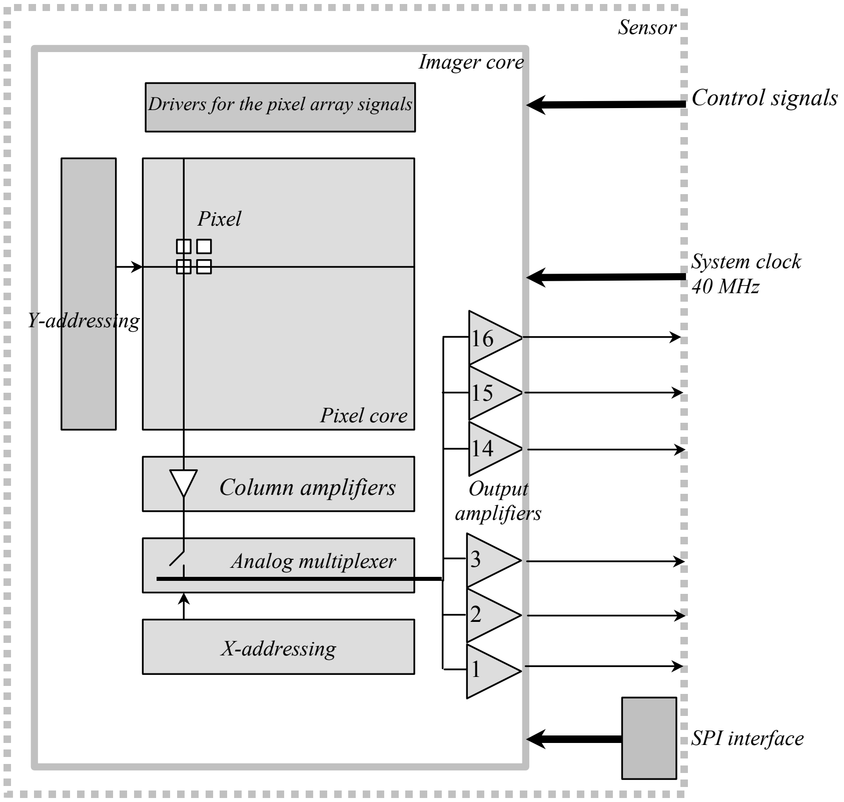

Figure 3: architecture of the LUPA sensor

Figure 3 shows a schematic representation of the image sensor on which the different modules are displayed.

The image core is a pixel array of 1280 * 1024 pixels each of 14 *14 µm2 in size. The readout is from bottom left to top right. To obtain a frame rate of 450 frames/sec for this resolution, 16 output amplifiers each capable of driving an output capacitance of 10 pF at 40MHz are placed on the image sensor.

The column readout amplifiers bring the pixel data to the output amplifiers. The logic and the x- and y addressing controls the image sensor so that progressive scan and windowing is possible. Extra pixel array drivers are foreseen at the top of the image sensor to control the global pixel array signals.

3.1 Pixel architecture

The active pixels allow synchronous shutter “i.e. all pixels are illuminated during the same integration time, starting from the same moment in time. After a certain integration time, the pixels are readout sequentially. Readout and integration are in parallel, which means that when the image sensor is readout, the integration time for the next frame is ongoing. This feature requires a memory element inside the pixel, which affects the maximum fill factor. A schematic representation of the pixel is given in figure 4.

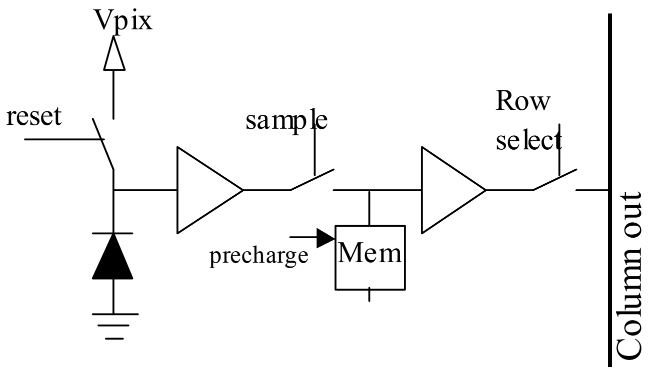

Figure 4: schematic representation of the synchronous pixel as used in the LUPA design
The signals mentioned in figure 4 are the internal signals, generated by the internal drivers, required to have the synchronous shutter feature.

The photodiode is designed to obtain sensitivity as high as possible for a dynamic range of at least 60dB. Consequently the photodiode capacitance is 10fF @ the output, resulting in a S/N of more than 60dB as the rms noise level is within the expectation of 45 noise electrons. The pixel was specially designed to have a very low parasitic light sensitivity (<0.5%). The pixels are based on the high-fill factor active pixel sensor technology of FillFactory (US patent No. 6,225,670 and others)).

3.2 Column readout amplifiers

The column readout amplifiers are the interface between the pixels and the output amplifiers. The pixels in the array are selected line by line and the pixels of the selected line are connected to the column readout amplifiers, which bring the pixel data in the correct format to the output amplifiers.

To obtain a high frame rate, the complexity and the number of stages in the column readout amplifiers must be minimized, so that the power dissipation remains as low as possible, but also to minimize the row blanking time. Figure 5 is a schematic representation of the column readout structure. It consists of 2 parts. The first part is a module that reduces the row blanking time. The second part shifts the signal to the correct level for the output amplifiers and allows multiplexing in the x-direction.

From the moment that a new row is selected, the pixel data of that row is placed onto the columns of the pixel array. These columns are long lines and have a large parasitic capacitance. As the pixel is small, it is not possible to match the transistor inside the pixel, which drives this column. Consequently, the first module in the column readout amplifiers must solve the mismatch between the pixel driver and the large column capacitance.

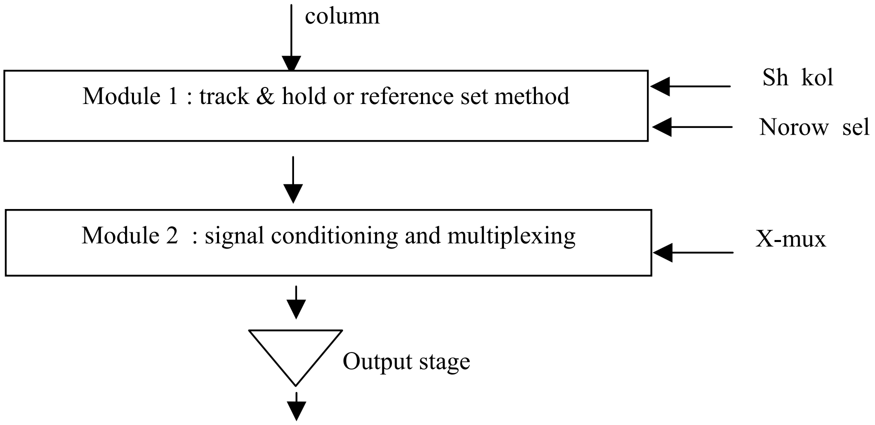

Figure 5: Schematic representation of the column readout structure.

3.3 Output amplifiers

16 output amplifiers each capable of working at 40MHz pixel rate are placed equidistant on the bottom of the image sensor. These output amplifiers are required to obtain a frame rate of 450 frames/sec. A single output stage, not only to reduce power, but also to achieve the required pixel rate is designed. Figure 6 is a schematic representation of this module.

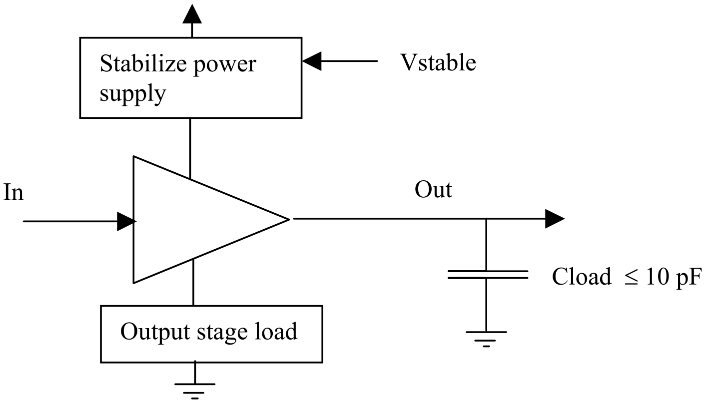

Figure 6: schematic representation of a single output stage.

Each output stage is designed to drive a load of 10pF at a pixel rate of 40MHz. The load in the output stage determines this pixel rate. In case the load capacitance is less than 10pF, the load in the output stage can increase, resulting in less power dissipation of the output stages and consequently of the whole sensor. Additionally, decreasing the load of the output stage allows having more current available for the output stage to charge or discharge the load capacitance to obtain a higher pixel rate.
To avoid variations on the supply voltage to be seen on the output signal, a special module to stabilize the power supply is required. This module that requires an additional supply voltage (Vstable) allows variation on the supply voltage Voo without being seen on the output signal.
One can also choose to have a passive load of chip instead of the active output stage load. This deteriorates the linearity of the output stages, but decreases the power dissipation, as the dissipation in the load is external.

Note: The LUPA-1300 is designed to drive a capacitive load, not a resistive. When one wants to transport the output signals over long distances (more than 1 inch), make sure to place buffers on the outputs with high input impedances (preferably >1Mohms). This is necessary because the output impedance of the LUPA-1300 is between 200-300 ohms typically.

3.4 Frame rate and windowing

3.4.1 Frame rate calculation

The frame period of the LUPA-1300 sensor can be calculated as follows:

Frame period = FOT + (Nr.Lns* (RBT + pixel period * Nr. Pxs / 16)

with: FOT: Frame Overhead Time = 1 us.
Nr. Lns : Number of Lines read out each frame (Y).
Nr. Pxs: Number of pixels read out each line (X).
RBT: Row blanking time = 200 ns (nominal; can be further reduced).
Pixel period: clock_x period/2 (both rising and falling edge are active edges).

- Example 1 read out of the full resolution at nominal speed (40 MHz pixel rate):

Frame period = 5 us + (1024 * (200 ns + 25 ns * 1280 / 16) = 2.25 ms => 444 fps.

- Example 2 read out of 800x600 at nominal speed (40 MHz pixel rate):

Frame period = 5 us + (600 * (200 ns + 25 ns * 800 / 16) = 871 us => 1148 fps.

- Example 3 read out of 640x480 at nominal speed (40 MHz pixel rate):

Frame period = 5 us + (480 * (200 ns + 25 ns * 640 / 16) = 577 us => 1733 fps.

- Example 4 read out of the full resolution at nominal speed (40 MHz pixel rate) with reduced overhead time:

Frame period = 5 us + (1024 * (100 ns + 25 ns * 1280 / 16) = 2.15 ms => 465 fps.

3.4.2 X-Y addressing and windowing

The pixel array is readout by means of programmable X and Y shift registers. The pixel array is scanned line-by-line and column-by-column. The starting point in X and Y is defined individually for each register and is determined by the address downloaded by the Serial – Parallel Interface (SPI). Both registers work in the same way. A sync pulse that sets the address pointer to the starting address of each register, initializes them. A clock pulse for the x- and y-shift register shifts the pointer individually and makes sure that the sequential selection of the lines and columns is correct.

3.5 Temperature reference circuits

3.5.1 Temperature diode

The most commonly used temperature measurement is monitoring of the junction voltage of a diode, therefore we also added a temperature diode to measure the temperature of the silicon die. This diode junction voltage is generated by a "small", forward biased, constant current flow (in between 10 and 100 µA).

This junction voltage has a nearly linear relationship with the temperature of the die with a typical sensitivity of about 430°C per volt (2.3 mV per °C) for silicon junctions.

3.5.2 Temperature module

On the same image sensor we have foreseen a module to verify the temperature on chip and the variation of the output voltage (dark level of the pixel array) due to a temperature variation. This module contains a copy of the complete signal path, including a blind pixel, the column amplifiers and an output stage. It DC response may serve a temperature calibration for the real signal. The temperature functionality is given in figure 7. Between room temperature and 60 °C we see a voltage variation of about 0.5 mV.

Due to different applied supply voltages, as there are: Vreset, Vmem, Vpix… an offset between the output voltage of the temperature sensor and the output of a black signal of the pixel array can occur. Depending on the working conditions of the image sensor one can fine-tune the temperature module with its voltage supply. In case one has a 6V signal for reset and a 4-6V signal for Vmem, a supply voltage of 5.5V for the temperature sensor will result in a closer match between this temperature sensor and the black level of the image sensor. Changing the supply voltage of the temperature sensor results only in a shift of the output voltage therefore the supply voltage of the temperature module can be tuned to make the output of the module equal to the dark signal of the pixel array at a certain working temperature.

Vsupply (V)	5	5.5	6	6.1	6.2	6.3	6.4	6.5
Vout @ 21°C	0.58	0.8	1.03	1.07	1.12	1.17	1.22	1.27

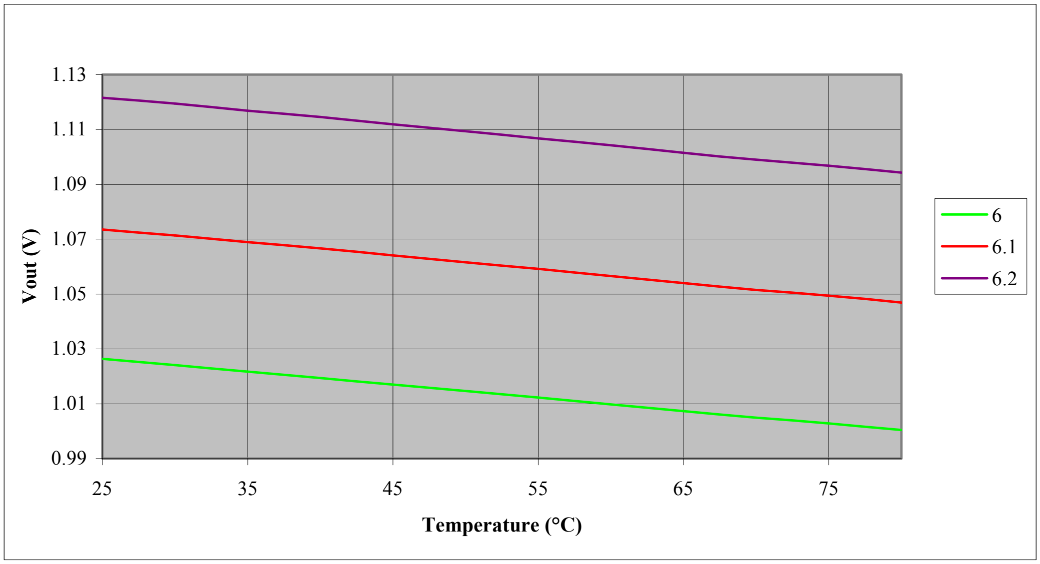

Figure 7: Output voltage of the temperature module versus temperature

3.6 Synchronous shutter

In a synchronous (snapshot) shutter light integration takes place on all pixels in parallel, although subsequent readout is sequential.

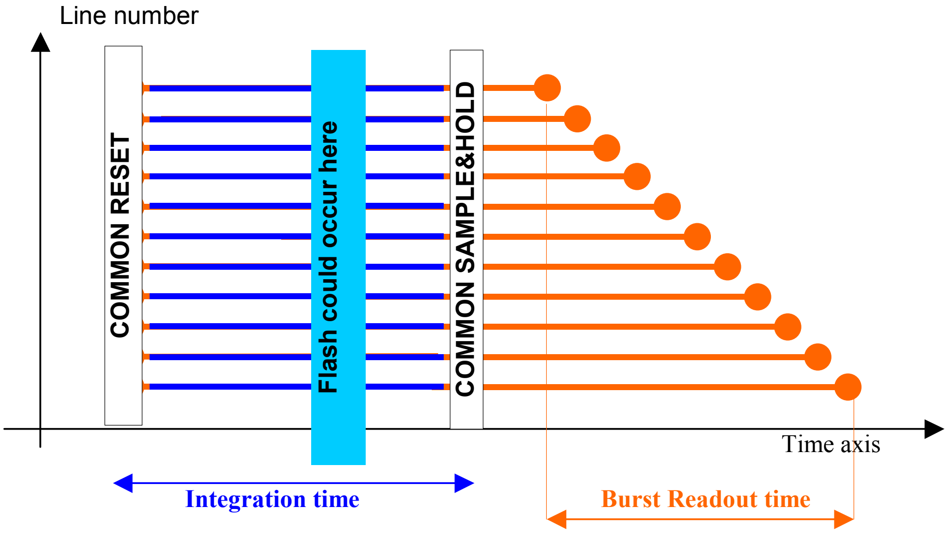

Figure 8: Synchronous shutter operation

Figure 8 shows the integration and read out sequence for the synchronous shutter. All pixels are light sensitive at the same period of time. The whole pixel core is reset simultaneously and after the integration time all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration.

Note that the integration and read out cycle can occur in parallel.

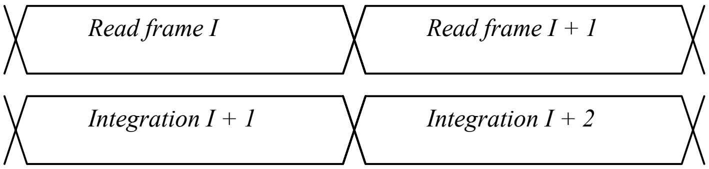

Figure 9:Integration and read out in parallel

The control of the readout of the frame and of the integration time are independent of each other with the only exception that the end of the integration time from frame I+1 is the beginning of the readout of frame I+1.

3.7 Non-destructive readout (NDR)

The sensor can also be read out in a non-destructive way. After a pixel is initially reset, it can be read multiple times, without resetting. The initial reset level and all intermediate signals can be recorded. High light levels will saturate the pixels quickly, but a useful signal is obtained from the early samples. For low light levels, one has to use the later or latest samples.

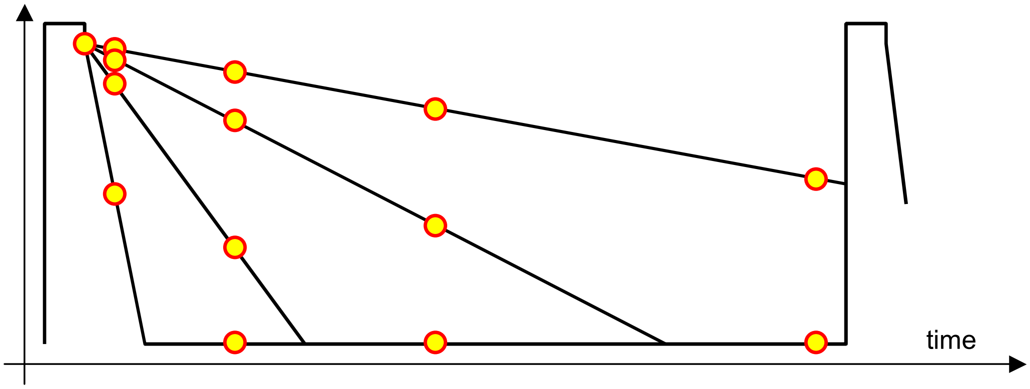

Figure 10. Principle of non-destructive readout.

Essentially an active pixel array is read multiple times, and reset only once. The external system intelligence takes care of the interpretation of the data. Table 6 summarizes the advantages and disadvantages of non-destructive readout.

Table 6: Advantages and disadvantages of non-destructive readout.

Advantages	Disadvantages
Low noise – as it is true CDS.	System memory required to record the reset level and the intermediate samples.
High sensitivity – as the conversion capacitance is kept rather low.	Requires multiples readings of each pixel, thus higher data throughput.
High dynamic range – as the results includes signal for short and long integrations times.	Requires system level digital calculations.

3.8 Operation and signaling

One can distinguish the different signals into different groups:

- Power supplies and grounds
- Biasing and analog signals
- Pixel array signals
- Digital signals
- Test signals

3.8.1 Power supplies and grounds

Every module on chip, as there are: column readout, output stages, digital modules, drivers, … has its own power supply and ground. Off chip the grounds can be combined, but not all power supplies may be combined. This results in several power supplies, but is required to reduce electrical crosstalk and to improve shielding. On chip we have the ground lines also separately for every module to improve shielding and electrical crosstalk between them. The only special ground is "Gnd_res", which can be used to remove the blooming if any and which can improve optical crosstalk.
An overview of the supplies is given in table 7. The power supplies related to the pixel array signals are described in the paragraph concerning the pixel array signals.

Note: Normal application doesn't require this Gnd_res and it can be connected to ground.

Name	Max current	Typ.	Max	Description
Vdda	*50mA*	*5V*		*Power supply column readout module*
Vdd	*20mA*	*5V*		*Power supply digital modules*
Voo	*85mA*	*5V*		*Power supply output stages*
Vstable	*6mA*	*5.5V*	*6V*	*Power supply output stages. Decouples noise on the Voo supply from the output signal.*
Vpix	*200mA*	*5V*	*6V*	*Power supply pixel array.*
Vddr	*20mA*	*5V*		*Power supply logic for drivers*
Vres	*50mA*	*6V*		*Power supply to reset the pixels*
VmemH	*50mA*	*6V*		*Power supply for high DC level Vmem*
VmemL	*50mA*	*4.5V*		*Power supply for low DC level Vmem*

Table 7: power supplies used in the LUPA design

The maximum currents mentioned in table 7 are peak currents. The power supplies need to be able to deliver these currents especially the maximum supply current for Vpix.
It is important to notice that we don't do any power supply filtering on chip and that noise on these power supplies can contribute immediately to the noise on the signal. Especially the voltage supplies Vpix and Vdda are important to be well noise free. With respect to the power supply Voo, a special decoupling is used, for which an additional power supply Vstable is required.

Important notes:

1.At start up the Vpix supply draws a very high current (> 300 mA) which has to be limited (max. 200 mA) otherwise the bond wires of the particular supply will be destroyed. One should make sure that the Vpix power supply limits the current draw to the Vpix sensor supply pins to max. 200mA. When the bond wires of Vpix are destroyed the sensor isn't operating normally and will not meet the described specifications.

2. VmemL must sink a current, not source it. All power supplies should be decoupled very close to the sensor pin (typical 100nF to filter high frequency dips and 10 microF to filter slow dips). A typical decoupling circuit is shown in the figure below. Vres_ds must be able to sink and source current.

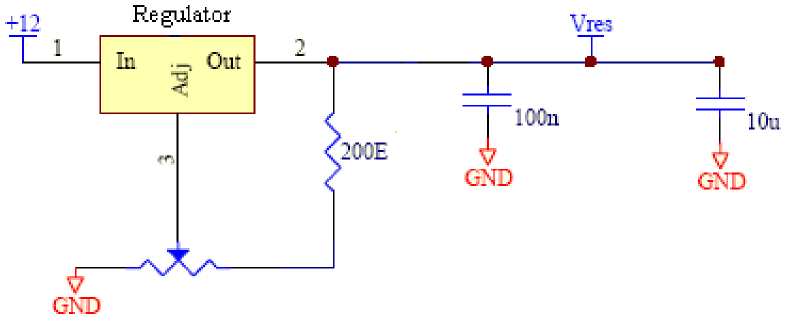

Figure 11a: Schematic of typical decoupling of power supply (source current)

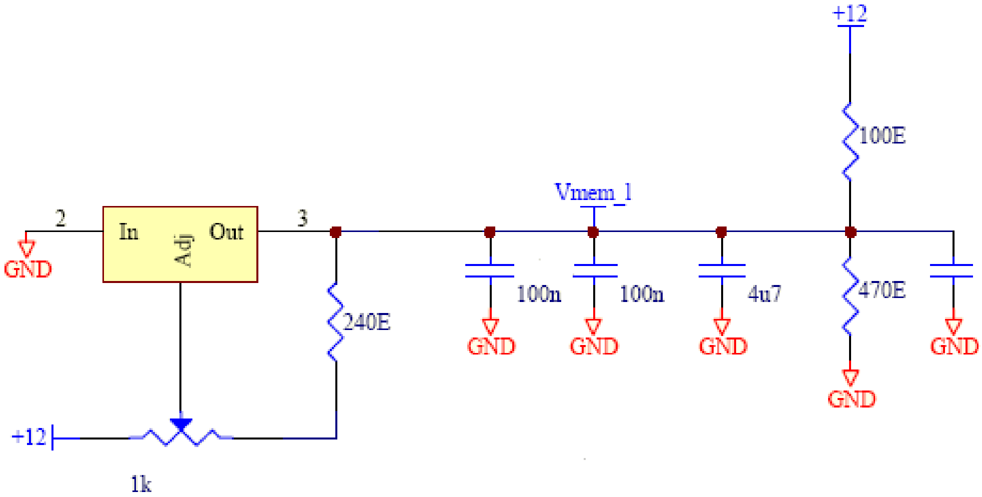

Figure 11b: Schematic of typical decoupling of power supply (sink current)

3.8.2 Biasing and analog signals

Besides the biasing signals, the only analog signals are the output signals Out1 – Out16. Each output signal is analog with respect to the voltage level, but is discrete in time. This means that on the speed of Clock_x, the outputs change to a different level, depending on the illumination of the corresponding pixels.

The biasing signals determine the speed and power dissipation of the different modules on chip. These biasing signals have to be connected trough a resistor to ground or power supply and should be decoupled with a capacitor. If the sensor is working properly, each of the biasing signals will have a dc-voltage depending on the resistor value and on the internal circuitry. These dc-voltages can be used to check the operation of the image sensor. Table 8 gives the different biasing signals, the way they should be connected, and the expected dc-voltage. Due to small process variations, these dc-voltages change from chip to chip and 10% variation is possible.

Signal	Comment	Expected dc-level
Pre_load	*Connect with 10KΩ to Vdda and capacitor of 100nF to Gnd*	*2.0V*
Col_load	*Connect with 2MΩ to Vdda and capacitor of 100nF to Gnd*	*0.9V*
Psf_load	*Connect with 240KΩ to Gnd and capacitor of 100nF to Vdda*	*3.7V*
Nsf_load	*Connect with 100KΩ to Vdda and capacitor of 100nF to Gnd*	*1.3V*
Load_out	*Connect with 27KΩ to Voo and capacitor of 100nF to Gnd*	*1.6V*
Decx_load	*Connect with 27KΩ to Gnd and capacitor of 100nF to Vdd*	*2.8V*
Decy_load	*Connect with 27KΩ to Gnd and capacitor of 100nF to Vdd*	*2.8V*

Table 8 : overview of biasing signals

Each resistor controls the speed and power dissipation of the corresponding module, as this resistor determines the current required to charge and/or discharge internal nodes inside the module.

A decoupling with a small capacitor is advisable to reduce the HF noise onto the analog signals. Only the capacitor on the Pre_load signal can be omitted.

3.8.3 Pixel array signals

Figure 4 in paragraph 2.2 is a schematic representation of the pixel as used in the LUPA design. The applied signals to this pixel are: reset, sample, Precharge, Vmemory, row select and Vpix. These are internal generated signals derived by on chip drivers from external applied signals. Consequently it is important to understand the relation between both internal and external signals and to understand the operation of the pixel.

The timing of the pixel is given in figure 12 in which only the internal signals are given.

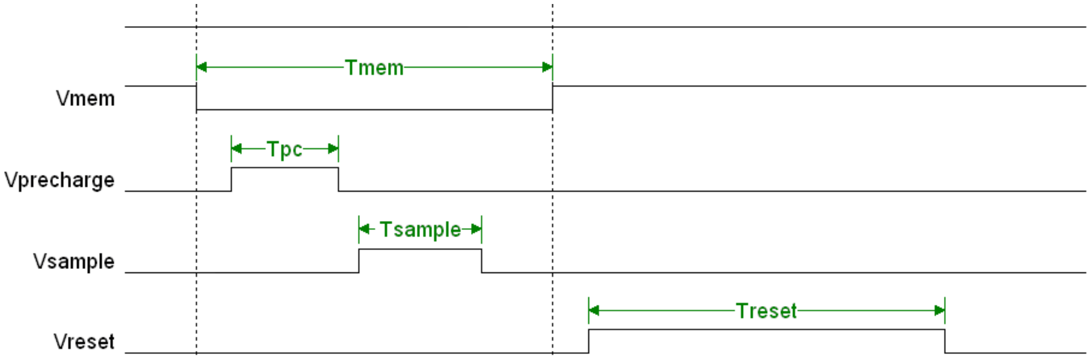

Figure 12: Internal timing of the pixel.

At the end of the integration time, the information on the photodiode node needs to be sampled and stored onto the pixel memory, required to allow synchronous shutter. To do this, we need the signals “Precharge” and “Sample”. “Precharge” resets the pixel memory and “Sample” places the pixel information onto the pixel memory. Once this information stored, the readout of the pixel memories can start in parallel with a new integration time. An additional signal “Vmem” is needed to obtain a larger output swing.

Except from Vpix power supply, drivers generate the other pixel signals on chip. The external signals to obtain the required pulses consist of 2 groups. One is the group of digital signals to indicate when the pulse must occur and the other group is dc-supply lines indicating the levels of the pulses. Table 9 summarizes the relation between the internal and external pixel array signals

Internal signal	Vlow	Vhigh	External control signal	Low dc level	High dc level
Precharge	*0*	*5V*	*Precharge*	*Gnd*	*Vddr*
Sample	*0*	*5V*	*Sample*	*Gnd*	*Vddr*
Reset	*0V*	*4 – 6V*	*Reset & Reset_ds*	*Gnd_res*	*Vres & Vres_ds*
Vmemory	*4.5V*	*6V*	*Mem_hl*	*Vmem_l*	*Vmem_h*

Table 9: overview of the internal and external pixel array signals.

The Precharge and Sample signals are the most straightforward signals. The internal

signal Vmemory is a signal that switches between a low voltage (3.5 – 5.5V) and a high voltage (5-6V). The signal Mem_hl controls the applied level and the power supply lines Vmem_l and Vmem_h determine the low and high dc-levels.
The Reset signal is due to the dual slope technique a little more complex. In case the dual slope is not used, the reset signal is straightforward generated from the external reset pulse. In this case the supply voltage Vres determines the level to which the pixel is resetted.
In case the dual slope operation is desired, one needs to give a second pulse to a lower reset level during integration. This can be done by the control signal Reset_ds and by the power supply Vres_ds that defines the level to which the pixel has to be resetted.
If a pulse is given on the Reset_ds signal, a second pulse on the internal reset line is generated to a lower level, determined by the supply Vres_ds. If no Reset_ds pulse is given, the dual slope technique is not implemented.
Note that Reset is dominant over Reset_ds, which means that the high voltage level will be applied for reset, if both pulses occur at the same time.

The external control signals should be capable of driving input capacitance of about 20pF.

3.8.4 Digital signals

The digital signals control the readout of the image sensor. These signals are:
- Sync_y: Starts the readout of the frame or window at the address defined by the y-address register. This pulse synchronizes the y-address register: active high. This signal is at the same time the end of the frame or window and determines the window width.
- Clock_y: Clock of the y-register. On the rising edge of this clock, the next line is selected.
- Sync_x: Starts the readout of the selected line at the address defined by the x-address register. This pulse synchronizes the x-address register: active high. This signal is at the same time the end of the line and determines the window length.
- Address: the x- and y-address is downloaded serial through this signal.
- Clock_spi: clock of the serial parallel interface. This clock downloads the address into the SPI register.
- Load_addr: when the SPI register is downloaded with the desired address, the signal Load_addr signal loads the x-and y-address into their address register as starting point of the window of interest.
- Sh_col: control signal of the column readout. Is only used in sample & hold mode (See timing)
- Norow_sel: Control signal of the column readout. Is only used in Norow_sel mode (See timing)
- Pre_col: Control signal of the column readout to reduce row blanking time
- Sel_active: activates the active load on chip for the output amplifiers. If not used, a passive load can be used or one can use this signal to put the output

stages in standby mode.

- Eos_x: end of scan signal: is an output signal, indicating when the end of the line is reached. Is not generated when doing windowing
- Eos_y: end of scan signal: is an output signal, indicating when the end of the frame is reached. Is not generated when doing windowing.

All digital signals are buffered and filtered on chip to remove spikes and to achieve the required on chip driving speed. The applied digital signals should be capable of driving 20pF input capacitance.

3.8.5 Test signals

Some test signals are required to evaluate the optical performance of the image sensor. Other test signals allow us to test internal modules in the image sensor and some test signals will give us information concerning temperature and influence of the temperature on the black level.

Evaluation on the optical performance (Spectral response, fill factor)

- Array_diode
- Full_diode

Evaluation of the output stages:

- Black
- Dc_black

Evaluation of the x and y –shift registers:

- Eos_x
- Eos_y

Indication of the temperature and influence on the black level:

- Temp_diode_n
- Temp_diode_p

4 Timing

4.1 Timing of the pixel array

The timing of the image sensor can be divided in two major parts. The first part of the timing is related with the timing of the pixel array. This implies the control of the integration time, the synchronous shutter operation, and the sampling of the pixel information onto the memory element inside each pixel. The signals needed for this control are described in previous paragraph 3.7.3 and figure 12 shows the timing of the internal signals. Figure 13 should make the timing of the external signals clear.

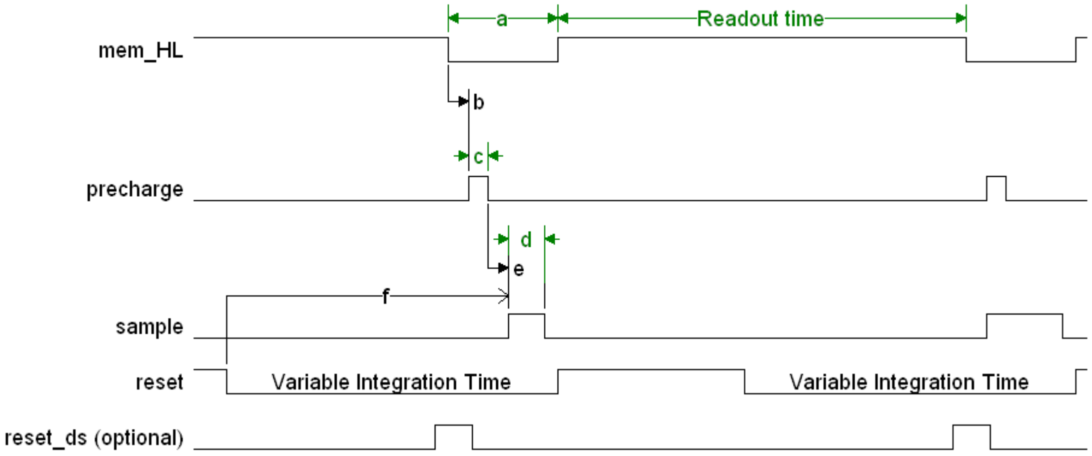

Figure 13: timing of the pixel array. All external signals are digital signals between 0 and 5V. The Reset_ds is only required in case dual slope is desired.

Symbol	Name	Value
a	Mem_HL	> 5 µsec
b	MEM_HL –Precharge	> 200 nsec
c	Precharge	> 500 nsec
d	Sample	> 3.9 µsec
e	Precharge-Sample	> 400 nsec
f	Integration time	> 2 µsec

Table 10: Typical timings of the pixel array

The timing of the pixel array is straightforward. Before the frame is read, the information on the photodiode needs to be stored onto the memory element inside the pixels. This is done by means of the signals Vmemory, Precharge and Sample. Precharge sets the memory element to a reference level and Sample stores the photodiode information onto the memory element. Vmemory pumps up this value to reduce the loss of signal in the pixel and this signal must be the envelop of Precharge and Sample. After Vmemory is high again, the readout of the pixel array can start. The frame blanking time or frame overhead time is thus the time that Vmemory is low, which is about 5µsec. Once the readout starts, the photodiodes can all be initialised by reset for the next integration time. The duration of the reset pulse indicates the integration time for the next frame. The longer this duration, the shorter the integration time becomes. Maximum integration time is thus the time it takes to readout the frame, minus the minimum pulse for reset, which is preferred not to be less than 10µsec. The minimal integration time is the minimal time between the falling edge of reset and the rising edge of sample. Keeping the slow fall times of the corresponding internal generated signals, a minimal integration time is about 2µsec. An additional reset pulse can be given during integration by Reset_ds to implement the double slope integration mode. (See paragraph 6.1)

4.2 Readout of the pixel array

Once the photodiode information is stored into the memory element in each pixel, the total pixel array of 1280 * 1024 needs to be readout in less than 2 msec (2msec – frame overhead time = 1995µsec). Additionally, it is possible that only a part of the whole frame is read out. This is controlled by the starting address that has to be downloaded and from the end address, which is controlled by the synchronisation pulses in x- and y direction. The readout itself is straightforward. Line by line is selected by means of a sync-pulse and by means of a Clock_y signal. Once a new line selected, it takes a while (row blanking time) before the information of that line is stable. After this row blanking time the data is multiplexed in blocks of 16 to the output amplifiers. A sync-pulse and a clock pulse in the x-direction do this multiplexing.

Figure 14 shows the y-address timing. The top curves are the selection signals of the pixels, which are sequentially active, starting by the sync pulse. The next line is selected on the rising edge of Clock_y. It is important that the Sync_y pulse covers 1 rising edge of the Clock_y signal. Otherwise the synchronization will not work properly.

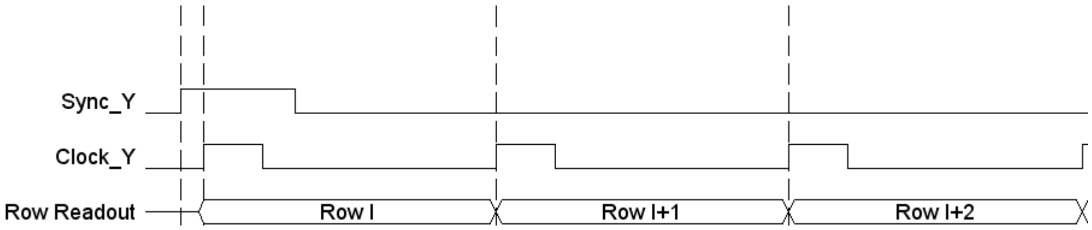

Figure 14 : timing of the y shift register.

The first selected line after a Sync_y pulse is the line defined by the y-address in the y-address register. Every select line is in principle 1 clock period long, except for the first select line. The first select line goes high as soon as a Sync_y pulse occurs together with a rising edge of Clock_y. On the next rising edge of Clock_y, the next row is selected, unless Sync_y is still active. In figure 15, a short Sync_y pulse makes sure that the first row is selected during 1 period of Clock_y.

Once a line is selected, it needs to stabilize first of all, which is called the row blanking time, and secondly the pixels need to be read out. Figure 15 shows the principle.

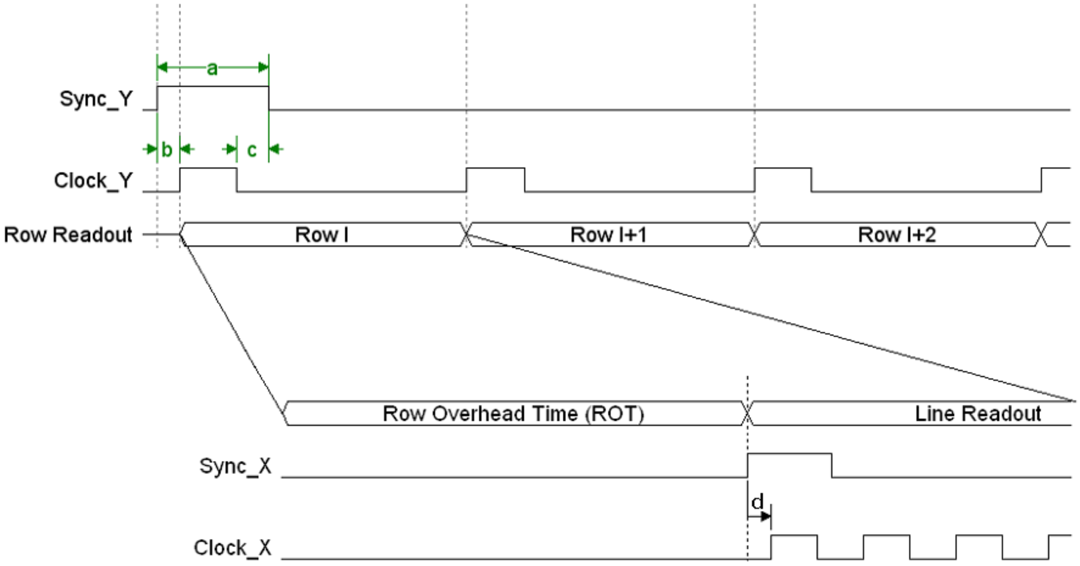

Figure 15: Readout time of a line is the sum of the row blanking time and on the line readout time.

Symbol	Name	Value
a	Sync_Y	> 100 nsec
b	Sync_Y-Clock_Y	> 50 nsec
c	Clock_Y-Sync_Y	> 50 nsec
d	Sync_X –Clock_X	> 50ns

Once the information of the selected line is stable the addressing of the pixels can start. This is done by means of a Sync_x and a Clock_x pulse in the same way as the Y-addressing. The Sync_x pulse downloads the address in the address register into the shift register and connects the first block of 16 columns to the 16 outputs.
In fact on chip is a 32-output bus instead of 16, but on the rising edge of Clock_x the first 16 columns of the bus are connected to the output stages. On the falling edge of Clock_x, the last 16 columns of the selected bus are connected to the output stages.

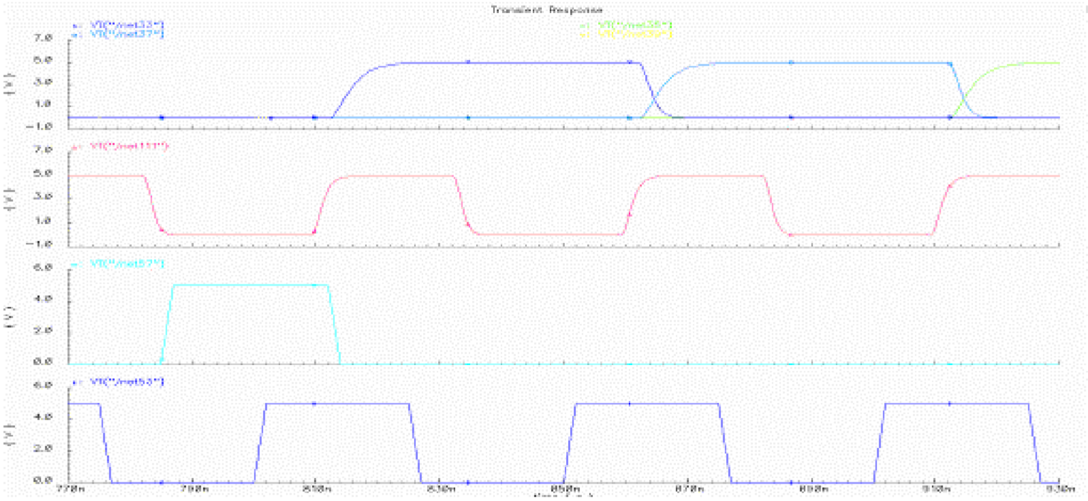

Figure 16: Timing of the x-shift register. The curves from bottom to top : Clock_x, Sync_x, Internal generated Clock, Sel_block1, sel_block2,…

The timing in figure 16 is comparable with the timing of the y-shift register, only that the timing is much faster. Again the synchronization pulse must be high on the rising edge of Clock_x.

IMPORTANT note : The applied Clock_x, is filtered on chip to remove spikes. This is especially required at these high speeds. This filtering results in an on chip Clock_x that is delayed in time with about 10nsec. In other words, the data at the output has, with respect to the external Clock_x, a propagation delay of 20nsec. This 20nsec come from 10nsec of the generation of the internal Clock_x and 10nsec due to other on chip generated signals.

4.2.1 Reduced Row Overhead Time timing

The row overhead time is the time between the selection of lines that one has to wait to get the data stable at the column amplifiers.
This row overhead time is a loss in time, which should be reduced as much as possible.

4.2.1.1 Reduced timing

A straightforward way of reducing the R.O.T is by using a sample and hold function. By means of Sh_col the analog data is tracked during the first 200nsec during the selection of a new set of lines. After 200nsec, the analog data is stored. The ROT is in this case reduced to 200nsec, but as the internal data was not stable yet dynamic range is lost because not the complete analog levels are reached yet after 200ns. Figure 17 shows this principle. Sh_col is now a pulse of 100ns-200ns starting 25 ns after Norowsel. The duration of Sh_col is equal to the ROT. The shorter this time the shorter the ROT will be however this lowers also the dynamic range.

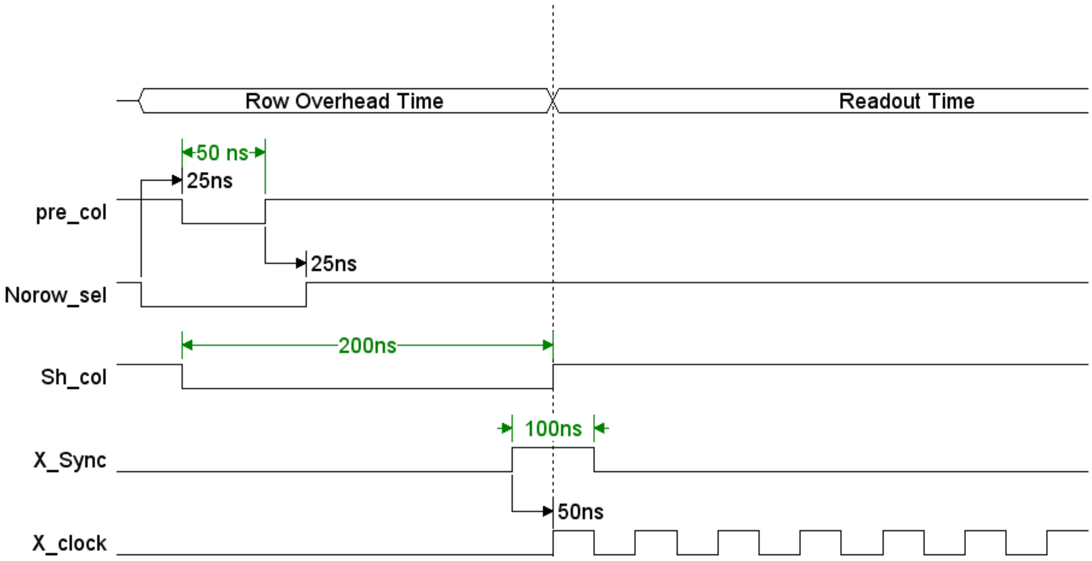

Figure 17: Reduced standard ROT by means of Sh_col signal. pre_col (short pulse) , Norowsel (short pulse) and Sh_col (large pulse).

4.2.1.2 Standard timing (ROT = 200 ns)

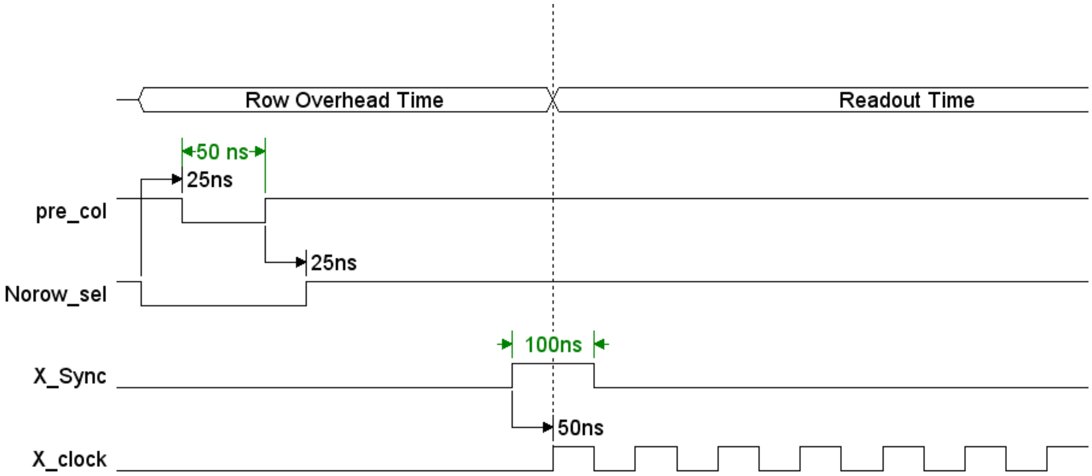

Figure 18: Only pre_col and Norowsel control signals are required. SH_col is made active low.

In this case the control signals Norowsel and pre_col are made active for about 50 nsec from the moment the next line is selected. The time these pulses have to be active is related with the biasing resistance Pre_load. The lower this resistance, the shorter the pulse duration of Norowsel and pre_col may be. After these pulses are given, one has to wait for 180nsec before the first pixels can be sampled. For this mode Sh_col must be made active low.

4.3 Timing of the Serial Parallel Interface (SPI)

The serial parallel interface is used to upload the x- and y-address into the x- and y-address registers. This address is the starting point of the window of interest and is uploaded in the shift register by means of the corresponding synchronization pulse.

The elementary unit cell of the serial to parallel interface is shown in Figure 19. 16 of these cells are connected in parallel, having a common Load_addr and Clock_spi form the entire uploadable address block. The uploaded addresses are applied to the sensor on the rising edge of signal Load_addr.

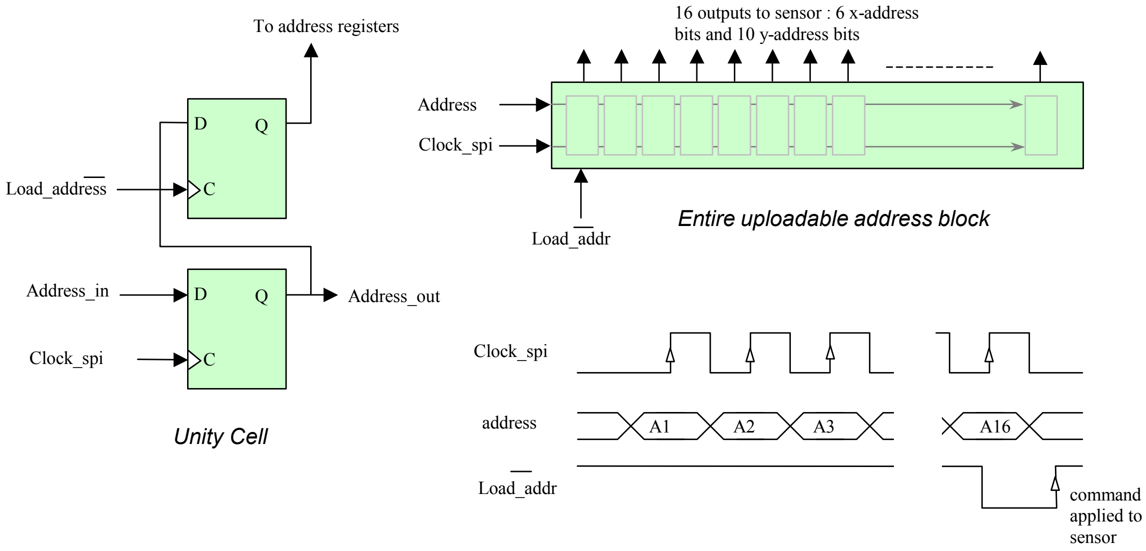

Figure 19: Schematic of the SPI interface

The Y-address has to be applied first and the X-address last. With respect to the timing in figure 19, A1 corresponds with the least significant bit of the Y-address (Y0) and A16 corresponds with the most significant bit of the X-address (X5). The Y-address is a 10 bit and the X-address is a 6-bit address register.

5 Pin configuration

The LUPA-1300 sensor will be packed in a PGA package with 145 pins. Each bond pad consists of 2 pad openings, one for wafer probing and one for bonding. Table 11 gives an overview of the pin names and their functionality.

Pin	fp	Name	Function	description
B3	1	n.c.		Not connected
C3	2	n.c.		
D3	3	Voo	Supply 5V	Supply voltage output stages : 5V
A2	4	Gnd	Ground	Ground of the sensor
B2	5	Out1	Analog out	Output 1
E3	6	Voo	Supply 5V	Supply voltage output stages : 5V
C2	7	Out2	Analog out	Output 2
D2	8	Gnd	Ground	Ground of the sensor
E2	9	Out3	Analog out	Output 3
A1	10	Voo	Supply 5V	Supply voltage output stages : 5V
F3	11	Out4	Analog out	Output 4
F2	12	Gnd	Ground	Ground of the sensor
B1	13	Out5	Analog out	Output 5
C1	14	Voo	Supply 5V	Supply voltage output stages : 5V
D1	15	Out6	Analog out	Output 6
G3	16	Gnd	Ground	Ground of the sensor
E1	17	Out7	Analog out	Output 7
G2	18	Voo	Supply 5V	Supply voltage output stages : 5V
F1	19	Out8	Analog out	Output 8
G1	20	Gnd	Ground	Ground of the sensor
H3	21	Out9	Analog out	Output 9
H2	22	Voo	Supply 5V	Supply voltage output stages : 5V
H1	23	Out10	Analog out	Output 10
J1	24	Gnd	Ground	Ground of the sensor
J2	25	Out11	Analog out	Output 11
J3	26	Voo	Supply 5V	Supply voltage output stages : 5V
K1	27	Out12	Analog out	Output 12
K2	28	Gnd	Ground	Ground of the sensor
L1	29	Out13	Analog out	Output 13
K3	30	Voo	Supply 5V	Supply voltage output stages : 5V
L2	31	Out14	Analog out	Output 14
M1	32	Gnd	Ground	Ground of the sensor
N1	33	Out15	Analog out	Output 15
L3	34	Voo	Supply 5V	Supply voltage output stages : 5V
M2	35	Out16	Analog out	Output 16

P1	36	Gnd	Ground	Ground of the sensor
N2	37	Voo	Supply 5V	Supply voltage output stages : 5V
M3	38	n.c.		
P2	39	n.c.		
N3	40	Gnd	Ground	Ground of the sensor
N4	41	Voo	Supply 5V	Supply voltage output stages : 5V
N5	42	Vstable	Supply 5V	Supply voltage to stabilize output stages : 5.5V
P3	43	Load_out	Biasing	Analog bias for output amplifiers 27KΩ to Voo and capacitor of 100nF to ground
P5	44	Dc_black	Testpin 6	dc-black signal required to characterise the output stages
P4	45	Vdd	Supply 5V	Supply voltage digital modules : 5V
Q1	46	Gnd	Ground	Ground of the sensor
N6	47	Vdda	Supply 5V	Supply voltage analog modules : 5V
P6	48	Gnd	Ground	Ground of the sensor
Q2	49	Vpix	Supply 5V	Supply voltage pixel array : 5V
Q3	50	Eos_x	Digital I/O	End of scan signal of the x-register : active high pulse indicates the end of the shift register is reached
Q4	51	Nsf_load	Biasing	Analog bias for column stages : 100KΩ to Vdda and capacitor of 100nF to ground
N7	52	Psf_load	Biasing	Analog bias for column stages : 240KΩ to gnd and capacitor of 100nF to Vdda
P7	53	Col_load	Biasing	Analog bias for column stages : 2MΩ to Vdda and capacitor of 100nF to ground
Q5	54	Pre_load	Biasing	Analog bias for column stages : 10KΩ to Vdda and capacitor of 100nF to ground
Q6	55	n.c.		
Q7	56	Array_diode	Testpin 3	Array of pixels as designed in pixel array
N8	57	Full_diode	Testpin 4	Full diode with same array as array diode : 140 * 70 μm^2
P8	58	Temp_diode_p	Testpin 1	Temperature diode p side
Q8	59	Temp_diode_n	Testpin 2	Temperature diode n side
Q9	60	n.c.		
P9	61	n.c.		
N9	62	n.c.		
Q10	63	n.c.		
Q11	64	n.c.		
Q12	65	n.c.		
P10	66	n.c.		
N10	67	n.c.		
Q13	68	n.c.		
P11	69	Vpix	Supply 5V	Supply voltage pixel array : 5V

P12	70	Gnd	Ground	Ground of the sensor
N11	71	Vddr	Supply 5V	Supply voltage of the logic for the drivers : 5V
N12	72	n.c.		
P13	73	Vmem_l	Supply	Voltage supply for Vmemory drivers : 3V- 5V (typ: 4.5V)
N13	74	Vmem_h	Supply	Voltage supply for Vmemory drivers : 4V- 6V (typ. 6V)
M13	75	Vres_ds	Supply	Voltage supply for reset double sloped drivers : 4V – 5V
Q14	76	Vres	Supply	Voltage supply for reset drivers : 5V – 6V (typ 6V)
P14	77	Gnd_res	Ground_ab	Ground anti-blooming : 0 – 1V
L13	78	n.c.		
N14	79	n.c.		
M14	80	n.c.		
L14	81	n.c.		
Q15	82	n.c.		
K13	83	n.c.		
K14	84	n.c.		
P15	85	n.c.		
N15	86	n.c.		
M15	87	n.c.		
J13	88	n.c.		
L15	89	n.c.		
J14	90	n.c.		
K15	91	n.c.		
J15	92	n.c.		
H13	93	n.c.		
H14	94	Gnd	Ground	Ground for temperature module
H15	95	Temp	Testpin 5	Dark level signal as function of temperature (figure 7)
G15	96	Vdd	Supply	Supply voltage temperature module : 5V (has to be tunable to adjust output of temperature module to analog output)
G14	97	n.c.		
G13	98	n.c.		
F15	99	n.c.		
F14	100	n.c.		
E15	101	Reset_ds	Digital I/O	Double slope reset of the pixels: active high pulse
F13	102	Reset	Digital I/O	Reset signal of the pixels : active high pulse
E14	103	Mem_hl	Digital I/O	Control of Vmemory signal : 5V: Vmem_h, 0V : Vmem_l

D15	104	Sample	Digital I/O	Samples the photodiode voltage onto the memory cell inside each pixel : active high pulse
C15	105	Precharge	Digital I/O	Precharge the memory cell inside the pixel : active high pulse
E13	106	Eos_y	Digital I/O	End of scan signal of the y-register : active high pulse indicates the end of the shift register is reached
D14	107	Gnd_Res	Ground_ab	Ground for the reset drivers. Can be used as anti-blooming by applying 1V instead of 0V
B15	108	Vres	Supply	Voltage supply for reset drivers : 5V – 6V (typ: 6V)
C14	109	Vres_ds	Supply	Voltage supply for reset double sloped drivers : 4V – 5V
D13	110	Vmem_h	Supply	Voltage supply for Vmemory drivers : 5V- 6V (typ: 6V)
B14	111	Vmem_l	Supply	Voltage supply for Vmemory drivers : 3V- 5V (typ: 4.5V)
C13	112	Vddr	Supply 5V	Supply voltage of the logic for the drivers : 5V
C12	113	Vpix	Supply 5V	Supply voltage pixel array : 5V
C11	114	Vdd	Supply 5V	Supply voltage digital modules : 5V
B13	115	Gnd	Ground	Ground of the sensor
B11	116	n.c.		
B12	117	n.c.		
A15	118	n.c.		
C10	119	n.c.		
B10	120	n.c.		
A14	121	n.c.		
A13	122	n.c.		
A12	123	n.c.		
C9	124	n.c.		
B9	125	n.c.		
A11	126	Load_addr	Digital I/O	Loads the address into the serial parallel interface (SPI)
A10	127	Address	Digital I/O	Serial address to be downloaded into the SPI
A9	128	Clock_spi	Digital I/O	Clock for the SPI
C8	129	Decy_load	Digital I/O	Bias for y address register : 27KΩ to ground and capacitor of 100nF to Vdd
B8	130	Sync_y	Digital I/O	Synchronisation of y-address register : active high
A8	131	Clock_y	Digital I/O	Clock of y-address register
A7	132	Norow_sel	Digital I/O	Control signal for Norow_sel mode to reduce row blanking time : active low

B7	133	Sh_col	Digital I/O	Control signal for Sh_col mode to reduce row blanking time : active low (baseline method) : active low
C7	134	Pre_col	Digital I/O	Additional control signal for reducing the row blanking time
A6	135	Sync_x	Digital I/O	Synchronisation of the x-address register : active high
A5	136	Clock_x	Digital I/O	Clock of the x-address register
A4	137	Decx_load	Biasing	Bias for x address register : 27KΩ to ground and capacitor of 100nF to Vdd
B6	138	Black	Digital I/O	Controls black test function of the output stages : active high
C6	139	Sel_active	Digital I/O	set the output stages active or in standby mode : active low
A3	140	Vdd	Supply 5V	Supply voltage digital modules : 5V
B5	141	Gnd	Ground	Ground of the sensor
B4	142	Vdda	Supply 5V	Supply voltage analog modules : 5V
C5	143	Gnd	Ground	Ground of the sensor
C4	144	Voo	Supply 5V	Supply voltage output stages : 5V

Table 11 : pin description of the assembled LUPA-1300 sensor in the PGA 144 package.

6 Pad positioning and packaging

6.1 Package

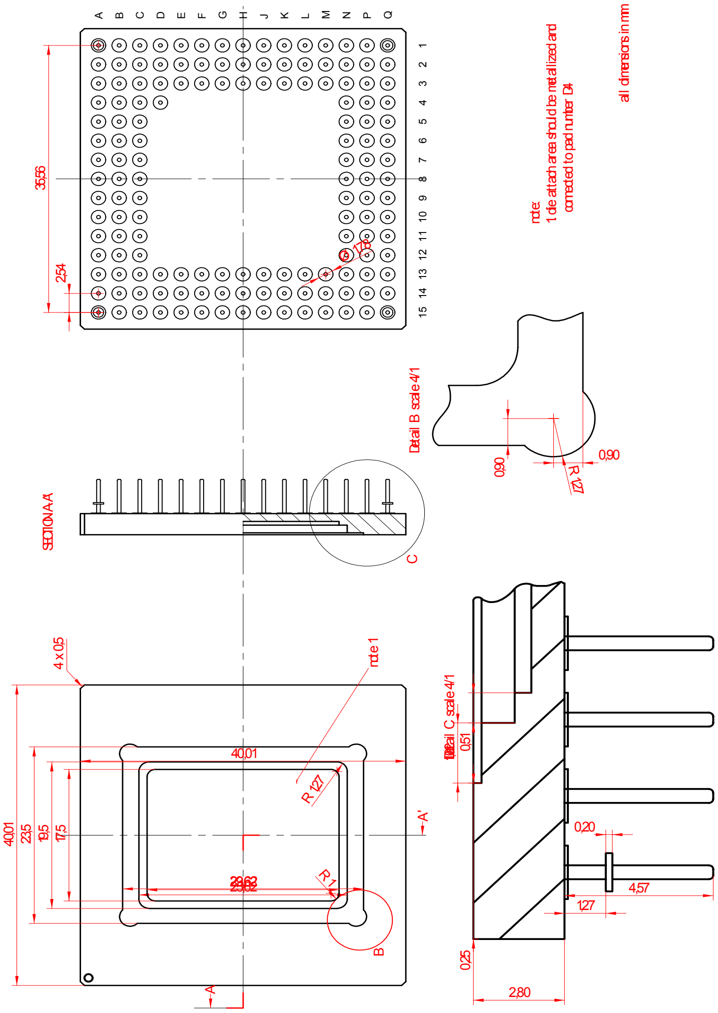

Figure 20: Package drawing of the LUPA-1300 sensor

6.2 Package and die

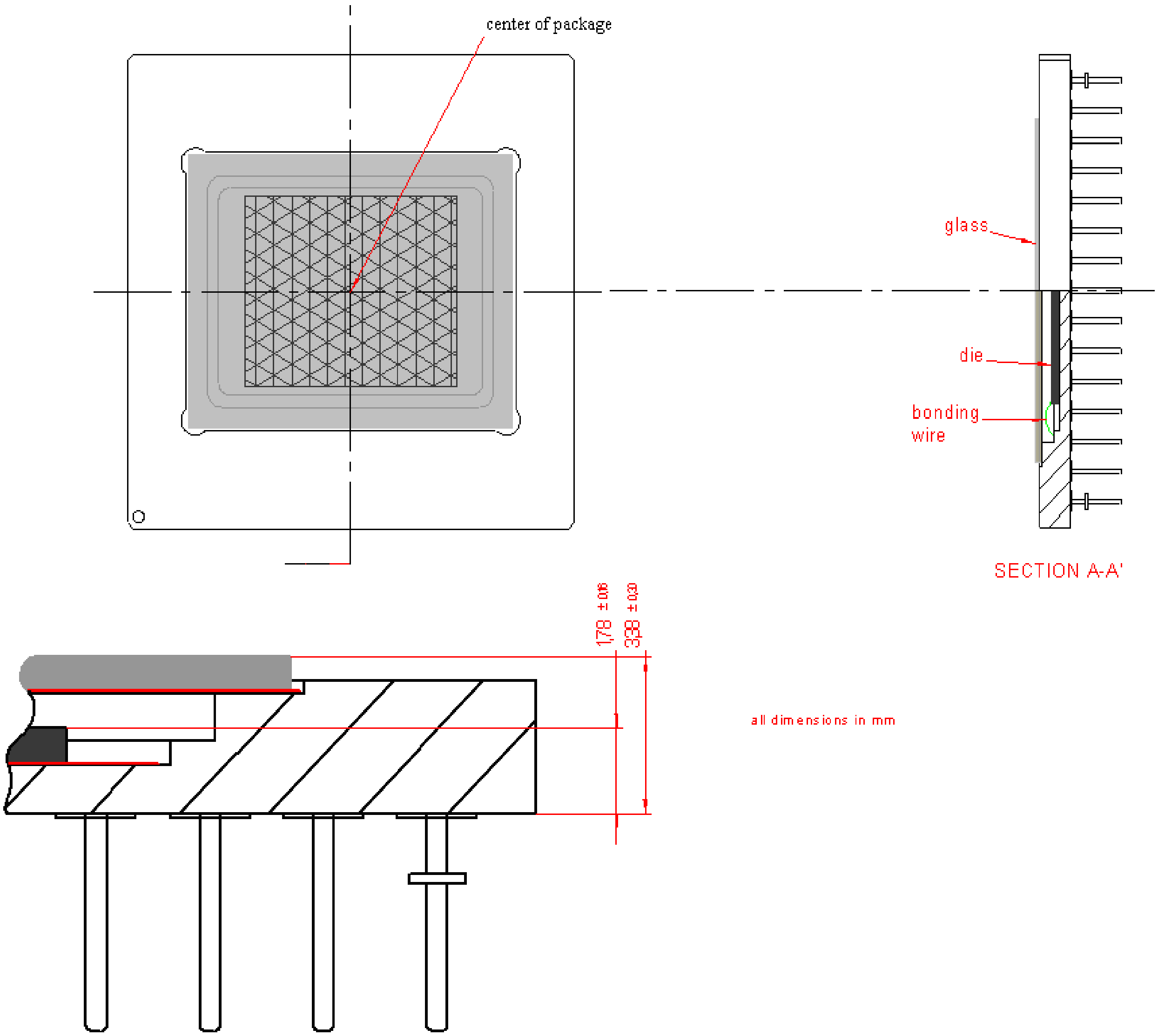

Figure 21: Package drawing with die of the LUPA-1300 sensor

The center of the pixel array is located 200 µm to the right and 51 µm above the center of the package. The first pixel is located at 9160 µm to the left and 7219 to the bottom from this center. All distances are with a deviation of 50 µm.

6.3 Color filter

An optional color filter can be processed as well.
The LUPA-1300 can also be processed with a Bayer RGB color pattern. Pixel (0,0) has a red filter.

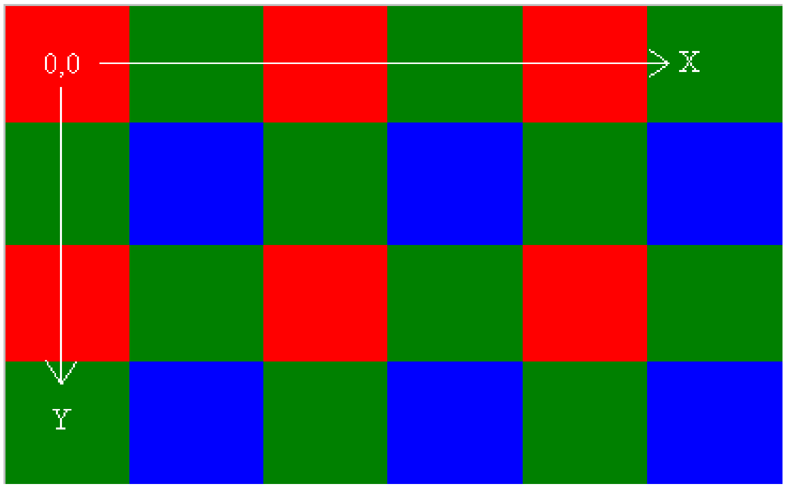

Figure 22: Color filter arrangement on the pixels.

6.4 Glass transmittance

6.4.1 Monochrome

A D263 glass will be used as protection glass lid on top of the LUPA-1300 monochrome sensors. Figure 23 shows the transmission characteristics of the D263 glass.

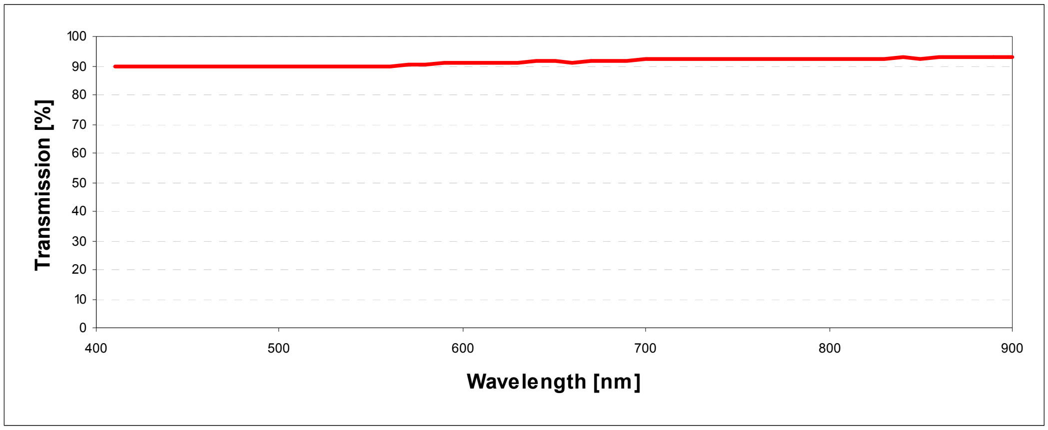

Figure 23: Transmission characteristics of the D263 glass used as protective cover for the IBIS5A-1300 sensors.

6.4.2 Color

For color devices a near infrared attenuating color filter glass is used. The dominant wavelength is around 490 nm. Figure 24 shows the transmittance curve for the glass. A S8612 glass will be used as NIR cut-off filter on top of the LUPA-1300-C color image sensor. Figure 24 shows the transmission characteristics of the S8612 glass.

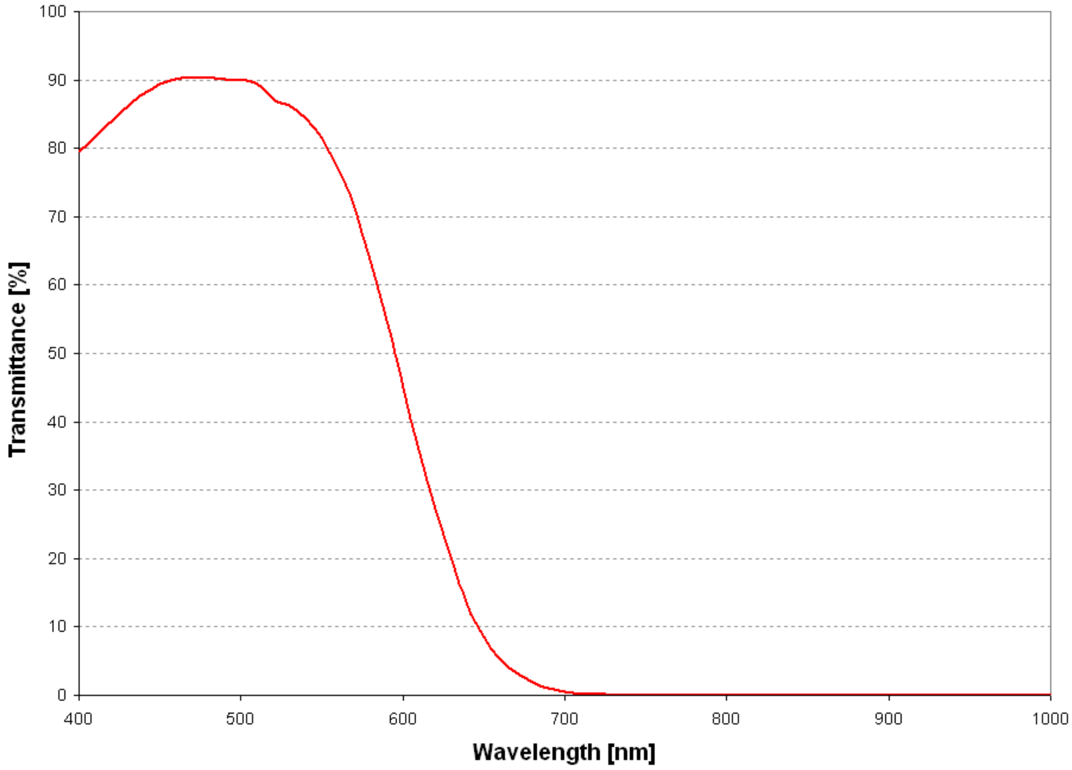

Figure 24: Transmission characteristics of the S8612 glass used as NIR cut-off filter.

6.5 Handling and Storage precautions

6.6 Handling precautions

Special care should be given when soldering image sensors with color filter arrays (RGB color filters), onto a circuit board, since color filters are sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the performance of the sensor. The following recommendations are made to ensure that sensor performance is not compromised during end-users' assembly processes.

Board Assembly:

Device placement onto boards should be done in accordance with strict ESD controls for Class 0, JESD22 Human Body Model, and Class A, JESD22 Machine Model devices. Assembly operators should always wear all designated and approved grounding equipment; grounded wrist straps at ESD protected workstations are recommended including the use of ionized blowers. All tools should be ESD protected.

Manual Soldering:

When a soldering iron is used the following conditions should be observed:

- Use a soldering iron with temperature control at the tip.

- The soldering iron tip temperature should not exceed 350°C.
- The soldering period for each pin should be less than 5 seconds.

Precautions and cleaning:
Avoid spilling solder flux on the cover glass; bare glass and particularly glass with antireflection filters may be adversely affected by the flux. Avoid mechanical or particulate damage to the cover glass.
It is recommended that isopropyl alcohol (IPA) be used as a solvent for cleaning the image sensor glass lid. When using other solvents, it should be confirmed beforehand whether the solvent will dissolve the package and/or the glass lid or not.

6.7 Storage conditions

Description	Minimum	Maximum	Units	Conditions
Temperature	-10	66	°C	@ 15% RH
Temperature	-10	38	°C	@ 86% RH

Note: RH = Relative Humidity

7 Ordering Information

FillFactory Part Number	Cypress Semiconductor Part Number
LUPA-1300-C	CYIL1SC1300AA-GAC
LUPA-1300-M	CYIL1SM1300AA-GBC

Disclaimer

FillFactory image sensors are only warranted to meet the specifications as described in the data sheet. Specifications are subject to change without notice.

8 Application notes & FAQ

Q: Can the LUPA-1300 directly drive an ADC?
A: Yes, coupling the LUPA-1300 to a set of 16 ADC's close to the chip is the preferred way of operation. A suitable ADC must have thus

- Input range equal or larger than the 1.2 V- 0 V sensor signal swing
- In view of the LUPA-1300's S/N 10 bits are suitable. 11 or 12 bits may be considered too.
- Input capacitance 20 pF or lower (high output loads will limit the speed). And no significant resistive loading.
- Sampling frequency 40 MHz (or the application specific sample rate)
- The ADC's input bandwidth must be sufficiently higher than the sampling frequency, in order to avoid RC contamination between successive pixels.

Q: How does the dual slope extended dynamic range mode works?
A:

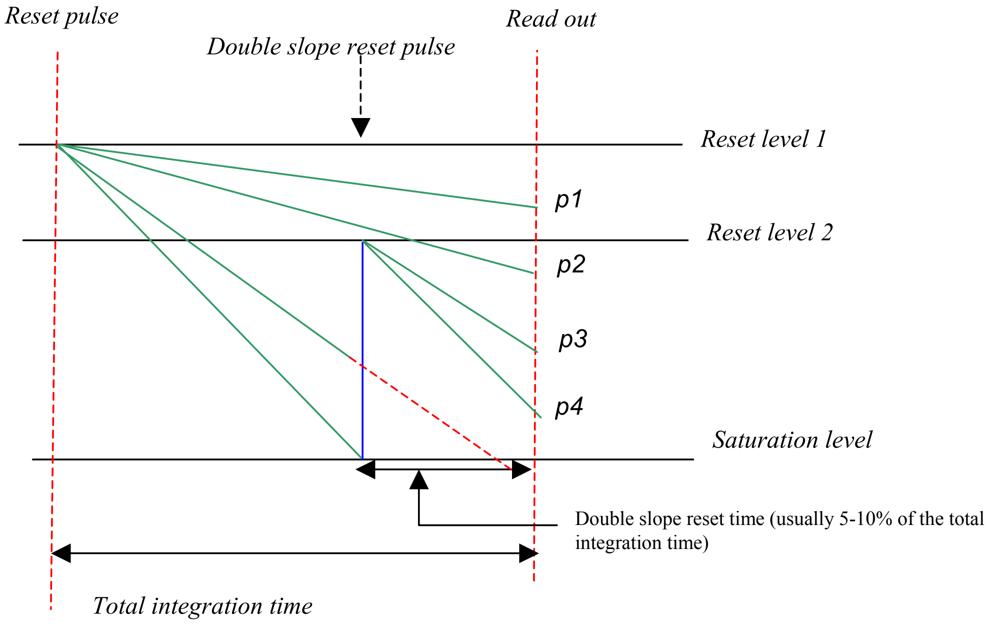

Figure 25: Dual slope diagram

The green lines are the analog signal on the photodiode, which decrease as a result of exposure. The slope is determined by the amount of light at each pixel (the more light the steeper the slope). When the pixels reach the saturation level the analog signal will not change despite further exposure. As you can see without any double slope pulse pixels p3 and p4 will reach saturation before the sample moment of the analog values, no signal will be acquired without double slope. When double slope is enabled a second reset pulse will be given (blue line) at a certain time before the end of the integration time. This double slope reset pulse resets the analog signal of the pixels BELOW this level to the reset level. After the reset the analog signal starts to decrease with the same slope as before the double slope reset pulse. If the double slope reset pulse is placed at the end of the integration time (90% for instance) the analog signal that would have reach the saturation levels aren't saturated anymore (this increases the optical dynamic range) at read out. It's important to notice that pixel signals above the double slope reset level will not be influenced by this double slope reset pulse (p1 and p2).

Please look at our website to find some pictures taken with the double slope mode on: http://www.fillfactory.be/htm/technology/htm/dual-slope.htm

APPENDIX A: LUPA-1300 Evaluation kit

For evaluating purposes a LUPA-1300 evaluation kit is available.

The LUPA-1300 evaluation kit consists of a multifunctional digital board (memory, sequencer and IEEE 1394 Fire Wire interface), an ADC-board and an analog image sensor board.

Visual Basic software (under Win 2000 or XP) allows the grabbing and display of images and movies from the sensor. All acquired images and movies can be stored in different file formats (8 or 16-bit). All setting can be adjusted on the fly to evaluate the sensors specs. Default register values can be loaded to start the software in a desired state.

Please contact Fillfactory (info@Fillfactory.com) if you want any more information on the evaluation kit.

Document History Page

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Document Number: 38-05711

Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	310396	See ECN	SIL	Initial Cypress release

(EOD)