

# **N-Channel Power MOSFET**

700V, 3.5A, 3.3Ω

#### **FEATURES**

- High power and current handling capability
- Pb-free plating
- RoHS compliant
- Halogen-free mold compound

KEY PERFORMANCE PARAMETERS				
PARAMETER	VALUE	UNIT		
$V_{DS}$	700	V		
R <sub>DS(on)</sub> (max)	3.3	Ω		
$Q_g$	14	nC		

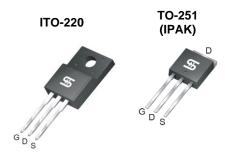
# Pb



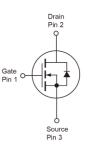


#### **APPLICATION**

- Power Supply
- Lighting







Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT		
			ITO-220	IPAK/DPAK	UNIT
Drain-Source Voltage		$V_{DS}$	700		V
Gate-Source Voltage		$V_{GS}$	±30		V
Continuous Drain Current (Note 1)	$T_C = 25^{\circ}C$	I <sub>D</sub>	2	3.5	А
	T <sub>C</sub> = 100°C		1.3	1.6	
Pulsed Drain Current (Note 2)		I <sub>DM</sub>	8	14	А
Total Power Dissipation @ T <sub>C</sub> = 25°C		$P_{DTOT}$	38	56	W
Single Pulsed Avalanche Energy (Note 3)		E <sub>AS</sub>	43		mJ
Single Pulsed Avalanche Current (Note 3)		I <sub>AS</sub>	3.5		А
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	- 55 to +150		°C

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	L		
	SYMBOL	ITO-220	IPAK/DPAK	UNIT
Junction to Case Thermal Resistance	R <sub>eJC</sub>	3.6	2.2	°C/W
Junction to Ambient Thermal Resistance	$R_{\Theta JA}$	62	50	°C/W

**Notes:**  $R_{\Theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\Theta JA}$  is guaranteed by design while  $R_{\Theta CA}$  is determined by the user's board design.  $R_{\Theta JA}$  shown below for single device operation on FR-4 PCB in still air



<b>ELECTRICAL SPECIFICATIONS</b> (T <sub>A</sub> = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV <sub>DSS</sub>	700			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	V <sub>GS(TH)</sub>	2		4	V
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	I <sub>GSS</sub>			±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 700V, V_{GS} = 0V$	I <sub>DSS</sub>			25	μA
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 2A$	R <sub>DS(on)</sub>		2.5	3.3	Ω
Dynamic (Note 5)						
Total Gate Charge	.,	Qg		14		
Gate-Source Charge	$V_{DS} = 480V, I_{D} = 4A,$	$Q_{gs}$		3		nC
Gate-Drain Charge	$V_{GS} = 10V$	$Q_{gd}$		6		
Input Capacitance	.,	C <sub>iss</sub>		595		
Output Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1.0MHz	C <sub>oss</sub>		80		pF
Reverse Transfer Capacitance	7 I = 1.0IVIDZ	C <sub>rss</sub>		20		
Switching (Note 6)						
Turn-On Delay Time		t <sub>d(on)</sub>		18		
Turn-On Rise Time	$V_{DD} = 300V,$ $R_{GEN} = 25\Omega,$ $I_{D} = 4A, V_{GS} = 10V,$	t <sub>r</sub>		17		
Turn-Off Delay Time		t <sub>d(off)</sub>		40.5		ns
Turn-Off Fall Time	- 1D - +Λ, VGS - 10V,	t <sub>f</sub>		19		
Source-Drain Diode (Note 4)						
Forward On Voltage	I <sub>S</sub> = 2.5A, V <sub>GS</sub> = 0V	$V_{SD}$			1.5	V

#### Notes:

- 1. Current limited by package
- 2. Pulse width limited by the maximum junction temperature
- 3. L = 7mH,  $I_{AS} = 3.5A$ ,  $V_{DD} = 50V$ ,  $R_G = 25\Omega$ , Starting  $T_J = 25^{\circ}C$
- 4. Pulse test: PW ≤ 300µs, duty cycle ≤ 2%
- 5. For DESIGN AID ONLY, not subject to production testing.
- 6. Switching time is essentially independent of operating temperature.





## **ORDERING INFORMATION**

PART NO.	PACKAGE	PACKING
TSM4N70CI C0G	ITO-220	50pcs / Tube
TSM4N70CH C5G	TO-251 (IPAK)	75pcs / Tube
TSM4N70CP ROG	TO-252 (DPAK)	2,500pcs / 13" Reel

#### Note:

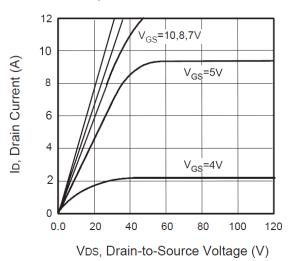
- 1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- 2. Halogen-free according to IEC 61249-2-21 definition



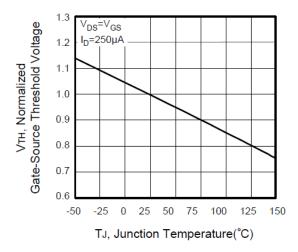
#### **CHARACTERISTICS CURVES**

 $(T_C = 25^{\circ}C \text{ unless otherwise noted})$ 

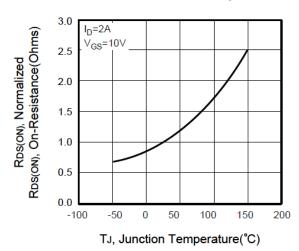
#### **Output Characteristics**



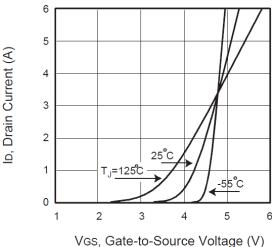
#### Normalized Vth vs. Junction Temperature



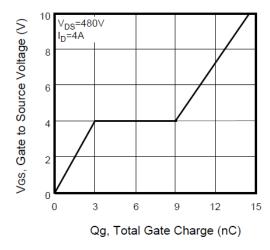
#### **On-Resistance Variation vs. Temperature**



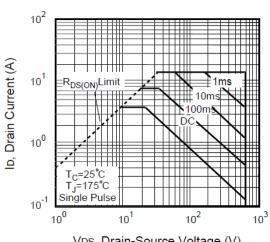
#### **Transfer Characteristics**



# **Gate Charge**



#### **Maximum Safe Operating Area (ITO-220)**



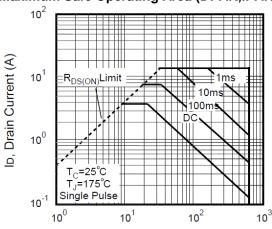
VDS, Drain-Source Voltage (V)



#### **CHARACTERISTICS CURVES**

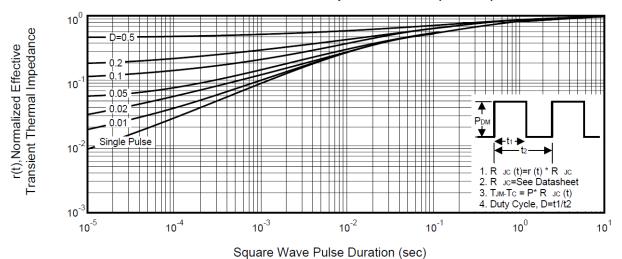
 $(T_C = 25^{\circ}C \text{ unless otherwise noted})$ 

#### Maximum Safe Operating Area (DPAK,IPAK)

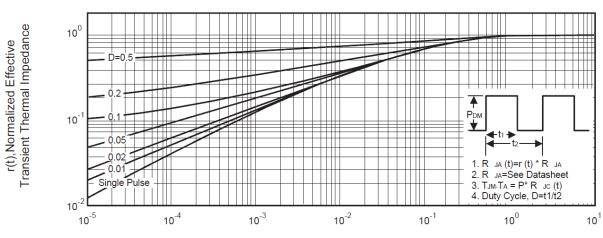


VDS, Drain-Source Voltage (V)

#### **Normalized Thermal Transient Impedance Curve (ITO-220)**



#### Normalized Thermal Transient Impedance Curve (DPAK,IPAK)

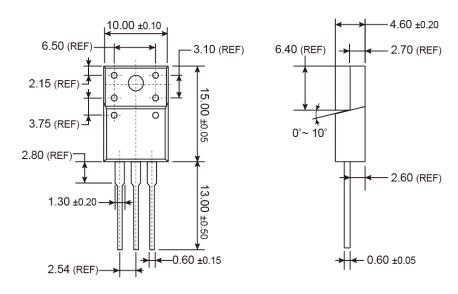


Square Wave Pulse Duration (sec)

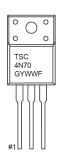


# PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

#### **ITO-220**



#### **MARKING DIAGRAM**



**G** = Halogen Free

Y = Year Code

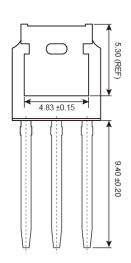
**WW** = Week Code (01~52)

**F** = Factory Code

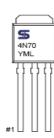


# PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

# TO-251 (IPAK) 1.02 (REF) 0.53 ±0.05 1.07 ±0.10 0.53 (BSC)



#### **MARKING DIAGRAM**



Y = Year Code

**M** = Month Code for Halogen Free Product

O =Jan P =Feb Q =Mar R =Apr

S =May T =Jun U =Jul V =Aug

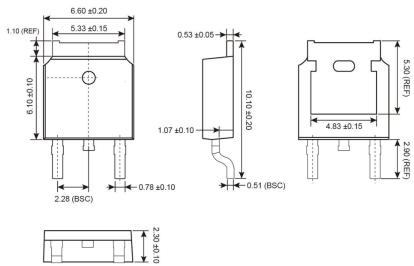
W =Sep X =Oct Y =Nov Z =Dec

L = Lot Code (1~9, A~Z)

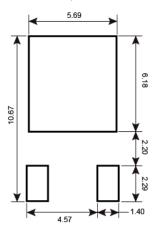


#### PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

#### **TO-252 (DPAK)**



## SUGGESTED PAD LAYOUT (Unit: Millimeters)



#### **MARKING DIAGRAM**



Y = Year Code

M = Month Code for Halogen Free Product

O =Jan **P** =Feb

**Q** =Mar

R =Apr

**S** =May

**T** =Jun

**U** =Jul

V =Aug

W =Sep

X =Oct

Y =Nov

**Z** =Dec

 $L = \text{Lot Code } (1\sim 9, A\sim Z)$ 





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