

### **Product Features**

- · GaN on SiC Chip on Board
- Surface Mount Hybrid Type
- Asymmetric Doherty Amplifier
- · High Efficiency
- No Matching circuit needed

### **Applications**

- RF Sub-Systems
- · Base Station
- RRH
- 4G/LTE system
- Small cell



# **Description**

Accommodating the future of 4G/LTE small cells, RFHIC introduces RTH18007-10 amplifier fabricated using an advanced high power density Gallium Nitride (GaN) semiconductor process. This high performance amplifier achieves high efficiency of 45%, and powers 7W over the frequency range from 1805MHz to 1880MHz. Integrated with Asymmetrical Doherty configurations, RTH Series is packaged in a very small form-factor 28 x 19 x 4.8mm on AIN (aluminum nitride) board which provides excellent thermal dissipation.

### **Electrical Specifications** @ Vds =31V, Ta=25 °C

PARAMETER	UNIT	MIN TYP MAX		CONDITION	
Frequency Range	MHz	1805	-	1880	ZS = ZL = 50  ohm
Power Gain		14	16	-	
Gain Flatness	dB	-3.0	-	3.0	Carrier Idq = 160mA
Input Return Loss		-6	-9	-	Vgp = -4.7V
Pout @ Average	dBm	-	38.5	-	
Pout @ Psat	dBm	46	47	-	Pulse Width=20us, Duty10%
ACLR @ BW 10MHz	dBc	-	-27	-	Non DPD
LTE (PAPR 7.5dB)		-	-53	-	With DPD
Drain Efficiency	%	40	45	-	
Carrier Idq	4	-	220	-	Pout @ Average
Total Ids	mA	-	500	-	
		-	-3.0	-2.0	Vgc
Supply Voltage	V	-	-5.0	-4.0	Vgp
		30.5	31	-	Vds

#### Caution

The drain voltage must be supplied to the device after the gate voltage is supplied

Turn on: Turn on the Gate voltage supply and last turn on the Drain voltage supplies

Turn off: Turn off the Drain voltage and last turn off the Gate voltage

#### Note

1. ACLR Measured Pout=38.5dBm @ fc± 10MHz / 9.015MHz

LTE 10MHz 1FA PAPR=7.5dB @ 0.01% probability on CCDF, (DPD Engine: Optichron OP6180)

# **Mechanical Specifications**

PARAMETER	UNIT	ТҮР	REMARK
Mass	g	5	-
Dimension	mm	28 x 19 x 4.8	-

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Version 1.0



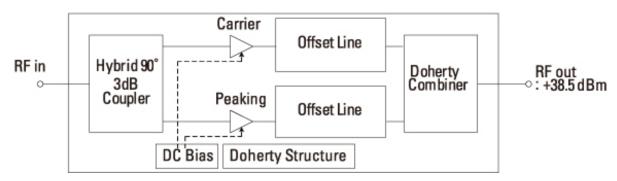
# **Absolute Maximum Ratings**

PARAMETER	UNIT	RATING	SYMBOL
Gate-Source Voltage	V	-10 ~ 0	Vgc Vgp
Drain-Source Voltage	V	50	Vds
Gate Current	mA	4.0	Igs
<b>Operating Junction Temperature</b>	°C	225	$T_{\mathrm{J}}$
Operating Case Temperature	°C	-30 ~ 85	$T_{C}$
Storage Temperature	°C	-40 ~ 100	$T_{STG}$

# **Operating Voltages**

PARAMETER	UNIT	MIN	ТҮР	MAX	SYMBOL
Drain Voltage	V	30.5	31	-	Vds
Gate Voltage (on-stage)	V	-	Vgc @Carrier Idq	-2	Vgc
Gate Voltage (on-stage)	V	-	Vgp	-2	Vgp
Gate Voltage (off-stage)	V	-	-8	-	Vgc
Gate Voltage (off-stage)	V	-	-8	-	Vgp

# **Block Diagram**

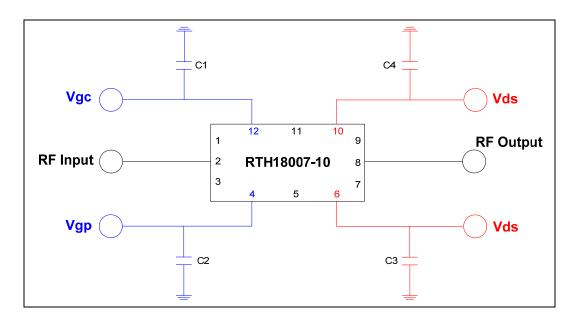


\*Note

 $Directional\ coupler,\ is olator\ and\ drive\ amplifier\ MUST\ be\ located\ CLOSE\ to\ the\ DUT (device\ under\ test)\ is\ needed\ for\ best\ performance.$ 



# **Application Circuit**



# **Part List**

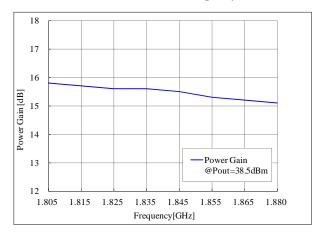
Location	Model No.	Spec.	Maker	
C3, C4	1812C225K101CT	2.2uF / 100V	WALSIN	
C1, C2	C3216X7R1C106K	10uF / 16V	TDK	
Evaluation Board	RO4350B	2Layer, 30mil	ROGERS	



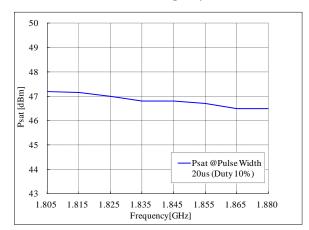
### **Performance Charts**

\* Bias condition @ Carrier Idq= 160mA, Vgp= 4.7V, Ta=25  $^{\circ}$ C

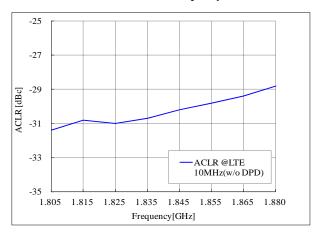
#### Power Gain vs. Frequency



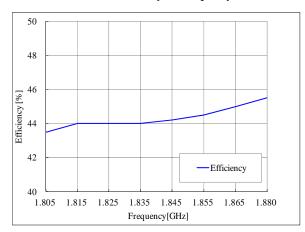
#### Psat vs. Frequency



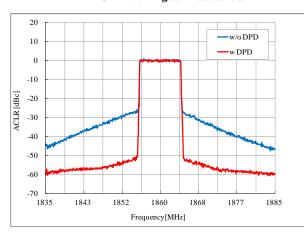
**ACLR vs. Frequency** 



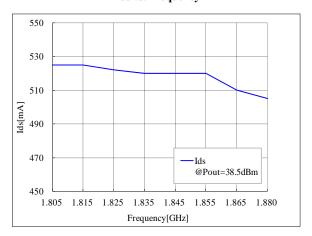
**Drain Efficiency vs. Frequency** 



**ACLR** with Digital Predistortion



Ids vs. Frequency

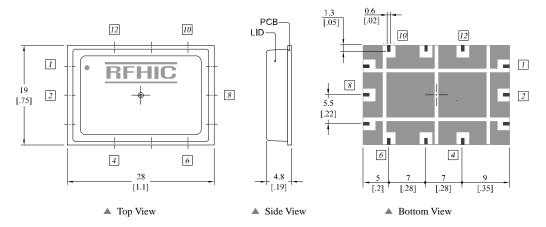


<sup>\*</sup>DPD Engine: Optichron OP6180



## Package Dimensions (Type: NP-8CL)

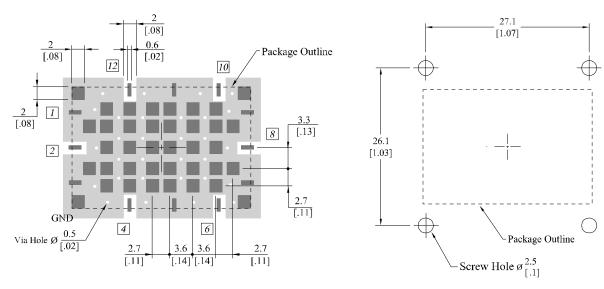
\* Unit: mm[inch] | Tolerance: ±0.15[.008]



Pin Description								
Pin No	Function	Pin No	Function	Pin No	Function	Pin No	Function	
1	GND	4	Vgp	7	GND	10	Vds	
2	RF Input	5	GND	8	RF Output	11	GND	
3	GND	6	Vds	9	GND	12	Vgc	

### **Recommended Pattern**

# **Recommended Mounting Configuration**



#### \* Mounting Configuration Notes

- 1. For the proper performance of the device, Ground / Thermal via holes must be designed to remove heat.
- 2. To properly use heatsink, ensure the ground/thermal via hole region to contact the heatsink. We recommend the mounting screws be added near the heatsink to mount the board
- 3. In designing the necessary RF trace, width will depend upon the PCB material and construction.
- 4. Use 1 oz. Copper minimum thickness for the heatsink.
- 5. Do not put solder mask on the backside of the PCB in the region where the board contacts the heatsink
- 6. We recommend adding as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.



### **Precautions**

This product is a Gallium Nitride Transistor.

The Gallium Nitride Transistor requires a Negative Voltage Bias which operates alongside a Positive Voltage Bias. These Biases are applied in accordance to the Sequence during Turn-On and Turn-Off.

The Pallet Amplifier does not have a built-in Bias Sequence Circuit. Therefore, users need to either apply positive voltages and negative voltages in the required sequence, or add an external Bias Circuit to this Amplifier.

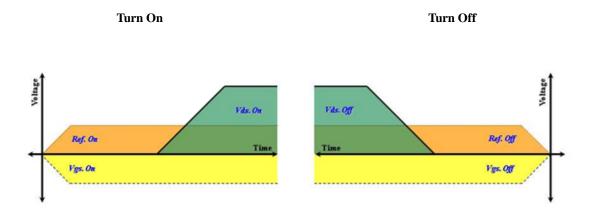
The required sequence for power supply is as follows.

## **During Turn-On**

- 1. Connect GND.
- 2. Apply Gate Voltage (Vgc and Vgp)
- 3. Apply Drain Voltage (Vds)
- 4. Apply the RF Power.

## **During Turn-Off**

- 1. Turn off RF power.
- 2. Turn off Drain Voltage (Vds), and then, turn off the Gate Voltage (Vgc and Vgp)
- 3. Remove all connections.



- Sequence Timing Diagram -



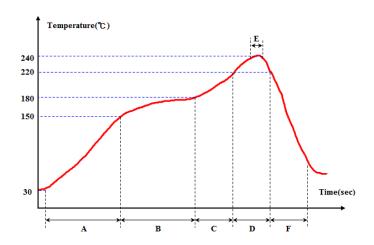
#### **Reflow Profile**

### \* Reflow oven settings

Zone	A	В	С	D	E	F
Temperature(°C)	30 ~ 150 ℃	150 ~ 180 ℃	180 ~ 220 ℃	220 ~ 220 ℃	235 ~ 240 ℃	2 ~ 6 °C/ Sec Drop
Belt speed	55 ~ 115 sec	55 ~ 75 sec	30 ~ 50 sec	30 ~ 50 sec	5 ~ 10 sec	60 ~ 90 sec

Reflow Cycle Limit= 1time

#### \* Measured reflow profile



## **Ordering Information**

Part Number	Package Design	
	-R (Reel)	
RTH18007-10	-B (Bulk)	
	-EVB (Evaluation Board)	

# **Revision History**

Part Number	Release Date	Version	Modification	Data Sheet Status
RTH18007-10	2013.11.15	1.0	Electrical specifications (1p)	-
RTH18007-10	2013.02.25	0.5	Package Dimension	Preliminary
RTH18007-10	2013.01.15	0.3	Application circuit	Preliminary

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