∗RP105Q (SC-88A) is the discontinued product as of June, 2016.

RICOH

RP105x Series

Low Voltage 400 mA LDO Regulator

NO.EA-179-160420

OUTLINE

The RP105x is a 400 mA output type CMOS-based voltage regulator with capability of low input voltage (Min. 0.9 V) and low output voltage (Min. 0.6 V). This device is remarkably improved the performance at low input voltage compared with conventional low voltage LDOs, and two power supply voltage type. (Another power source, V_{BIAS} pin voltage must be Min. 2.4 V). The device consists of a voltage reference unit, an error amplifier, resistor-net for voltage setting, a current limit circuit to avoid the destruction, a UVLO circuit with monitoring input voltage, and so on.

The RP105x has the ultra-low on resistance output driver, the on resistance is Typ. 0.4 Ω (V_{OUT} = 0.8 V, I_{OUT} = 300 mA). The built-in driver is Nch MOSFET, thus the load transient response is excellent, (under the condition of the current between 1 mA and 400 mA, tr = 0.5 μs, the undershoot level is approximately 50 mV).

The output voltage of this device is fixed with high accuracy. Since the packages for the device are DFN(PLP)1212-6, DFN1212-5, SOT-23-5 and SC-88A therefore high density mounting of the IC on boards is possible.

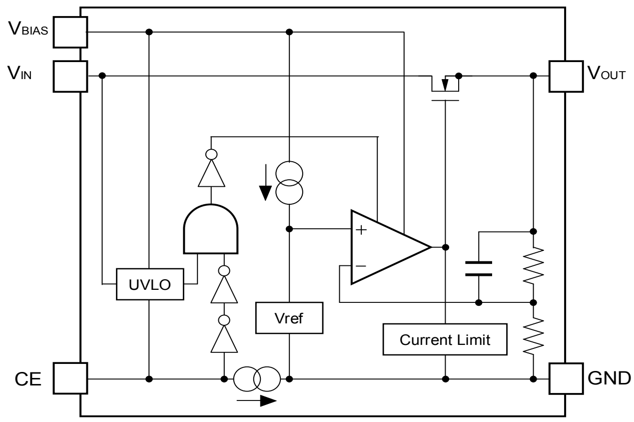
FEATURES

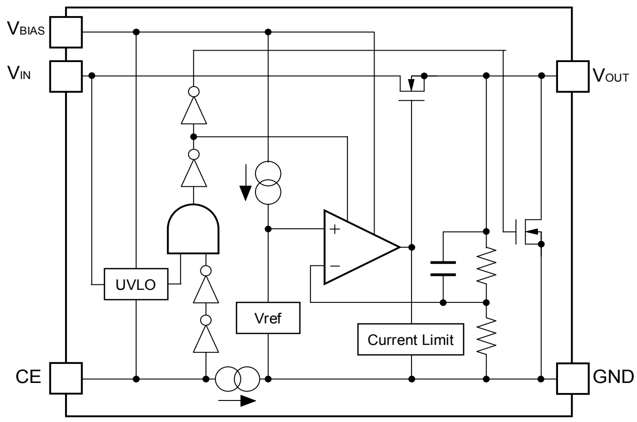
- Supply Current .... Typ. 28 μA
- Standby Current .... Typ. 0.1 μA
- Ripple Rejection .... Typ. 80 dB (f = 1 kHz, V_{IN} Ripple)
  Typ. 50 dB (f = 1 kHz, V_{BIAS} Ripple)
- Output Voltage Range .... 0.6 V to 1.5 V (0.1 V step)
  Contact Ricoh sales representatives for other voltages.
- Input Voltage Range (V_{BIAS}) .... 2.4 V to 5.25 V (V_{OUT} < 0.8 V)
  Set V_{OUT} + 1.6 V to 5.25 V (V_{OUT} ≥ 0.8 V)
- Input Voltage Range (V_{IN}) .... RP105xxxxB/D: 0.9 V to V_{BIAS} (V_{OUT} < 0.8 V)
  Set V_{OUT} + 0.1 V to V_{BIAS} (V_{OUT} ≥ 0.8 V)
  RP105xxxxE/F: 0.9 V to V_{BIAS}
- Output Voltage Accuracy .... Typ. ±15 mV (Ta = 25°C)
- Temperature-Drift Coefficient of Output Voltage ...... Typ. ±50 ppm/°C
- Dropout Voltage .... DFN1212-5: Typ. 105 mV
  (I_{OUT} = 400 mA, V_{OUT} = 1.5 V, V_{BIAS} = 3.6 V)
- Line Regulation .... Typ. 0.02%/V
- Packages .... DFN(PLP)1212-6, SC-88A, SOT-23-5, DFN1212-5
- Built-in Fold Back Protection Circuit .... Typ. 120 mA (Current at short mode)
- Ceramic capacitors are recommended .... C_{BIAS} = C_{IN} = 1.0 μF or more, C_{OUT} = 2.2 μF or more

APPLICATIONS

- Power source for battery-powered equipment.
- Power source for electrical appliances such as cameras, VCRs and camcorders.
- Power source for portable communication equipment.

BLOCK DIAGRAMS





SELECTION GUIDE

The output voltage, the UVLO circuit, the auto-discharge function[1], the package, and the taping type for the device are user-selectable options.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP105Kxx1∗-TR	DFN(PLP)1212-6	5,000 pcs	Yes	Yes
RP105Qxx2∗-TR-FE [2]	SC-88A	3,000 pcs	Yes	Yes
RP105Nxx1∗-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes
RP105Lxx1∗-TR	DFN1212-5	5,000 pcs	Yes	Yes

xx : The set output voltage (V_{SET}) can be designated within the range of 0.6 V (06) to 1.5 V (15) in 0.1 V step.

If the set output voltage (V_{SET}) is designated in 0.01 V step, indicate the product name as follows.
1.05 V: RP105x10x∗5-TR

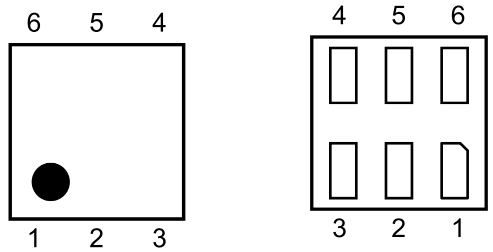
∗ : CE pin polarity and auto-discharge function of the product can be defined as follows.
(B) "H" active, auto-discharge function is not included, UVLO is included
(D) "H" active, auto-discharge function is included, UVLO is included
(E) "H" active, auto-discharge function is not included, UVLO is not included
(F) "H" active, auto-discharge function is included, UVLO is not included

[1] Auto-discharge function quickly lowers the output voltage to 0 V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.
[2] RP105Qxx2∗-TR-FE supports only RP105Qxx2B/D.

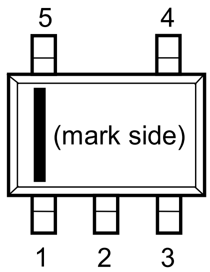
PIN DESCRIPTIONS

● DFN(PLP)1212-6

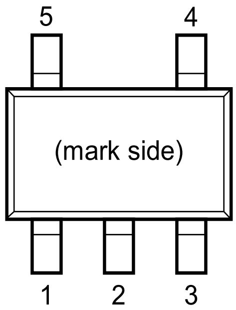
Mark Side   Bump Side



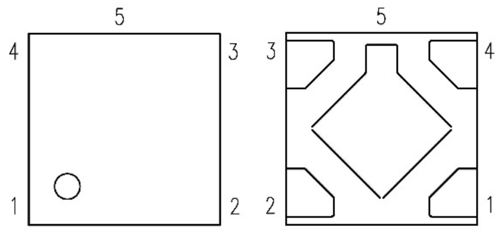
● SC-88A



● SOT-23-5



● DFN1212-5



● DFN(PLP)1212-6

Pin No	Symbol	Pin Description
1	V_{BIAS}	Input Pin 1
2	GND	Ground Pin
3	CE	Chip Enable Pin ("H" Active)
4	V_{IN}	Input Pin 2
5	NC	No Connection
6	V_{OUT}	Output Pin

● SC-88A

Pin No	Symbol	Pin Description
1	V_{BIAS}	Input Pin 1
2	GND	Ground Pin
3	V_{OUT}	Output Pin
4	V_{IN}	Input Pin 2
5	CE	Chip Enable Pin ("H" Active)

● **SOT-23-5**

Pin No	Symbol	Pin Description
1	V_{IN}	Input Pin 2
2	GND	Ground Pin
3	CE	Chip Enable Pin ("H" Active)
4	V_{BIAS}	Input Pin 1
5	V_{OUT}	Output Pin

● **DFN1212-5**

Pin No	Symbol	Pin Description
1	V_{OUT}	Output Pin
2	V_{BIAS}	Input Pin 1
3	CE	Chip Enable Pin ("H" Active)
4	V_{IN}	Input Pin 2
5	GND	Ground Pin

ABSOLUTE MAXIMUM RATINGS

Symbol	Item		Rating	Unit
V_{BIAS}	Input Voltage		6.0	V
V_{IN}	Input Voltage (for Driver)		−0.3 to V_{BIAS} + 0.3	V
V_{CE}	Input Voltage (CE Pin)		6.0	V
V_{OUT}	Output Voltage		−0.3 to V_{IN} + 0.3	V
I_{OUT}	Output Current		500	mA
P_D	Power Dissipation (Standard Test Land Pattern)[1]	DFN(PLP)1212-6	400	mW
		SC-88A	380	
		SOT-23-5	420	
		DFN1212-5	650	
Ta	Operating Temperature		−40 to 85	°C
Tstg	Storage Temperature		−55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

[1] Refer to *POWER DISSIPATION* for detailed information.

ELECTRICAL CHARACTERISTICS

V_{BIAS} = V_{CE} = 3.6 V, V_{IN} = Set V_{OUT} + 0.5 V, I_{OUT} = 1 mA, C_{BIAS} = C_{IN} = 1.0 μF, C_{OUT} = 2.2 μF, unless otherwise noted.
The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP105x (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{OUT}	Output Voltage	Ta = 25°C	Set V_{OUT} −15 mV		Set V_{OUT} + 15 mV	V
		−40°C ≤ Ta ≤ 85°C	Set V_{OUT} −20 mV		Set V_{OUT} + 20 mV	V
I_{OUT}	Output Current		400			mA
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation (K, Q, N package)	1 mA ≤ I_{OUT} ≤ 400 mA		30	50	mV
	Load Regulation (L package)	1 mA ≤ I_{OUT} ≤ 400 mA		15	35	mV
V_{DIF}	Dropout Voltage	Refer to *PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS*				
I_{SS}	Supply Current	I_{OUT} = 0 mA		28	40	μA
Istandby	Standby Current	V_{CE} = 0 V		0.1	3.0	μA
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	2.4 V ≤ V_{BIAS} ≤ 5.0 V		0.02	0.1	%/V
		Set V_{OUT} + 0.3 V ≤ V_{IN} ≤ 2.4 V		0.02	0.1	
RR	Ripple Rejection	I_{OUT} = 30 mA, f = 1 kHz, V_{IN} Ripple 0.2 Vp-p		80		dB
		I_{OUT} = 30 mA, f = 1 kHz, V_{BIAS} Ripple 0.2 Vp-p		50		
V_{BIAS}	Input Voltage(1)	V_{OUT} < 0.8 V	2.4		5.25	V
		V_{OUT} ≥ 0.8 V	Set V_{OUT} + 1.6		5.25	
V_{IN}	Input Voltage (for Driver)(1)	RP105xxxxB/D, V_{OUT} < 0.8 V	0.9		V_{BIAS}	V
		RP105xxxxB/D, V_{OUT} ≥ 0.8 V	Set V_{OUT} + 0.1		V_{BIAS}	
		RP105xxxxE/F	0.9		V_{BIAS}	
$\Delta V_{OUT}/\Delta Ta$	Output Voltage Temperature Coefficient	−40°C ≤ Ta ≤ 85°C		±50		ppm /°C
I_{SC}	Short Current Limit	V_{OUT} = 0 V		120		mA
I_{CEPD}	CE Pull-down Current			1.0		μA

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C) except Output Noise, Ripple Rejection and Output Voltage Temperature Coefficient.

(1) The maximum Input Voltage listed under Electrical Characteristics is 5.25 V. If for any reason the input voltage exceeds 5.25 V, it has to be no more than 5.5 V with 500 hours of the total operating time.

ELECTRICAL CHARACTERISTICS (continued)

V_{BIAS} = V_{CE} = 3.6 V, V_{IN} = Set V_{OUT} + 0.5 V, I_{OUT} = 1 mA, C_{BIAS} = C_{IN} = 1.0 µF, C_{OUT} = 2.2 µF, unless otherwise noted.
The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C.

RP105x (Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V_{CEH}	CE Input Voltage "H"		0.8			V
V_{CEL}	CE Input Voltage "L"				0.3	V
$V_{IN\ UVLO}$	V_{IN} Under Voltage Lock Out (only B/D version)	I_{OUT} = 1.0 µA		Set V_{OUT} + 50 mV	Set V_{OUT} + 100 mV	V
tdelay	Detector Delay Time (only B/D version)			100		µs
en	Output Noise	BM = 10 Hz to 100 kHz I_{OUT} = 30 mA, Set V_{OUT} = 0.6 V		70		µVrms
R_{LOW}	Nch On Resistance For auto-discharge (only D/F version)	V_{BIAS} = 3.6 V, V_{CE} = "L"		50		Ω

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj ≈ Ta = 25°C) except Output Noise, Ripple Rejection and Output Voltage Temperature Coefficient.

DFN(PLP)1212-6, SC-88A, SOT-23-5

The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C

PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS

Set V_{OUT} (V)	V_{BIAS} (V)	V_{GS} (V)	V_{DIF} (I_{OUT} = 300 mA) (V)		V_{DIF} (I_{OUT} = 400 mA) (V)	
			Typ.	Max.	Typ.	Max.
0.6	3.6	3.0	0.115	0.180	0.180	0.320
0.7	3.6	2.9	0.120	0.190	0.180	0.320
0.8	3.6	2.8	0.120	0.190	0.180	0.300
0.9	3.6	2.7	0.120	0.190	0.180	0.300
1.0	3.6	2.6	0.120	0.190	0.180	0.280
1.1	3.6	2.5	0.120	0.190	0.180	0.280
1.2	3.6	2.4	0.130	0.200	0.180	0.280
1.3	3.6	2.3	0.130	0.200	0.180	0.260
1.4	3.6	2.2	0.130	0.200	0.180	0.260
1.5	3.6	2.1	0.130	0.200	0.180	0.260

PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS (V_{GS} (V), V_{DIF} (V), I_{OUT} = 200 mA) (Ta = 25°C)

Set V_{OUT} (V)	V_{BIAS} = 2.5 V		V_{BIAS} = 3.0 V		V_{BIAS} = 3.3 V		V_{BIAS} = 3.6 V		V_{BIAS} = 4.2 V		V_{BIAS} = 5.0 V	
	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)
0.6	1.9	-	2.4	-	2.7	-	3.0	-	3.6	-	4.4	-
0.7	1.8	-	2.3	-	2.6	-	2.9	-	3.5	-	4.3	-
0.8	1.7	0.098	2.2	0.093	2.5	0.093	2.8	0.092	3.4	0.092	4.2	0.092
0.9	1.6	0.098	2.1	0.094	2.4	0.093	2.7	0.092	3.3	0.092	4.1	0.092
1.0			2.0	0.094	2.3	0.093	2.6	0.092	3.2	0.092	4.0	0.092
1.1			1.9	0.096	2.2	0.094	2.5	0.094	3.1	0.093	3.9	0.093
1.2			1.8	0.098	2.1	0.096	2.4	0.095	3.0	0.095	3.8	0.094
1.3			1.7	0.098	2.0	0.096	2.3	0.095	2.9	0.095	3.7	0.095
1.4			1.6	0.098	1.9	0.096	2.2	0.095	2.8	0.095	3.6	0.095
1.5					1.8	0.096	2.1	0.095	2.7	0.095	3.5	0.095

All of units are tested and specified under load conditions such that Tj ≈ Ta = 25°C except for Output Noise, Ripple Rejection and Output Voltage Temperature Coefficient items.

(diagonally hatched cell): V_{BIAS} pin voltage must be equal or more than Set V_{OUT} + 1.6 V.

DFN1212-5

The specifications surrounded by ☐ are guaranteed by design engineering at −40°C ≤ Ta ≤ 85°C

PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS

Set V_{OUT} (V)	V_{BIAS} (V)	V_{GS} (V)	V_{DIF} (I_{OUT} = 300 mA) (V)		V_{DIF} (I_{OUT} = 400 mA) (V)	
			Typ.	Max.	Typ.	Max.
0.6	3.6	3.0	-	-	-	-
0.7	3.6	2.9	-	-	-	-
0.8	3.6	2.8	0.077	0.130	0.105	0.170
0.9	3.6	2.7	0.077	0.130	0.105	0.170
1.0	3.6	2.6	0.077	0.130	0.105	0.170
1.05	3.6	2.55	0.077	0.130	0.105	0.170
1.1	3.6	2.5	0.077	0.130	0.105	0.170
1.2	3.6	2.4	0.077	0.130	0.105	0.170
1.3	3.6	2.3	0.077	0.130	0.105	0.170
1.4	3.6	2.2	0.077	0.130	0.105	0.170
1.5	3.6	2.1	0.077	0.130	0.105	0.170

PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS (V_{GS} (V), V_{DIF} (V), I_{OUT} = 200 mA) (Ta = 25°C)

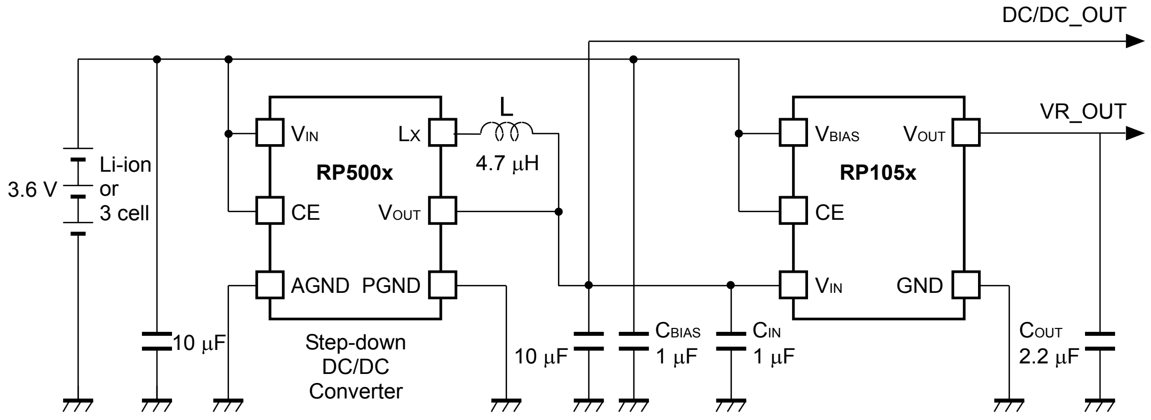
Set V_{OUT} (V)	V_{BIAS} = 2.5 V		V_{BIAS} = 3.0 V		V_{BIAS} = 3.3 V		V_{BIAS} = 3.6 V		V_{BIAS} = 4.2 V		V_{BIAS} = 5.0 V	
	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)	V_{GS} (V)	V_{DIF} (V)
0.6	1.9	-	2.4	-	2.7	-	3.0	-	3.6	-	4.4	-
0.7	1.8	-	2.3	-	2.6	-	2.9	-	3.5	-	4.3	-
0.8	1.7	-	2.2	-	2.5	-	2.8	-	3.4	-	4.2	-
0.9	1.6	0.059	2.1	0.054	2.4	0.053	2.7	0.051	3.3	0.050	4.1	0.048
1.0			2.0	0.054	2.3	0.053	2.6	0.051	3.2	0.050	4.0	0.048
1.05			1.95	0.054	2.25	0.053	2.55	0.051	3.15	0.050	3.95	0.048
1.1			1.9	0.054	2.2	0.053	2.5	0.051	3.1	0.050	3.9	0.048
1.2			1.8	0.054	2.1	0.053	2.4	0.051	3.0	0.050	3.8	0.048
1.3			1.7	0.054	2.0	0.053	2.3	0.051	2.9	0.050	3.7	0.048
1.4			1.6	0.054	1.9	0.053	2.2	0.051	2.8	0.050	3.6	0.048
1.5					1.8	0.053	2.1	0.051	2.7	0.050	3.5	0.048

All of units are tested and specified under load conditions such that Tj ≈ Ta = 25°C except for Output Noise, Ripple Rejection and Output Voltage Temperature Coefficient items.

(hatched cell) V_{BIAS} pin voltage must be equal or more than Set V_{OUT} + 1.6 V.

APPLICATION INFORMATION

TYPICAL APPLICATION



External Components

Symbol	Descriptions
C_{OUT}	2.2 µF, Ceramic Capacitor, GRM155B30J225ME15, MURATA
C_{BIAS}, C_{IN}	1.0 µF, Ceramic Capacitor, GRM155B31A105KE15, MURATA

TECHNICAL NOTES

UVLO (Undervoltage Lockout)

In RP105xxxxB/D, UVLO detects and turns off the output when the input voltage V_{IN} drops lower than or equal to V_{SET} + 50 mV (Typ) while CE = “H”. Since RP105xxxxE/F does not have UVLO, it continues to output even if V_{IN} drops to V_{SET} + 50 mV (Typ) or lower.

When V_{IN} drops below the set output voltage V_{SET}, UVLO does not turn off the output in RP105xxxxE/F while CE = “H”, therefore the current flows from V_{BIAS} pin to V_{IN} pin via the inside IC. This will not be generated in RP105xxxxB/D since UVLO turns off the output when V_{IN} is lower than or equal to V_{SET} + 50 mV (Typ).

Phase Compensation

In this device, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use a capacitor for C_{OUT} with the capacity of equal or more than 2.2 μF.

If tantalum capacitors are connected as C_{OUT}, and if the equivalent series resistance (ESR) value is large, the operation might be unstable. Because of this, test the device with as same external components as ones to be used on the PCB.

PCB Layout

Make V_{BIAS}, V_{IN}, and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect a capacitor with a capacitance value as much as 1.0 μF or more between V_{BIAS} pin and GND, between V_{IN} pin and GND, and as close as possible to the pins.

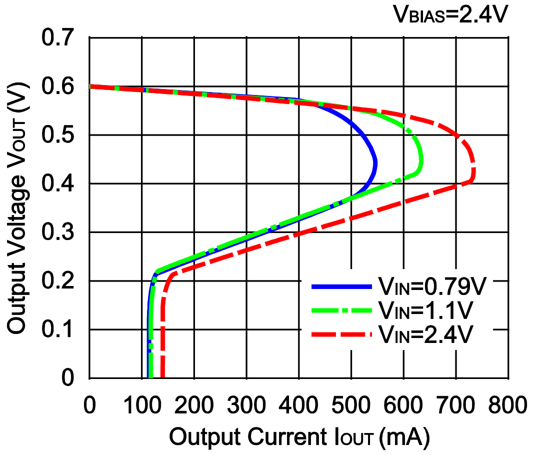
Set external components, especially the output capacitor, as close as possible to the device, and make wiring as short as possible. V_{IN} source is supposed to be the output of the DC/DC converter. The value should be equal or lower than V_{BIAS} voltage.

TYPICAL CHARACTERISTICS

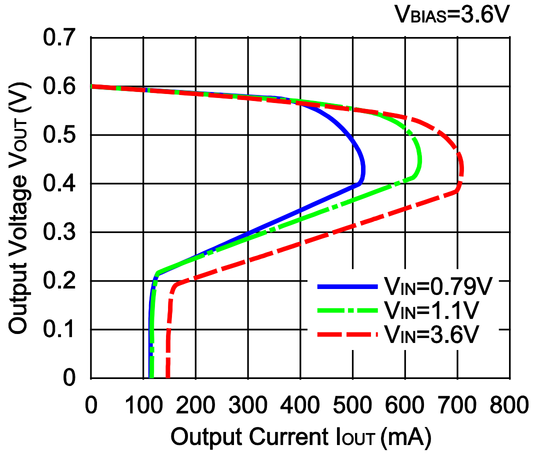
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Output Voltage vs. Output Current (C_{BIAS} = 1.0 µF, C_{IN} = C_{OUT} = 2.2 µF, Ta = 25°C)

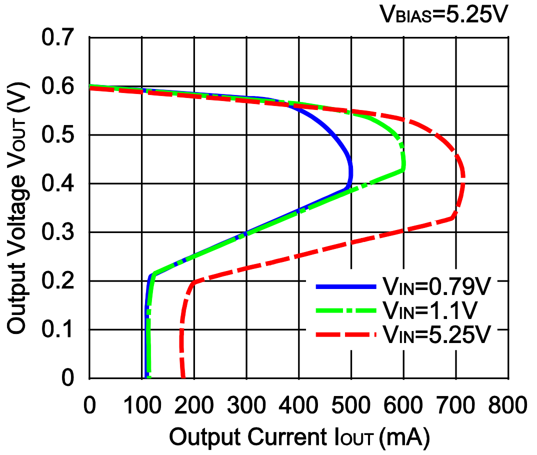
RP105x06xx



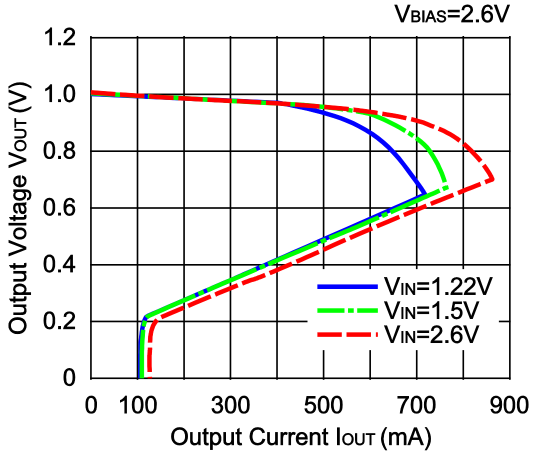
RP105x06xx



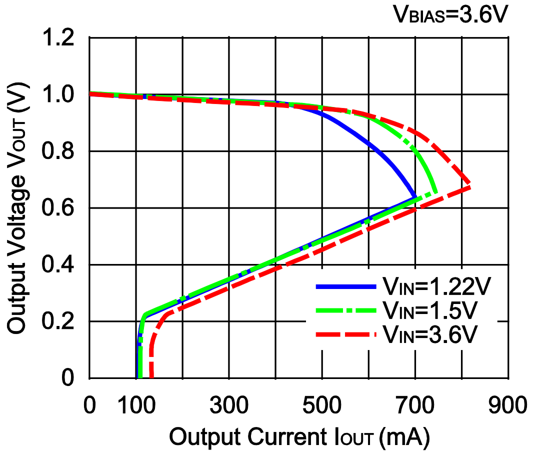
RP105x06xx



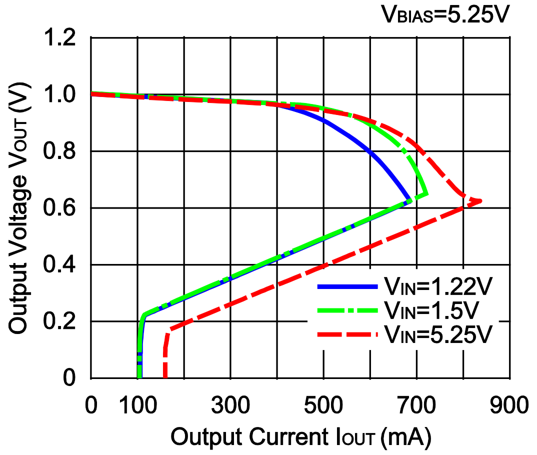
RP105x10xx



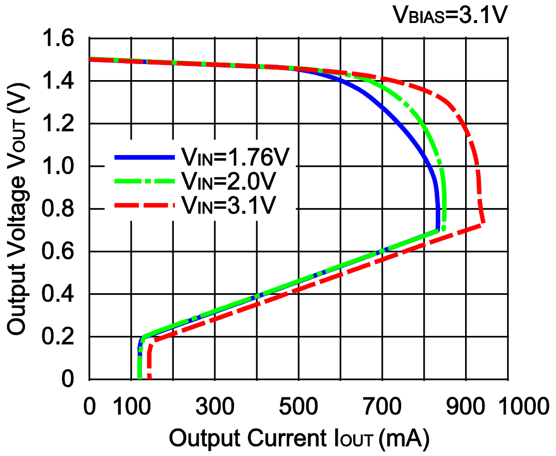
RP105x10xx



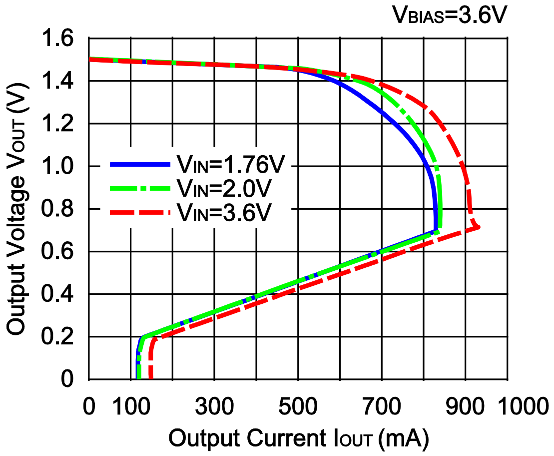
RP105x10xx



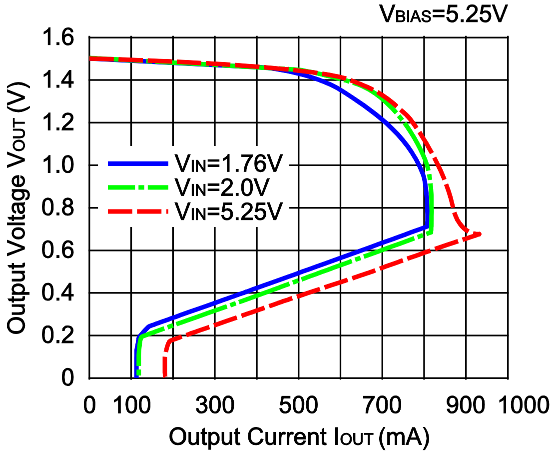
RP105x15xx



RP105x15xx

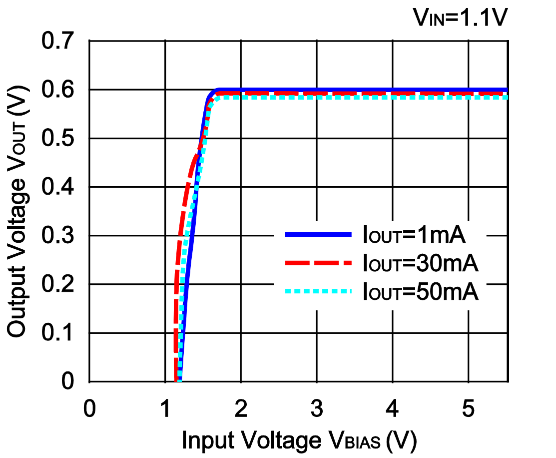


RP105x15xx

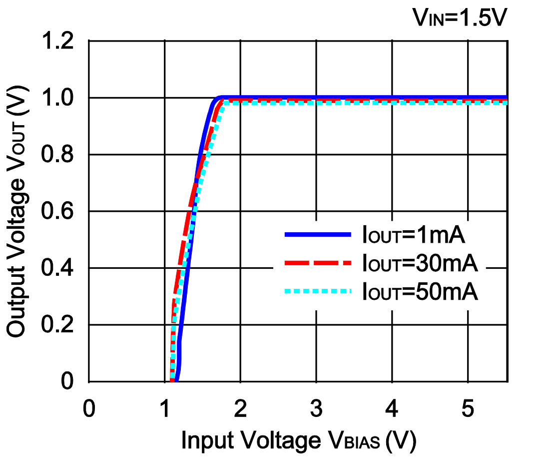


2) Output Voltage vs. Input Voltage (C_{BIAS} = 1.0 μF, C_{IN} = C_{OUT} = 2.2 μF, Ta = 25°C)

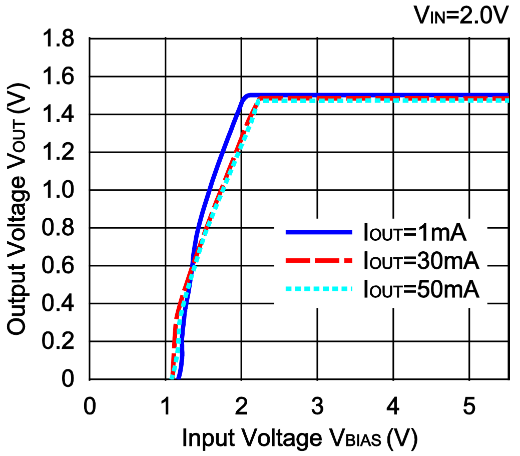
RP105x06xx



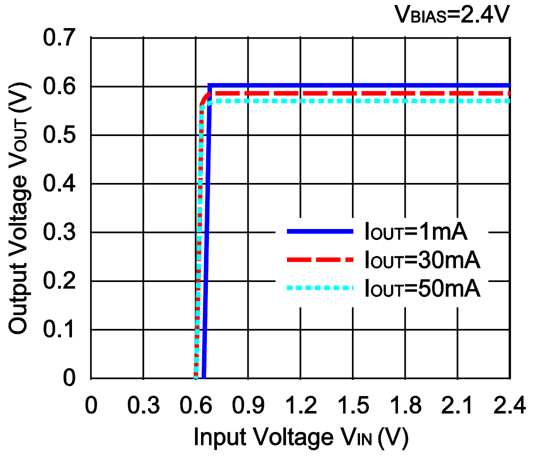
RP105x10xx



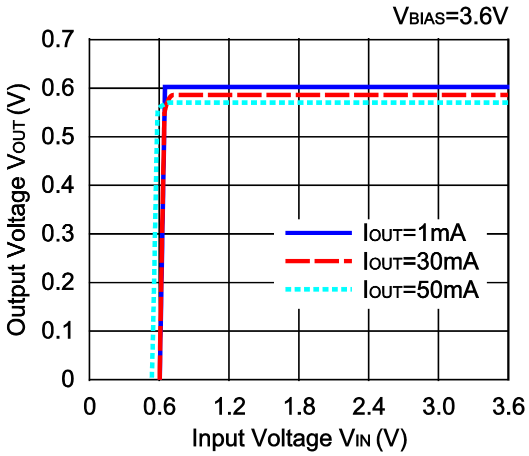
RP105x15xx



RP105x06xB/D



RP105x06xB/D



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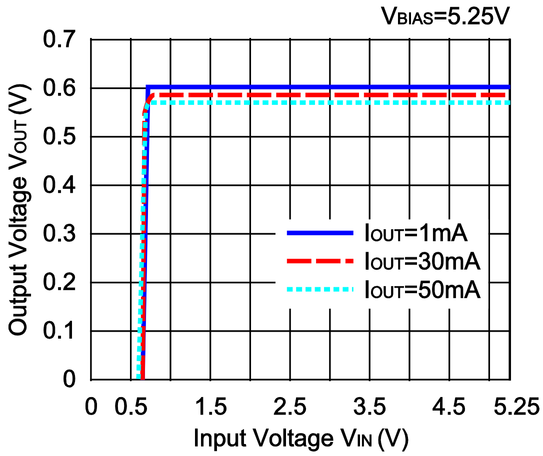

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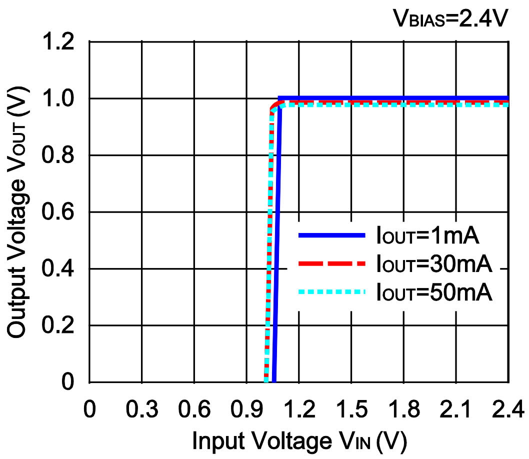

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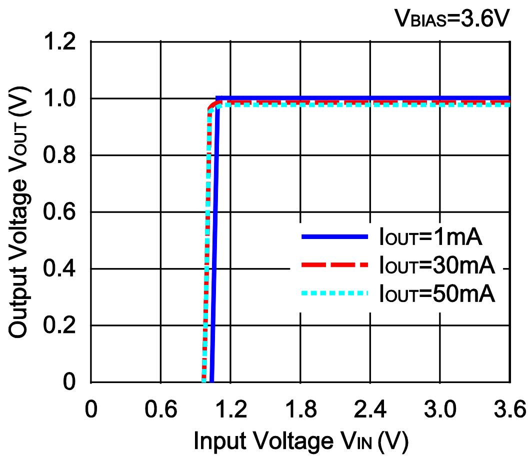

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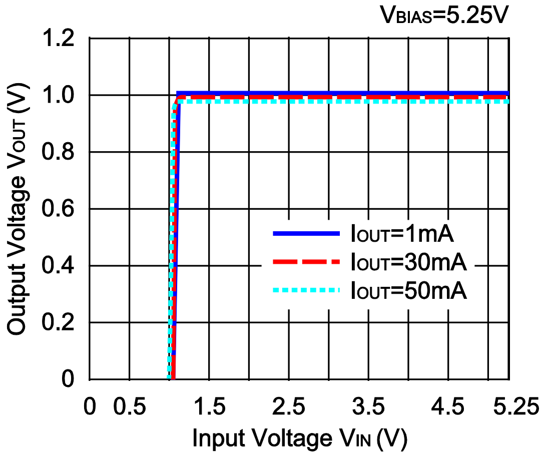

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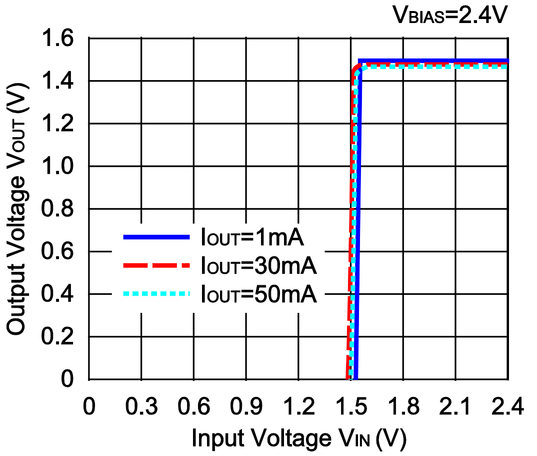
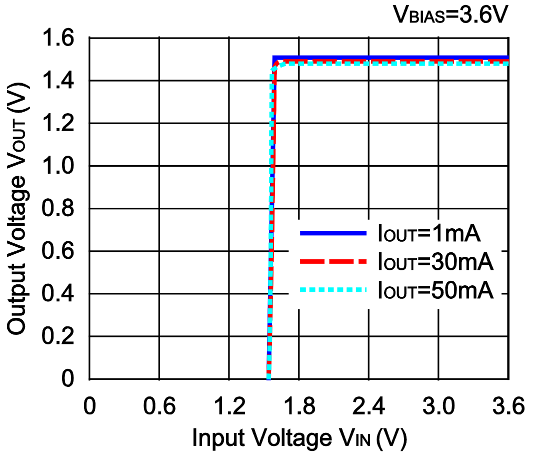


RP105x15xB/D



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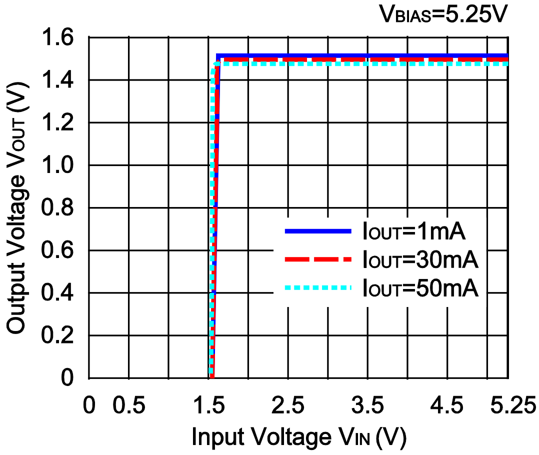

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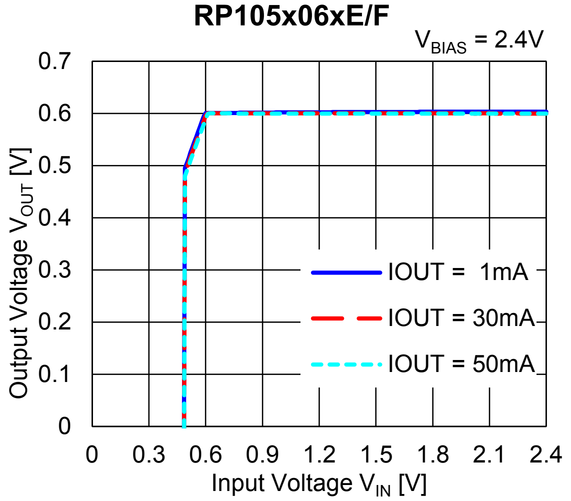

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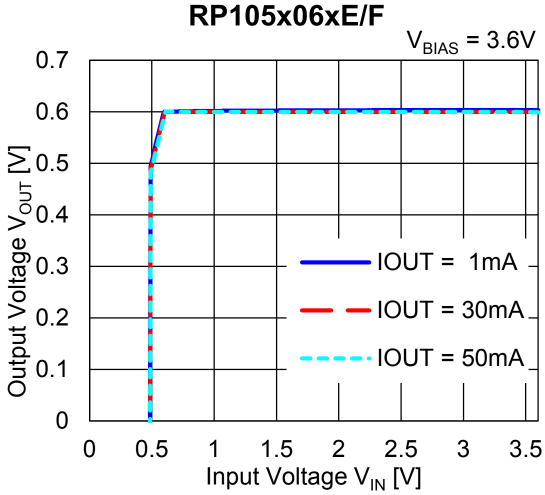

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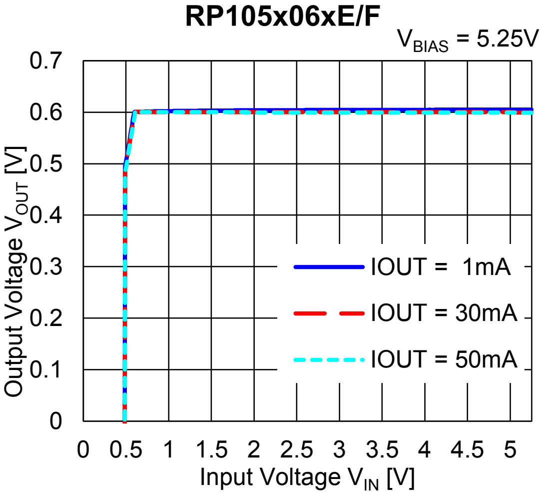
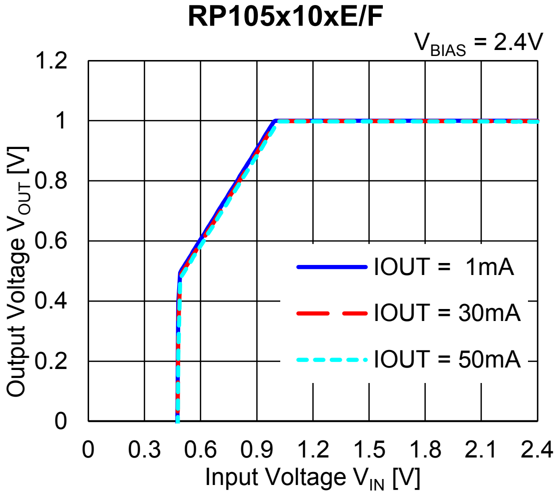
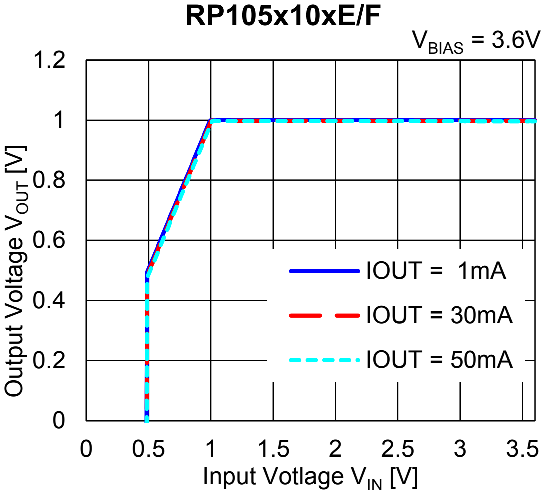


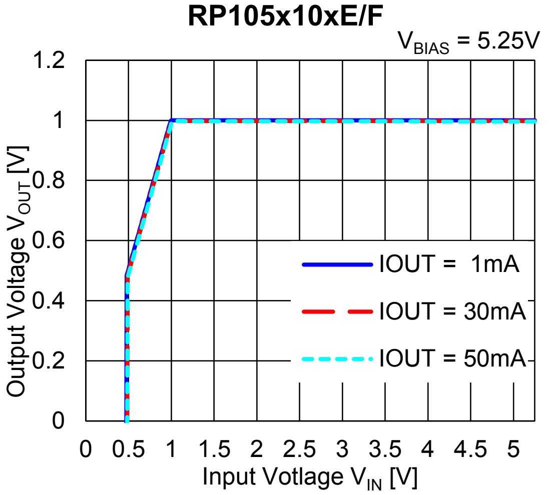
RP105x10xE/F



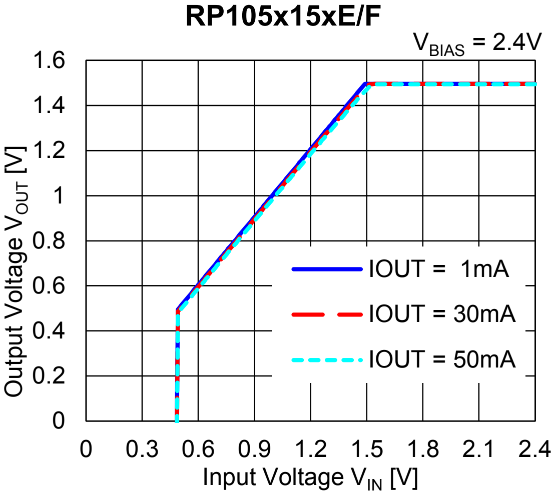
RP105x10xE/F



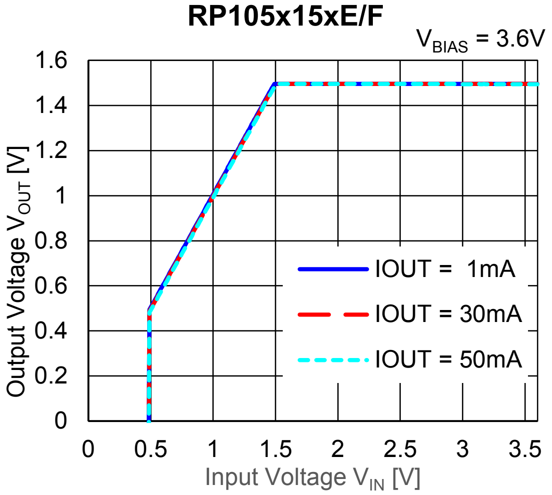
RP105x10xE/F

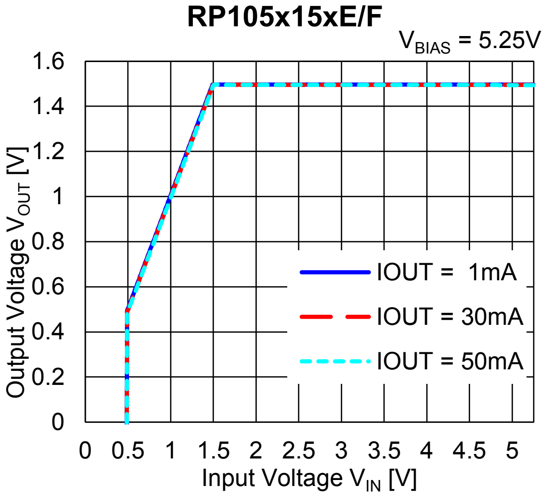


RP105x15xE/F

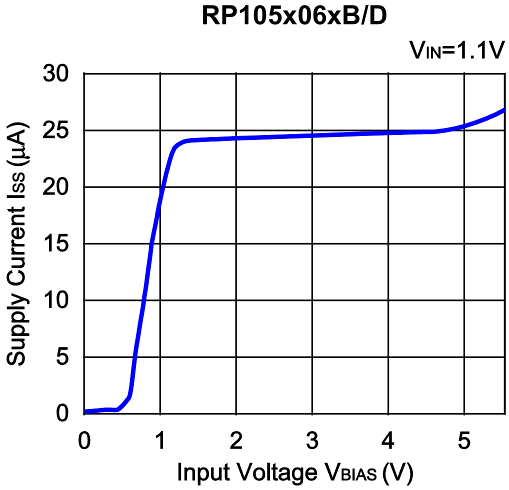


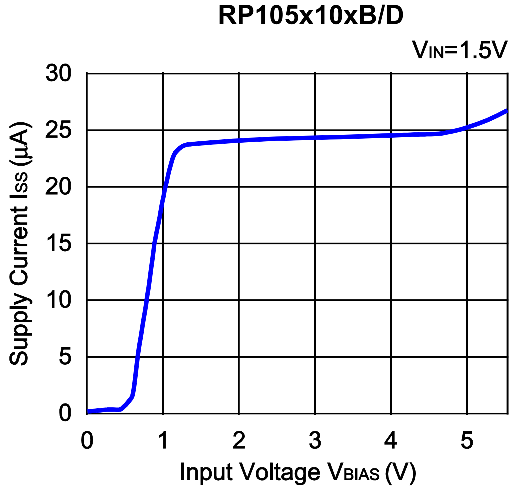
RP105x15xE/F

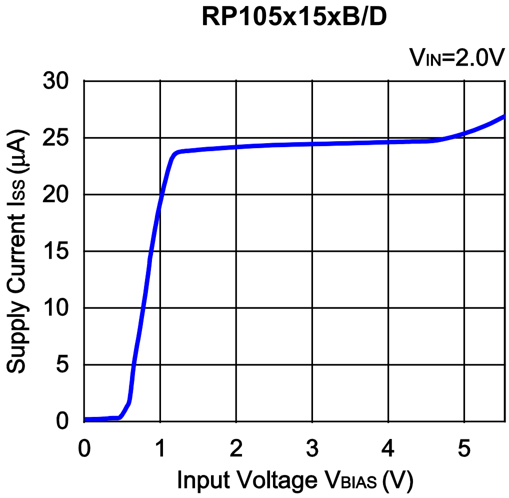


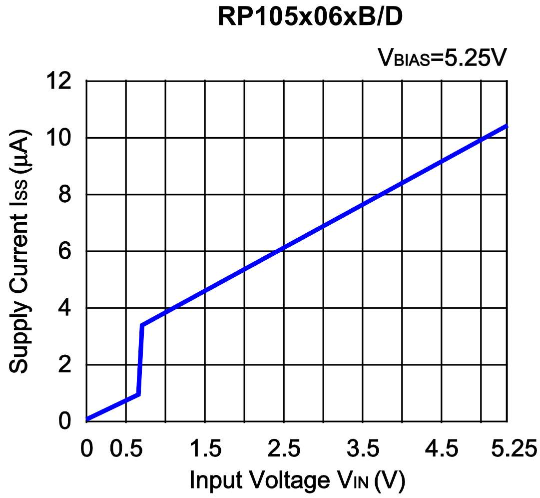


3) Supply Current vs. Input Voltage (C_{BIAS} = C_{IN} = C_{OUT} = none, Ta = 25°C)

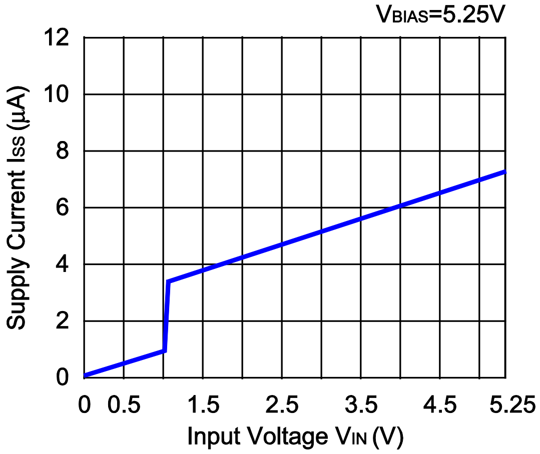




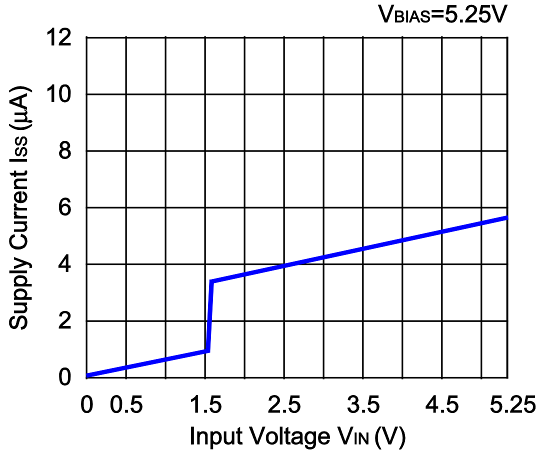




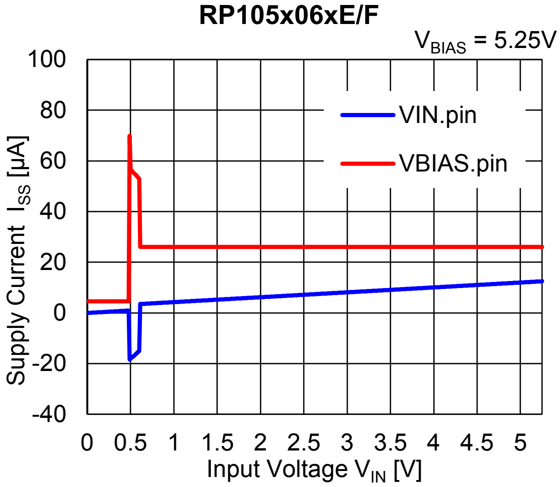
RP105x10xB/D



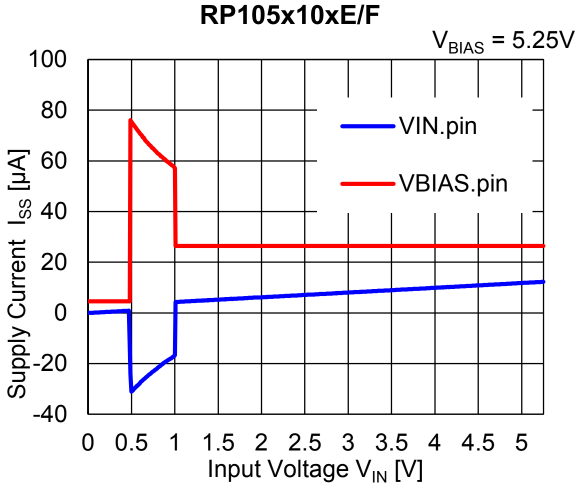
RP105x15xB/D



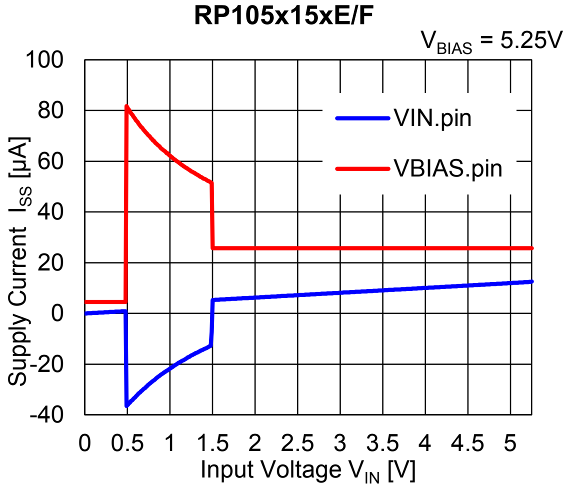
RP105x06xE/F



RP105x10xE/F



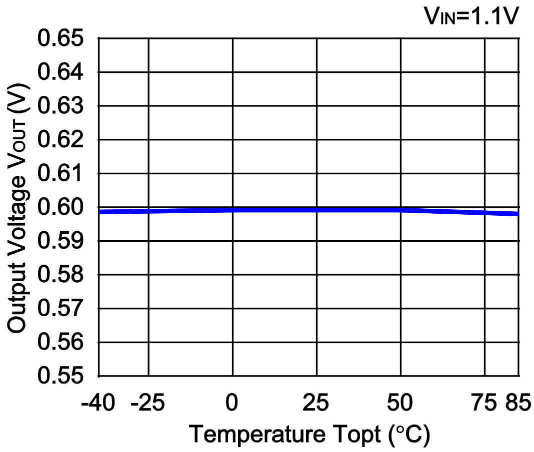
RP105x15xE/F



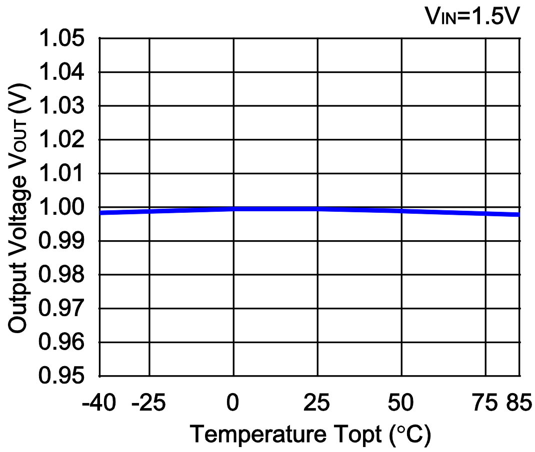
In RP105xxxxE/F, the current flows from V_{BIAS} pin to V_{IN} pin via the inside IC when the input voltage V_{IN} drops below the set output voltage V_{SET}.

4) Output Voltage vs. Temperature (C_{BIAS} = 1.0 μF, C_{IN} = C_{OUT} = 2.2 μF, I_{OUT} = 1 mA, V_{BIAS} = 3.6 V)

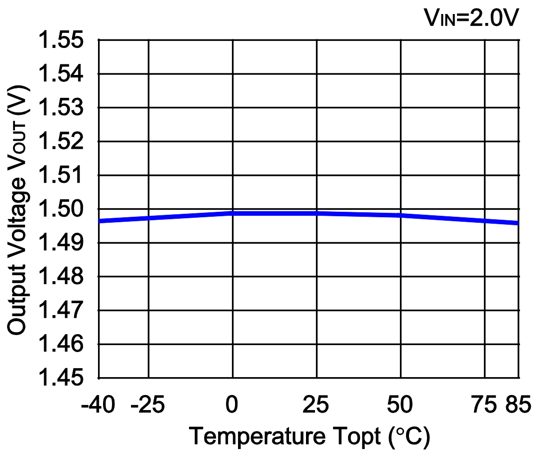
RP105x06xx



RP105x10xx

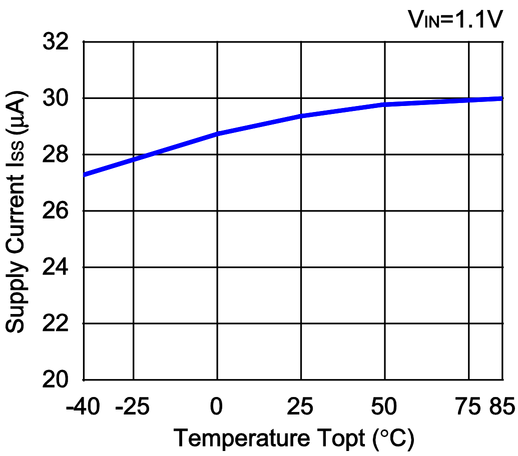


RP105x15xx

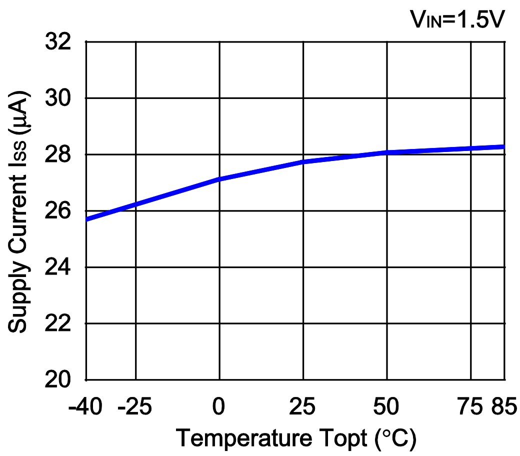


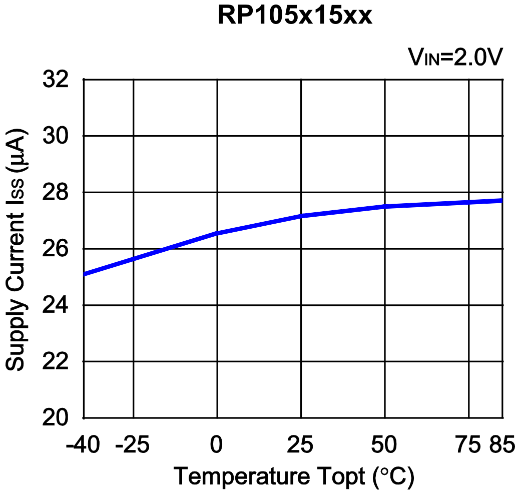
5) Supply Current vs. Temperature (C_{BIAS} = C_{IN} = C_{OUT} = none, V_{BIAS} = 3.6 V)

RP105x06xx

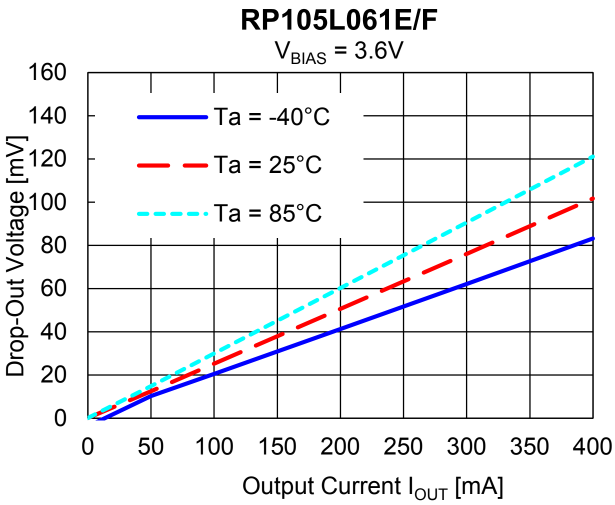


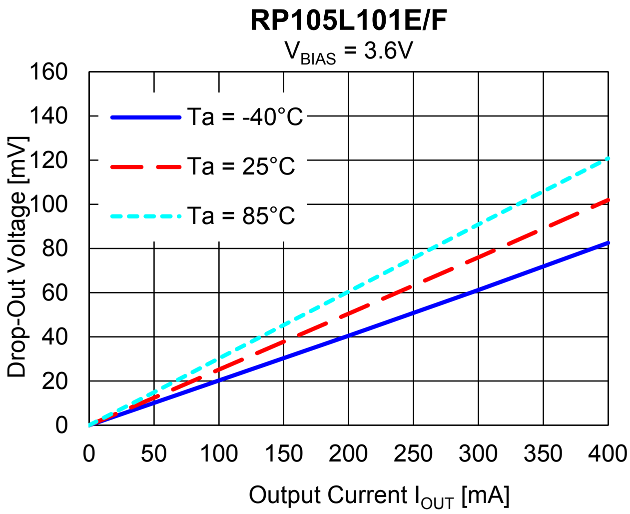
RP105x10xx

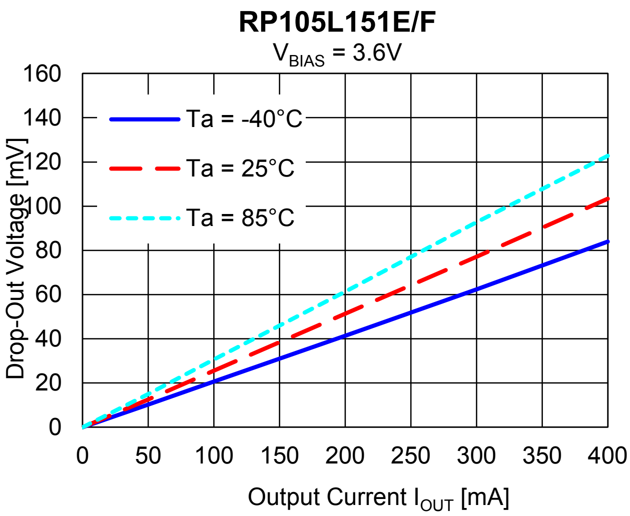




6) Dropout Voltage vs. Output Current (C_{BIAS} = 1.0 µF, C_{IN} = C_{OUT} = 2.2 µF)



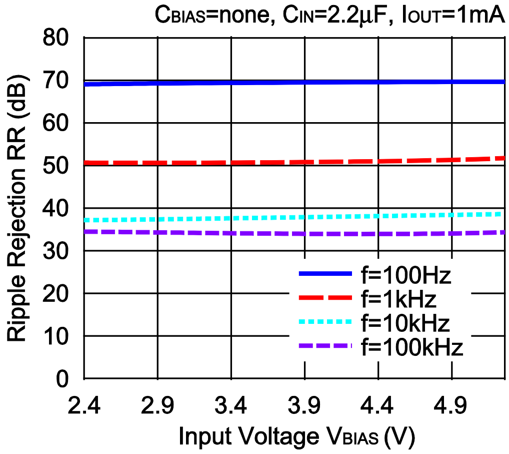




7) Ripple Rejection vs. Input Bias Voltage (C_{OUT} = 2.2 µF, Ripple = 0.2 Vp-p, Ta = 25°C)

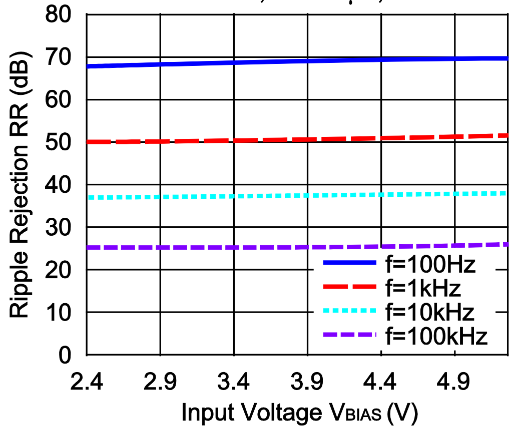
RP105x10xx

C_{BIAS}=none, C_{IN}=2.2µF, I_{OUT}=1mA



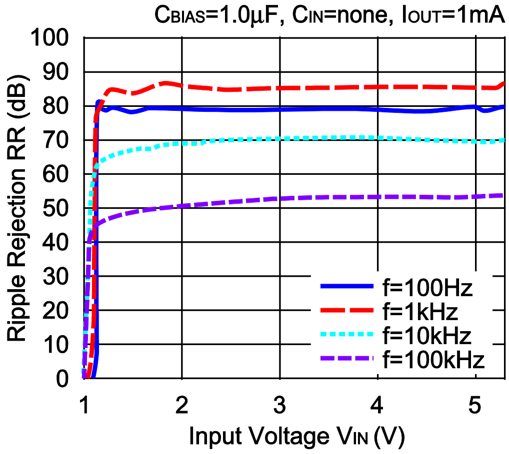
RP105x10xx

C_{BIAS}=none, C_{IN}=2.2µF, I_{OUT}=30mA



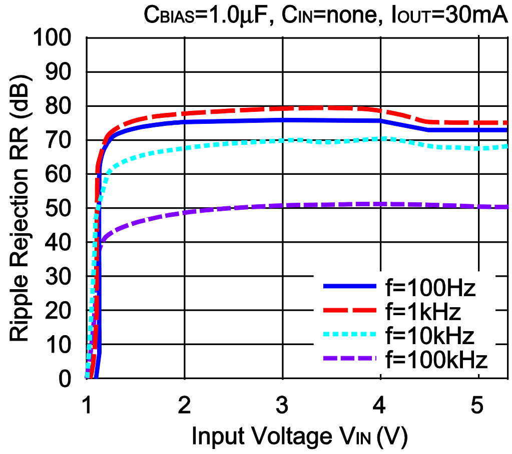
RP105x10xx

C_{BIAS}=1.0µF, C_{IN}=none, I_{OUT}=1mA



RP105x10xx

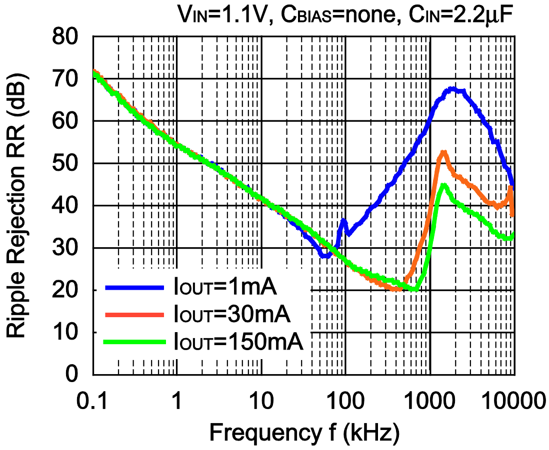
C_{BIAS}=1.0µF, C_{IN}=none, I_{OUT}=30mA



8) Ripple Rejection vs. Frequency (V_{BIAS} = 3.6 V, C_{OUT} = 2.2 µF, Ta = 25°C)

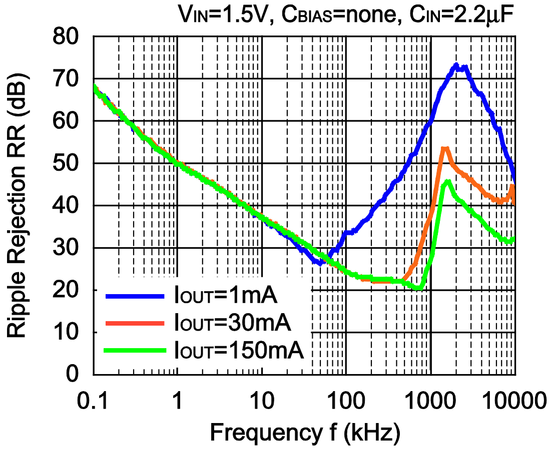
RP105x06xx

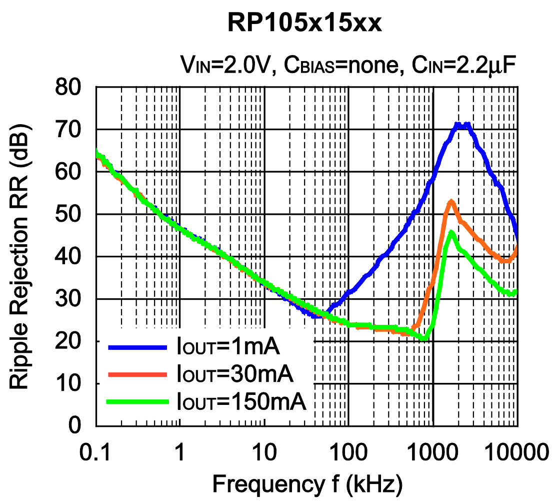
V_{IN}=1.1V, C_{BIAS}=none, C_{IN}=2.2µF

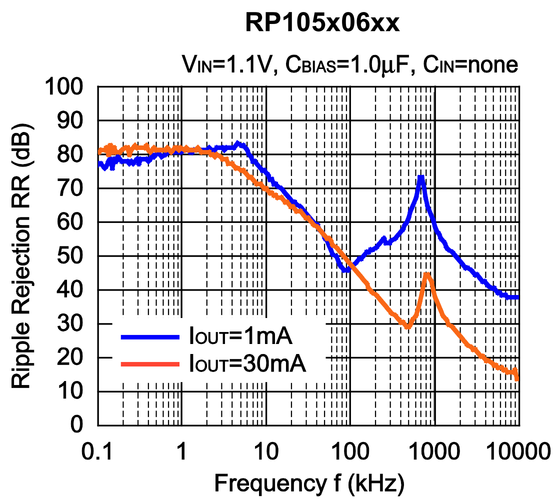


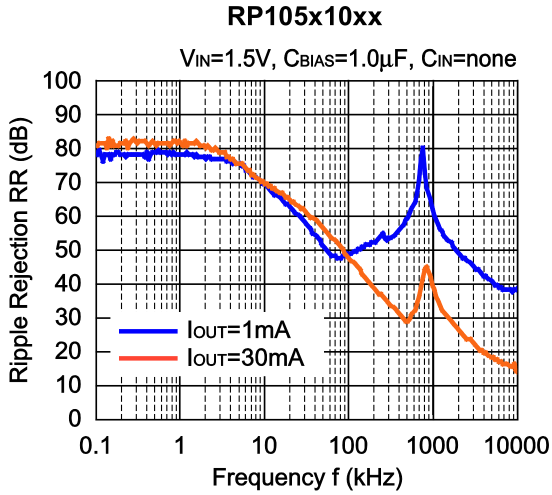
RP105x10xx

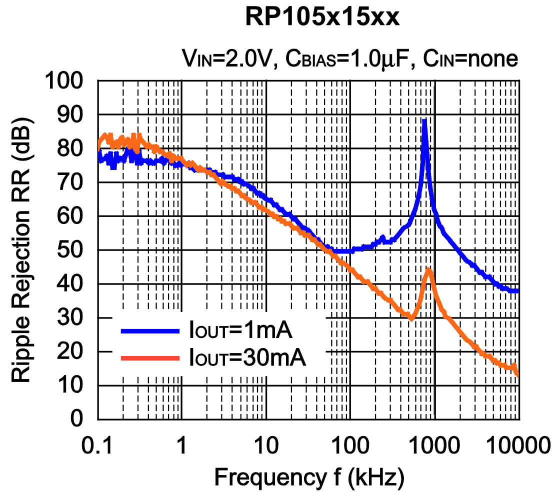
V_{IN}=1.5V, C_{BIAS}=none, C_{IN}=2.2µF



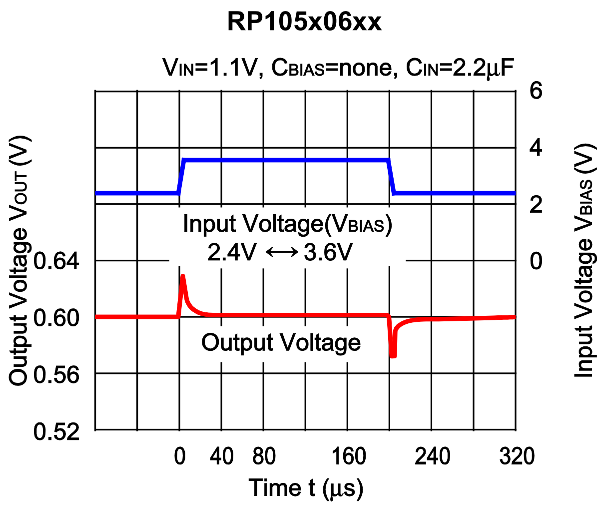


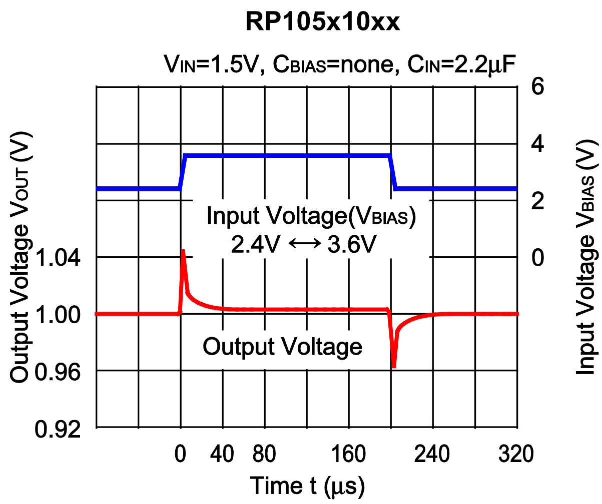






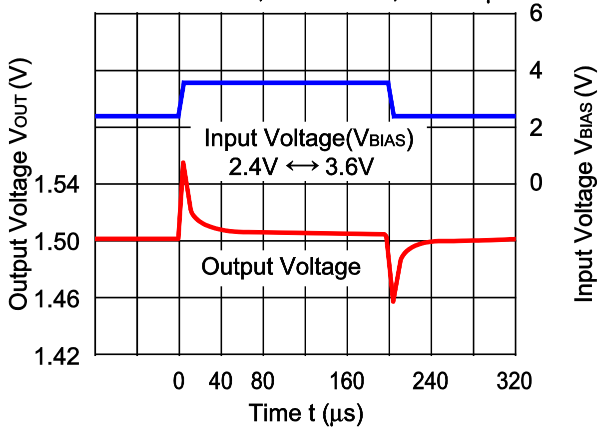
9) Input Transient Response (I_{OUT} = 30 mA, C_{OUT} = 1.0 µF, tr = tf = 5 µs, Ta = 25°C)





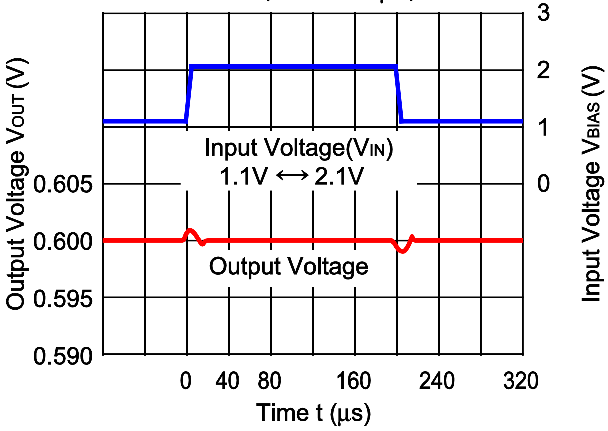
RP105x15xx

V_{IN}=2.0V, C_{BIAS}=none, C_{IN}=2.2μF



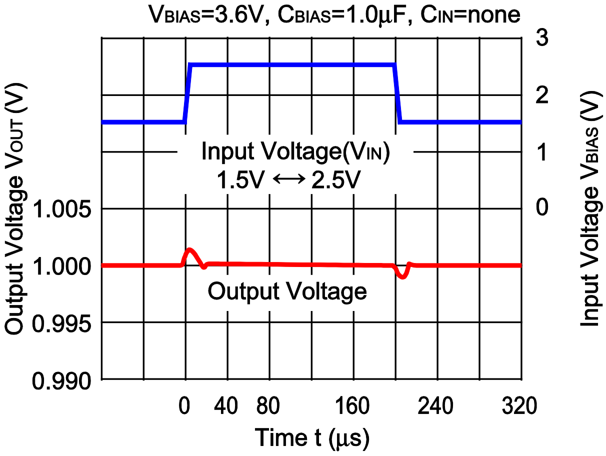
RP105x06xx

V_{BIAS}=3.6V, C_{BIAS}=1.0μF, C_{IN}=none



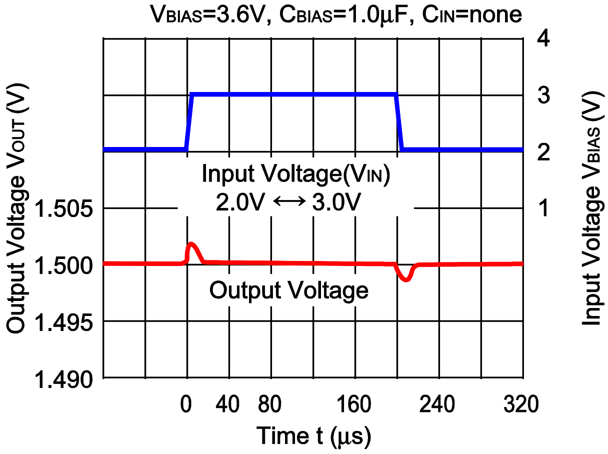
RP105x10xx

V_{BIAS}=3.6V, C_{BIAS}=1.0μF, C_{IN}=none



RP105x15xx

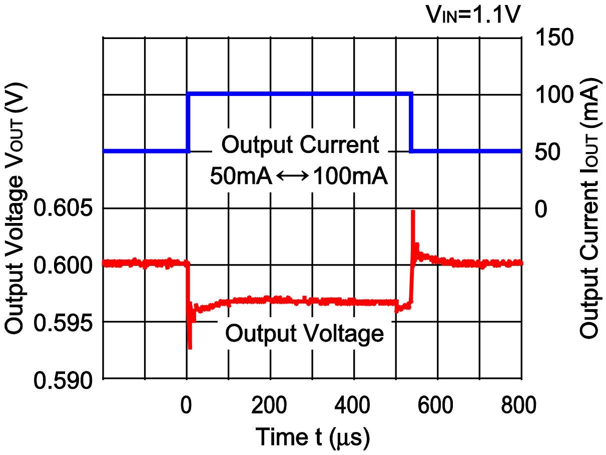
V_{BIAS}=3.6V, C_{BIAS}=1.0μF, C_{IN}=none



10) Load Transient Response (V_{BIAS} = 3.6 V, C_{BIAS} = 1.0 μF, C_{IN} = C_{OUT} = 2.2 μF, tr = tf = 0.5 μs, Ta = 25°C)

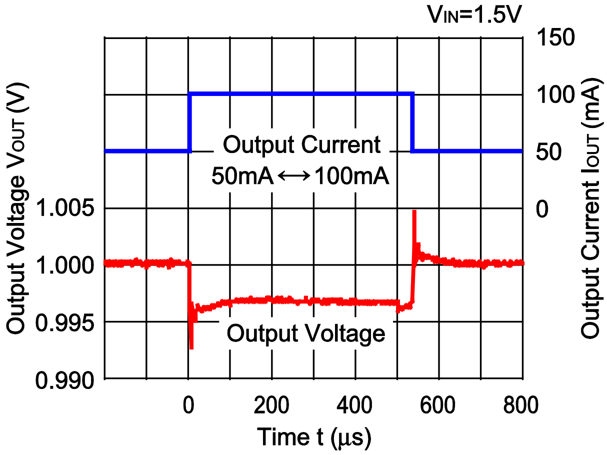
RP105x06xx

V_{IN}=1.1V

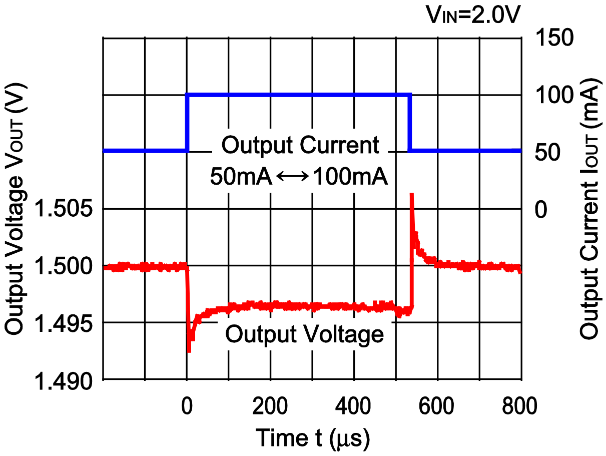


RP105x10xx

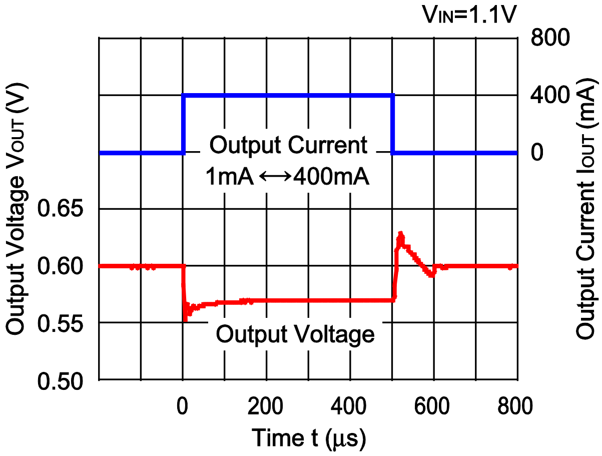
V_{IN}=1.5V



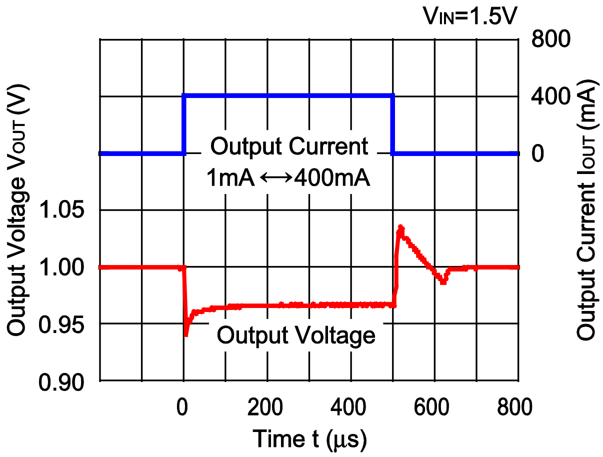
RP105x15xx



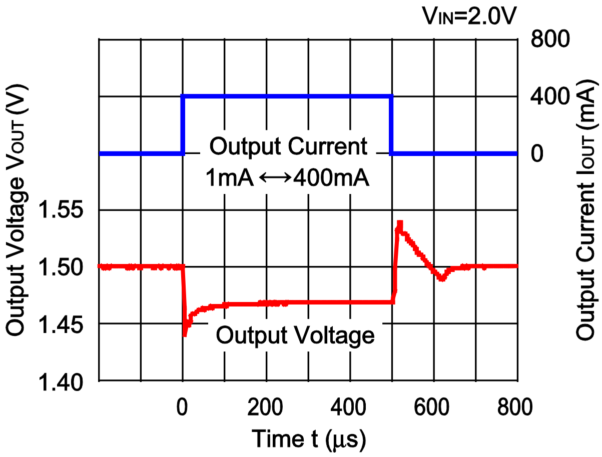
RP105x06xx



RP105x10xx

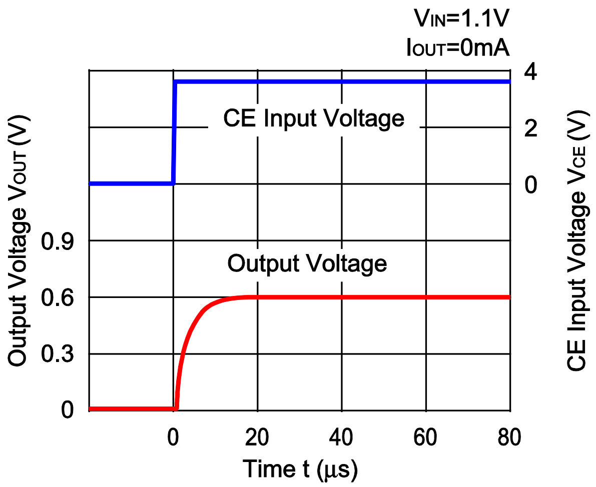


RP105x15xx

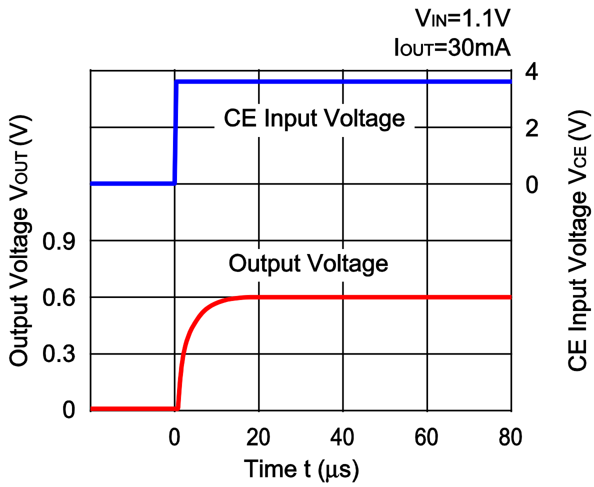


11) Turn On Speed with CE pin (V_{BIAS} = 3.6 V, C_{BIAS} = 1.0 µF, C_{IN} = C_{OUT} = 2.2 µF, Ta = 25°C)

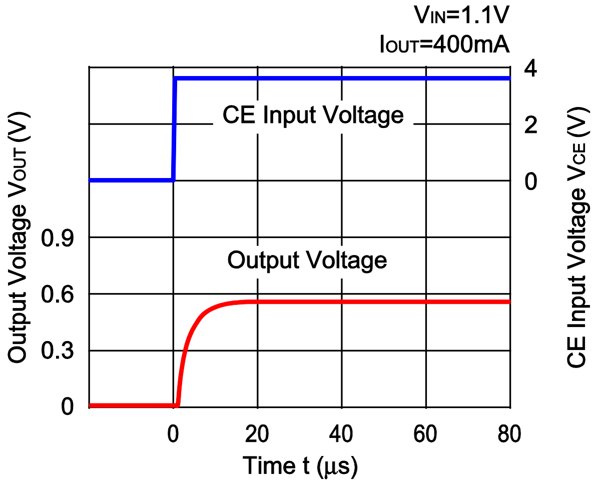
RP105x06xx



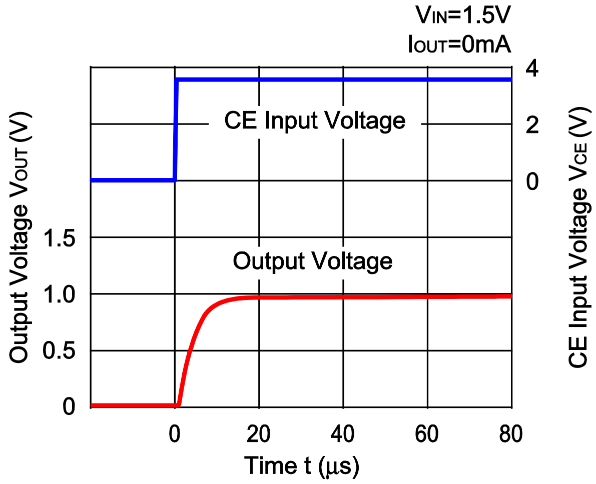
RP105x06xx



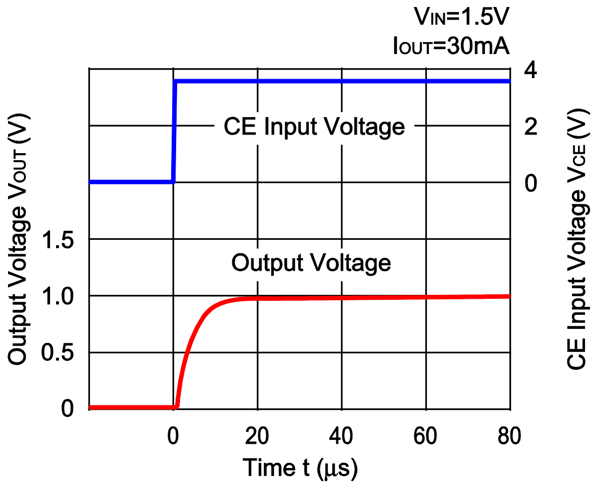
RP105x06xx



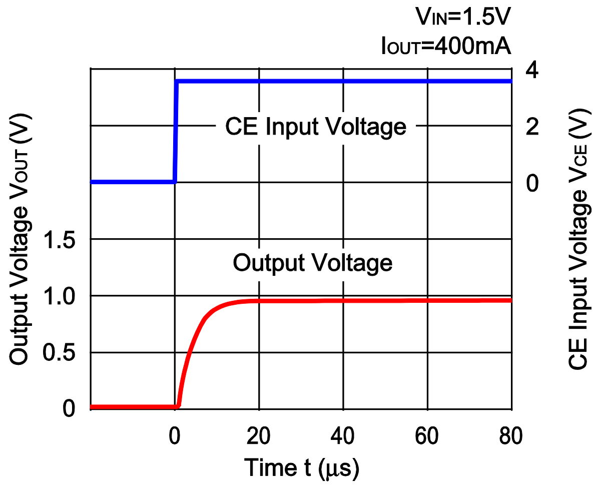
RP105x10xx



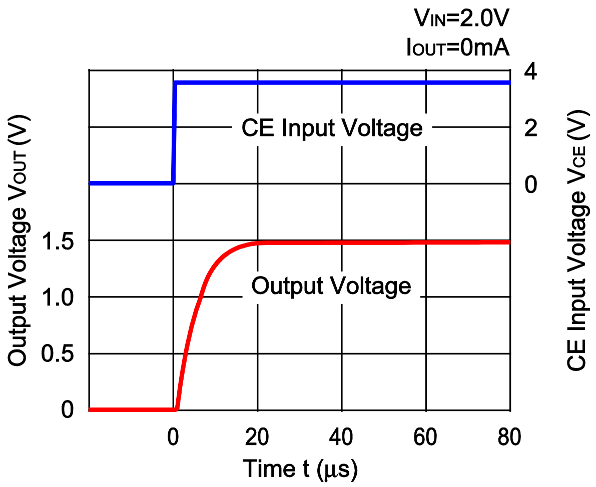
RP105x10xx



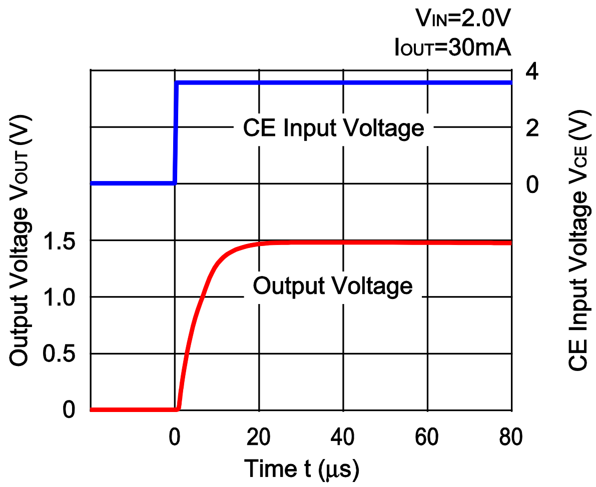
RP105x10xx



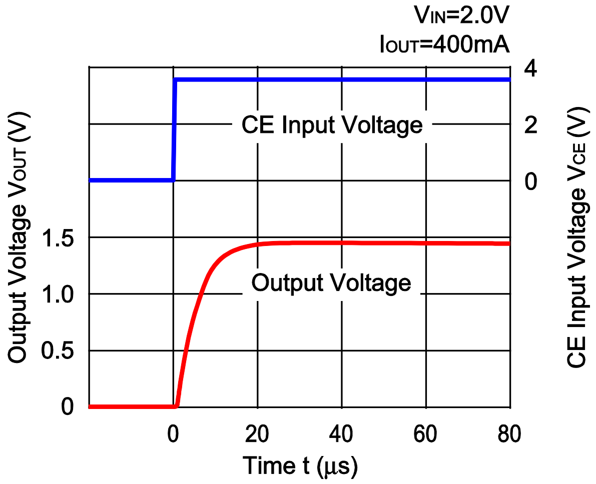
RP105x15xx



RP105x15xx

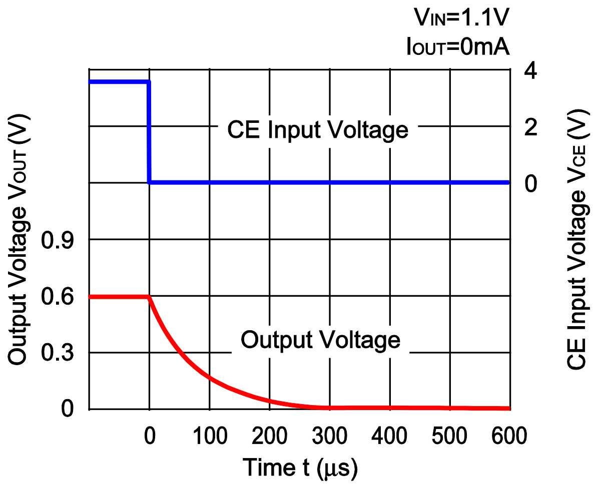


RP105x15xx

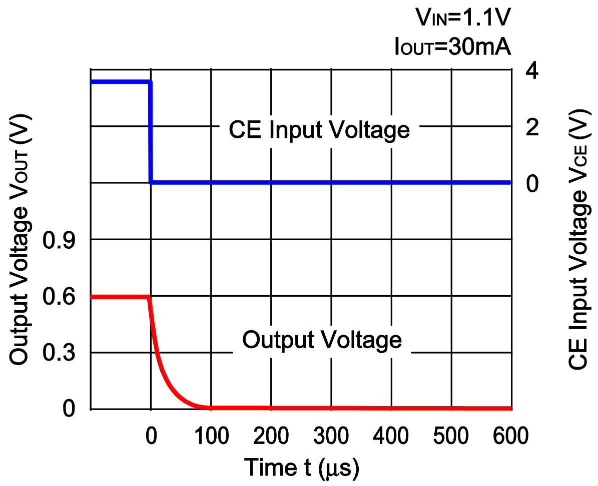


12) Turn Off Speed with CE Pin (V_{BIAS} = 3.6 V, C_{BIAS} = 1.0 μF, C_{IN} = C_{OUT} = 2.2 μF, Ta = 25°C)

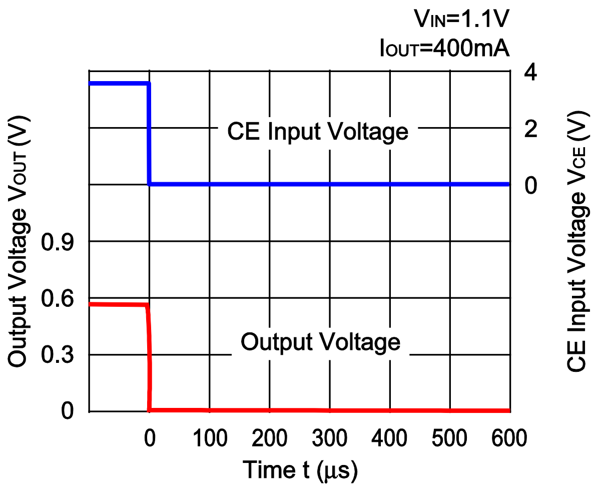
RP105x06xD/F



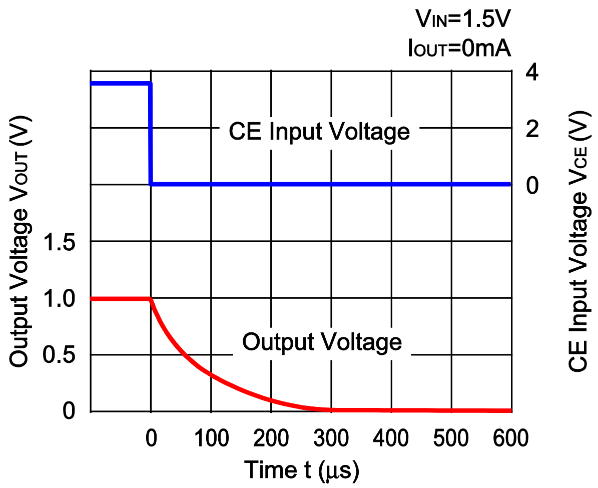
RP105x06xD/F

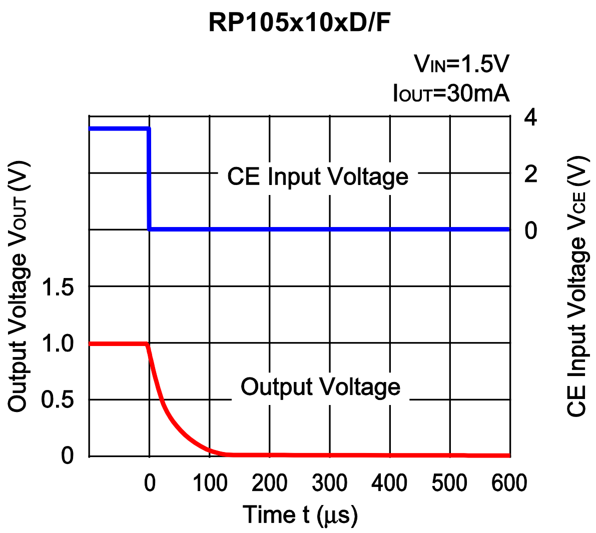


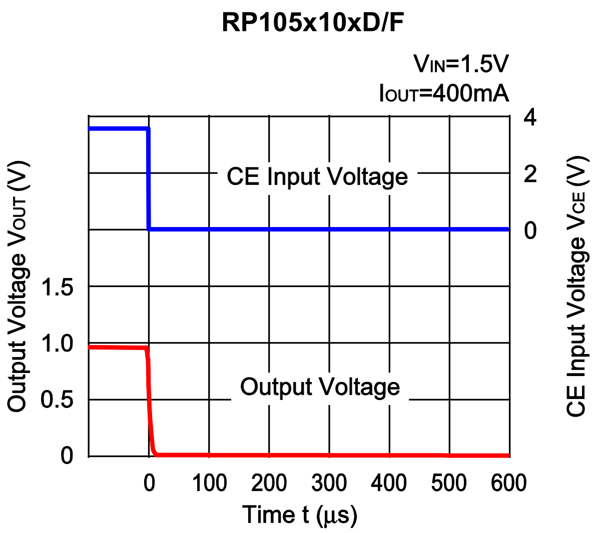
RP105x06xD/F

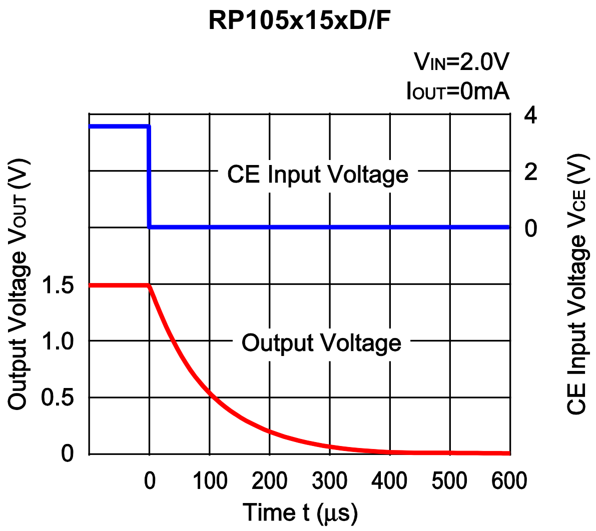


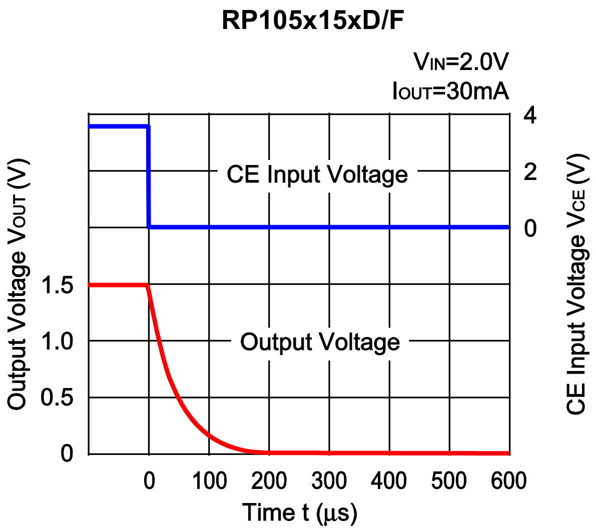
RP105x10xD/F

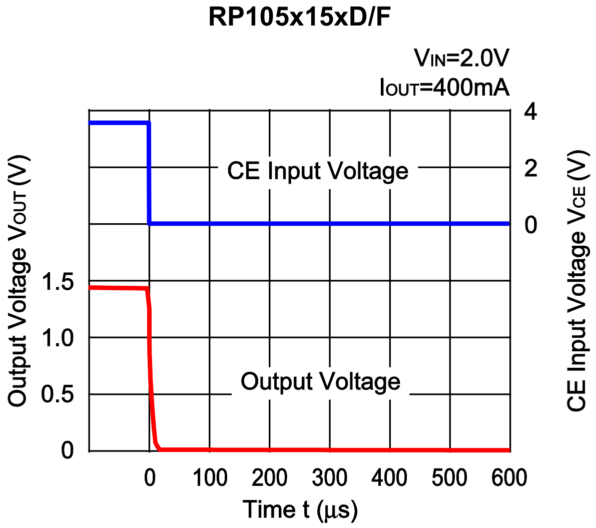



RP105x10xD/F
VIN=1.5V
IOUT=30mA
CE Input Voltage
Output Voltage
Output Voltage VOUT (V)
CE Input Voltage VCE (V)
Time t (µs)


RP105x10xD/F
VIN=1.5V
IOUT=400mA
CE Input Voltage
Output Voltage
Output Voltage VOUT (V)
CE Input Voltage VCE (V)
Time t (µs)

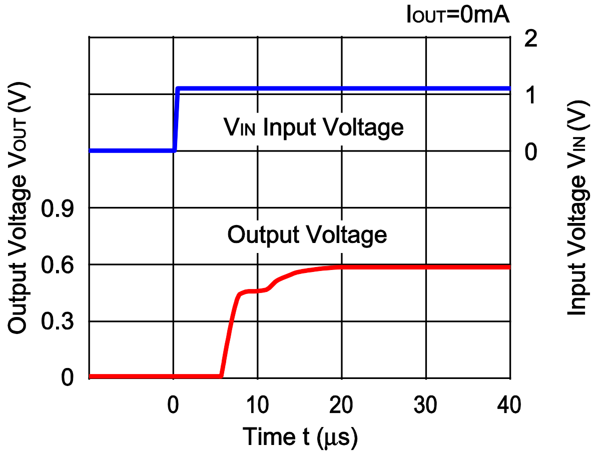

RP105x15xD/F
VIN=2.0V
IOUT=0mA
CE Input Voltage
Output Voltage
Output Voltage VOUT (V)
CE Input Voltage VCE (V)
Time t (µs)


RP105x15xD/F
VIN=2.0V
IOUT=30mA
CE Input Voltage
Output Voltage
Output Voltage VOUT (V)
CE Input Voltage VCE (V)
Time t (µs)

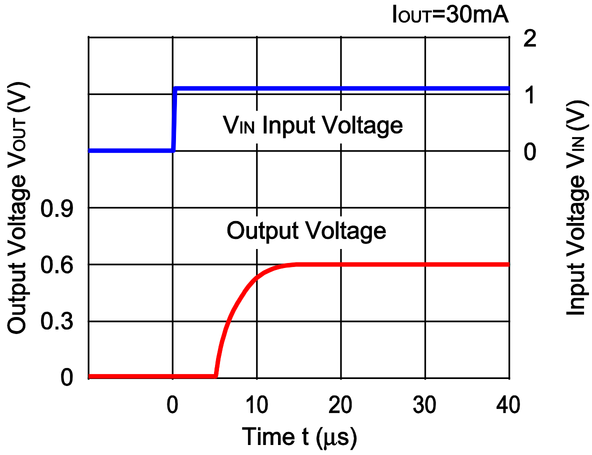

RP105x15xD/F
VIN=2.0V
IOUT=400mA
CE Input Voltage
Output Voltage
Output Voltage VOUT (V)
CE Input Voltage VCE (V)
Time t (µs)

13) Turn On Transient with V_{IN} pin (V_{BIAS} = 3.6 V, C_{BIAS} = 1.0 µF, C_{IN} = none, C_{OUT} = 2.2 µF, Ta = 25°C)

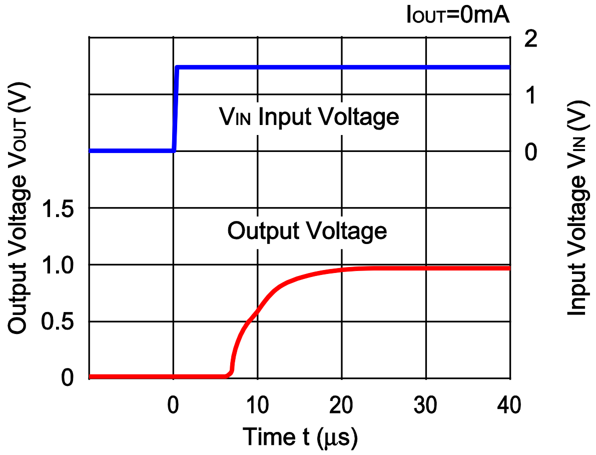
RP105x06xx



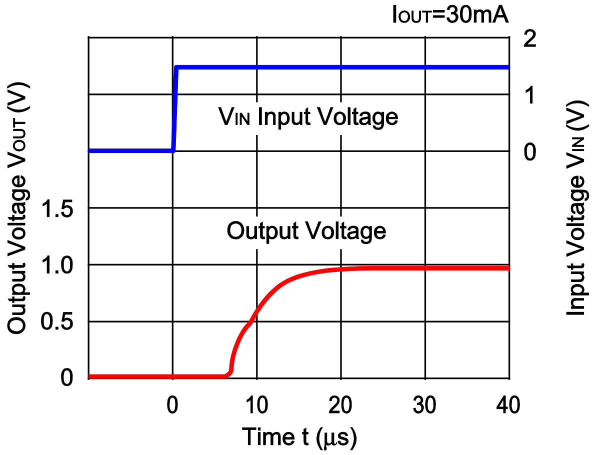
RP105x06xx



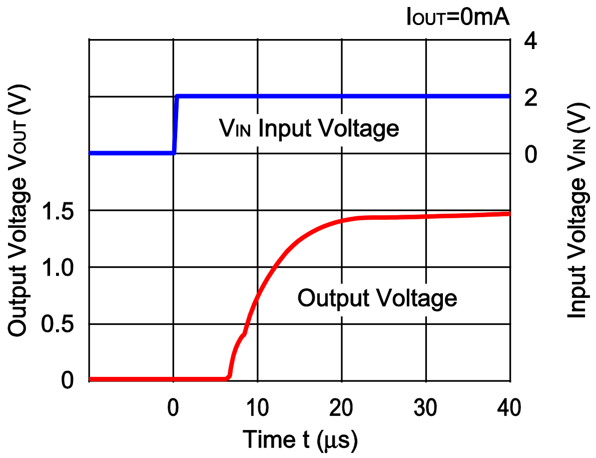
RP105x10xx



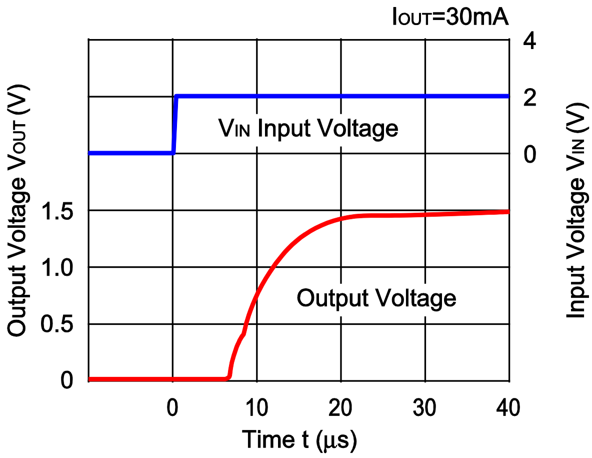
RP105x10xx



RP105x15xx



RP105x15xx



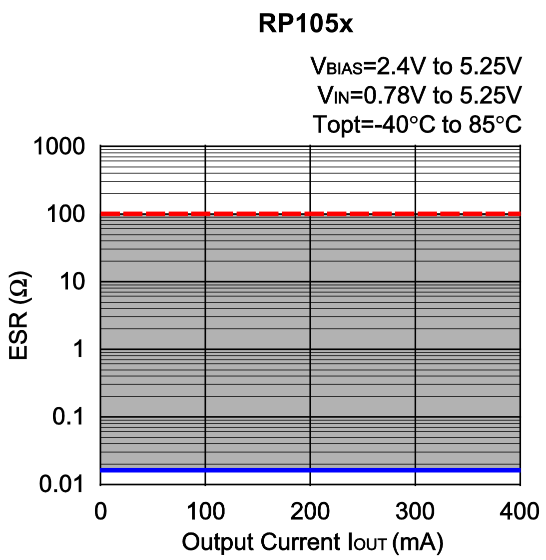
RICOH

ESR vs. Output Current

Ceramic type output capacitor is recommended for this series; however, the other output capacitors with low ESR also can be used. The relations between I_{OUT} (Output Current) and ESR of an output capacitor are shown below. The conditions when the white noise level is under 40 μV (Avg.) are marked as the hatched area in the graph.

Measurement conditions

Frequency Band	: 10 Hz to 2 MHz
Temperature	: –40°C to 85°C
Hatched Area	: Noise level is under 40 μV (Avg.)
C_{BIAS}, C_{IN}	: 1.0 μF
C_{OUT}	: 2.2 μF



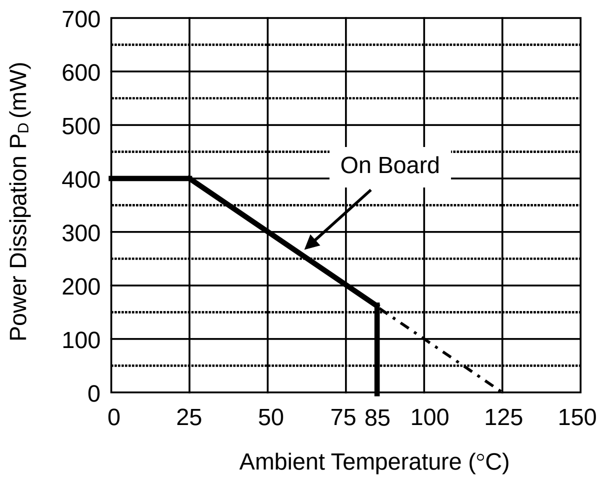
Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below.

Measurement Conditions

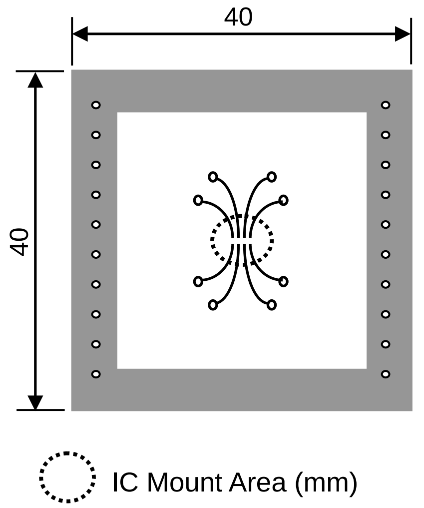
	Standard Test Land Pattern
Environment	Mounting on Board (Wind velocity = 0 m/s)
Board Material	Glass cloth epoxy plastic (Double-Sided Board)
Board Dimensions	40 mm x 40 mm x 1.6 mm
Copper Ratio	Top side: 50%, Back side: 50%
Through-holes	ϕ 0.54 mm x 28 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Standard Land Pattern
Power Dissipation	400 mW
Thermal Resistance	θja = (125 - 25°C) / 0.4 W= 250°C/W
	θjc = 67°C/W

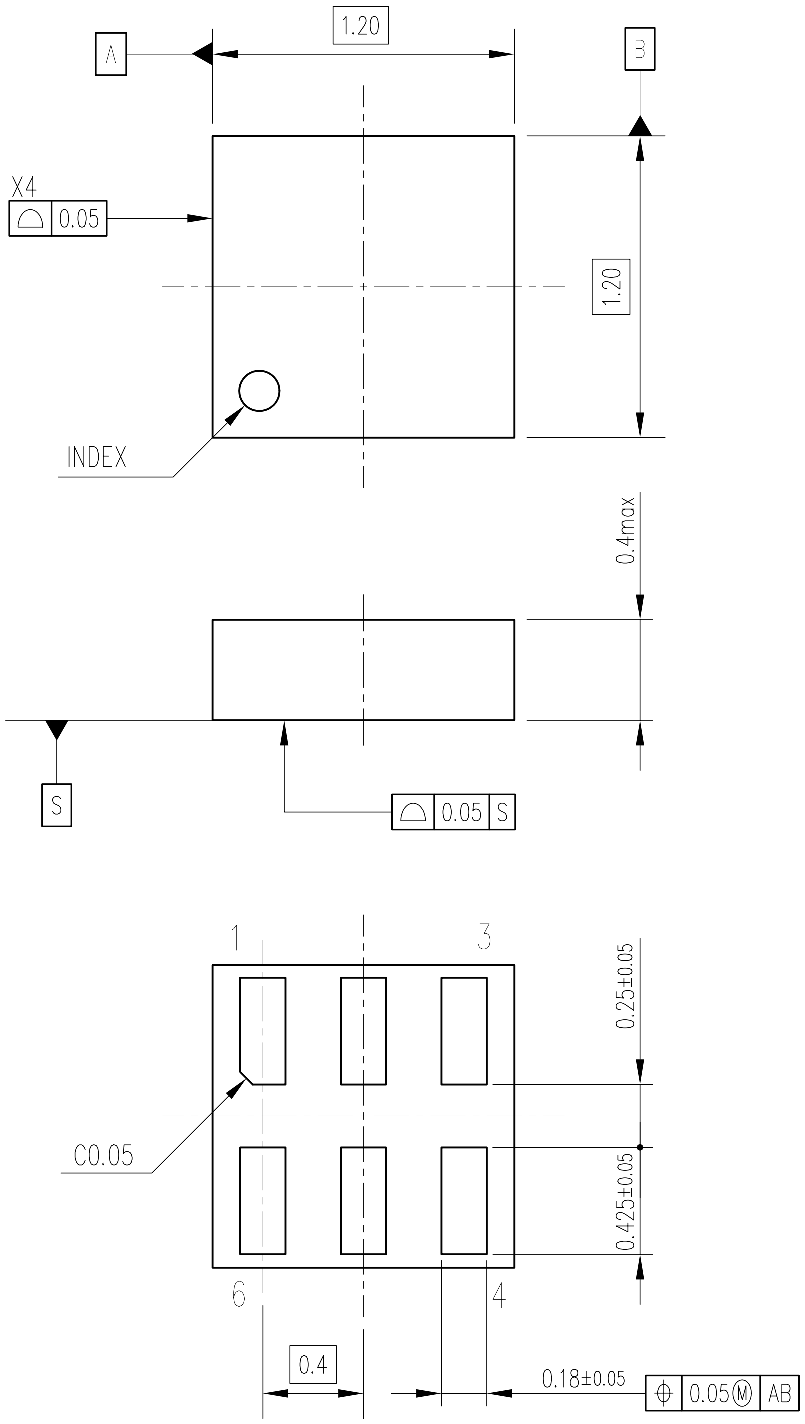


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

Ver. A



DFN(PLP)1212-6 Package Dimensions (Unit: mm)

Ver. A

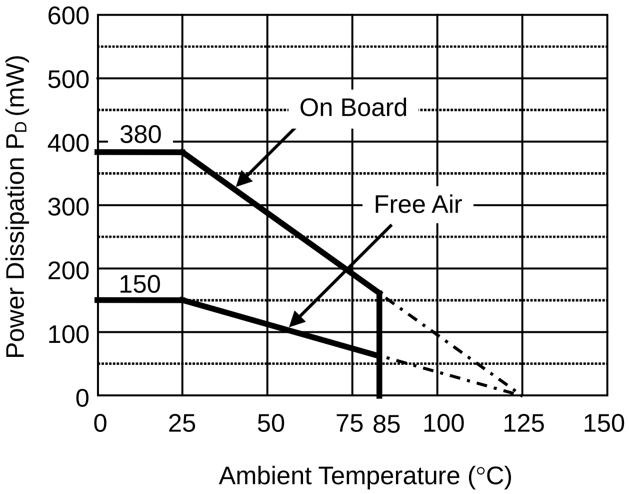
Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below.

Measurement Conditions

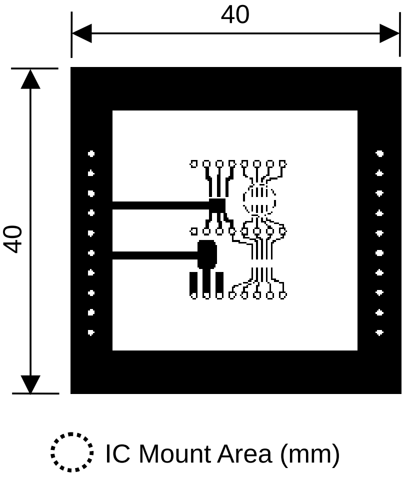
	Standard Test Land Pattern
Environment	Mounting on Board (Wind velocity = 0 m/s)
Board Material	Glass cloth epoxy plastic (Double-Sided Board)
Board Dimensions	40 mm x 40 mm x 1.6 mm
Copper Ratio	Top side: 50%, Back side: 50%
Through-holes	ϕ 0.5 mm x 44 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Standard Land Pattern	Free Air
Power Dissipation	380 mW	150 mW
Thermal Resistance	θja = (125 - 25°C) / 0.38 W = 263°C/W	θja = (125 - 25°C) / 0.15W = 667°C/W
	θjc = 75°C/W	-



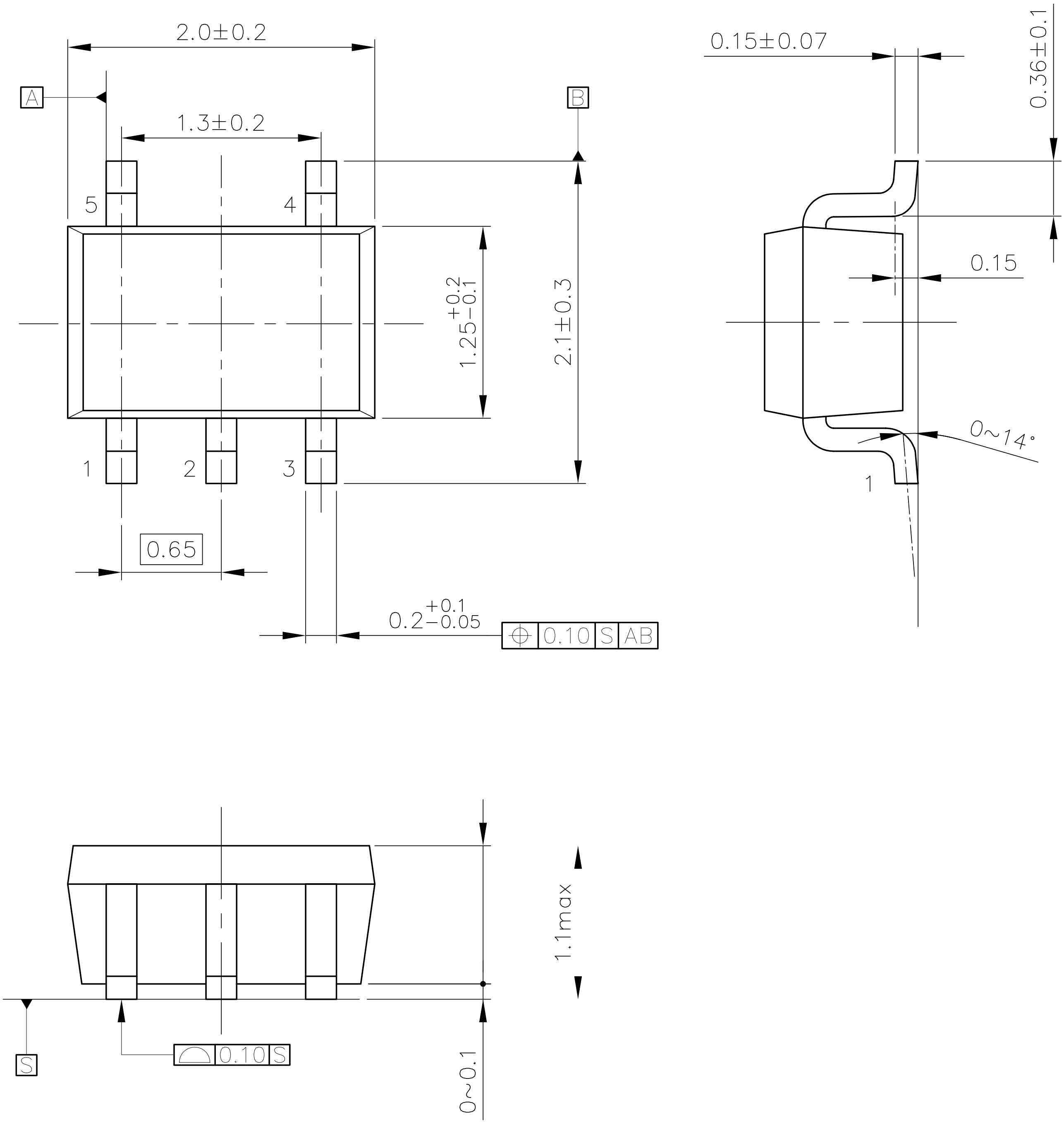
Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH

Ver. A



SC-88A Package Dimensions (Unit: mm)

Ver. A

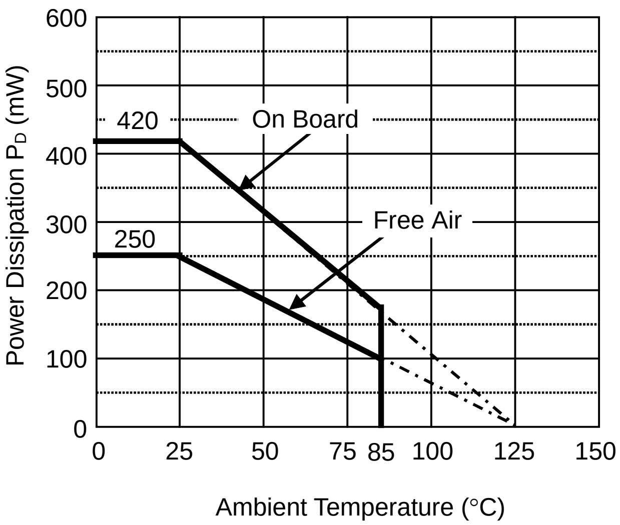
Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below (Power Dissipation (SOT-23-5) is substitution of SOT-23-6).

Measurement Conditions

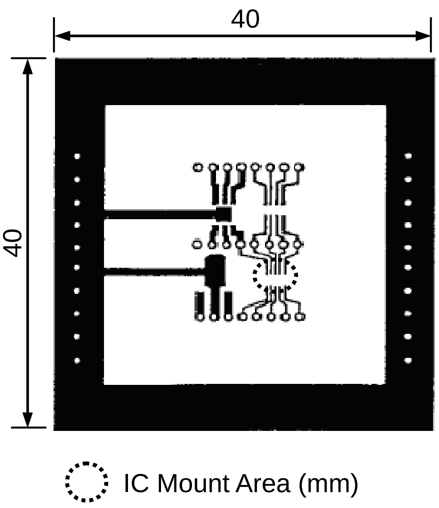
	Standard Test Land Pattern
Environment	Mounting on Board (Wind velocity = 0 m/s)
Board Material	Glass cloth epoxy plastic (Double-Sided Board)
Board Dimensions	40 mm x 40 mm x 1.6 mm
Copper Ratio	Top side: 50%, Back side: 50%
Through-holes	ϕ 0.5 mm x 44 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Standard Land Pattern	**Free Air**
Power Dissipation	420 mW	250 mW
Thermal Resistance	θja = (125 - 25°C) / 0.42 W= 238°C/W	400°C/W

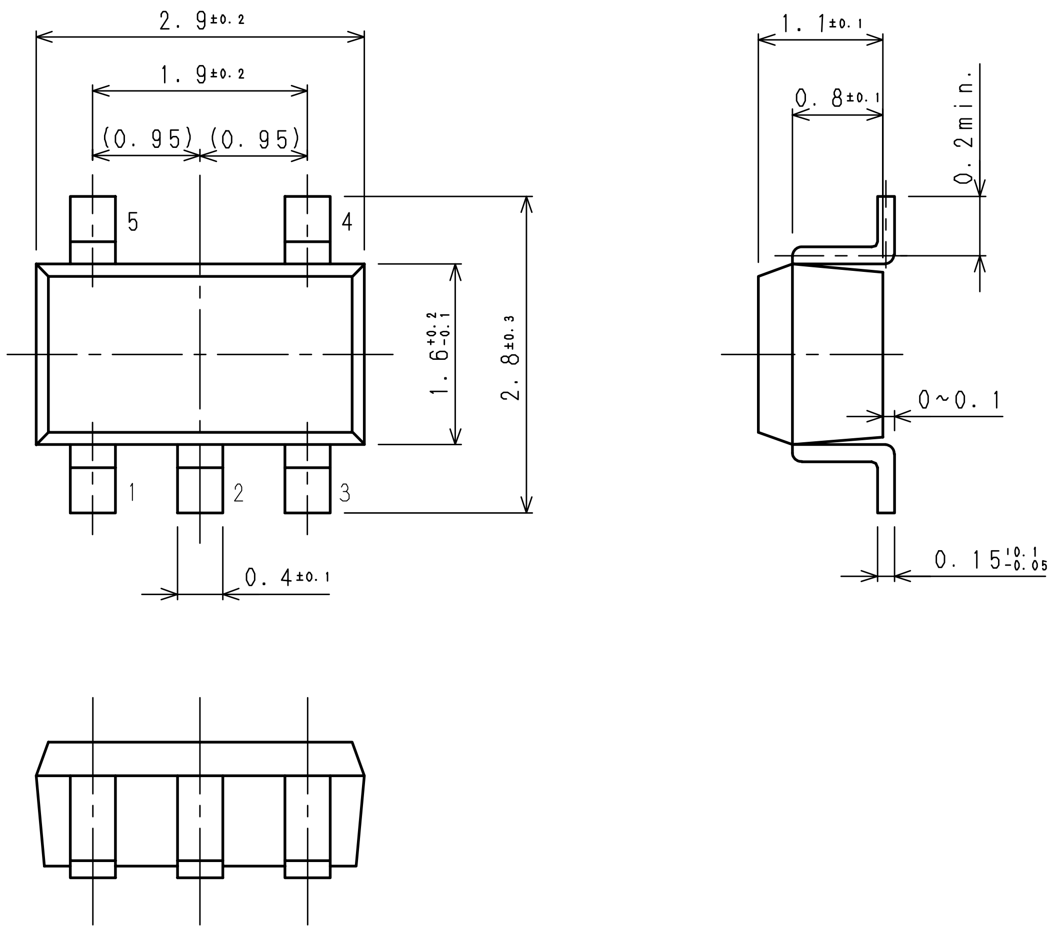


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

RICOH



SOT-23-5 Package Dimensions (Unit: mm)

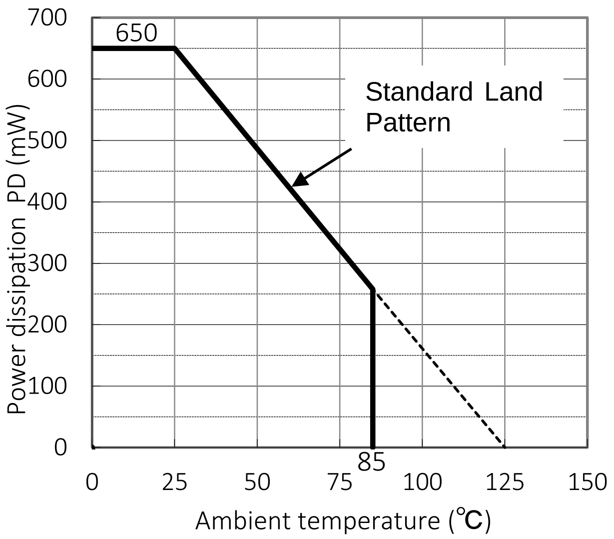
The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

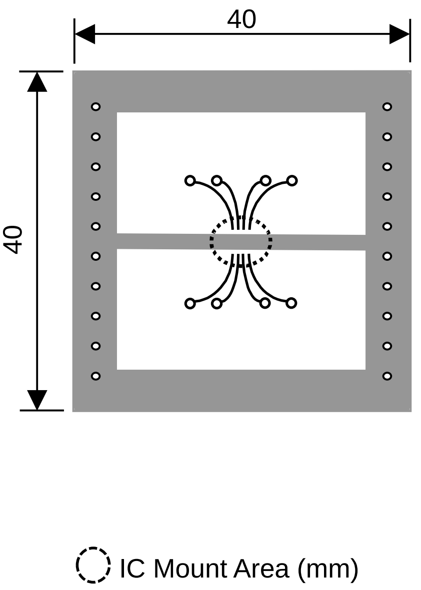
	Standard Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Two-Layer Boards)
Board Dimensions	40 mm x 40 mm x 1.6 mm
Copper Ratio	Font-side, Approx. 50% Back-side, Approx. 50%
Through-holes	ϕ 0.5 mm x 28 pcs

Measurement Result (Ta = 25°C, Tjmax = 125°C)

	Standard Land Pattern
Power Dissipation	650 mW
Thermal Resistance	θja = (125 − 25°C) / 0.65 W = 153°C/W θjc = 30°C/W

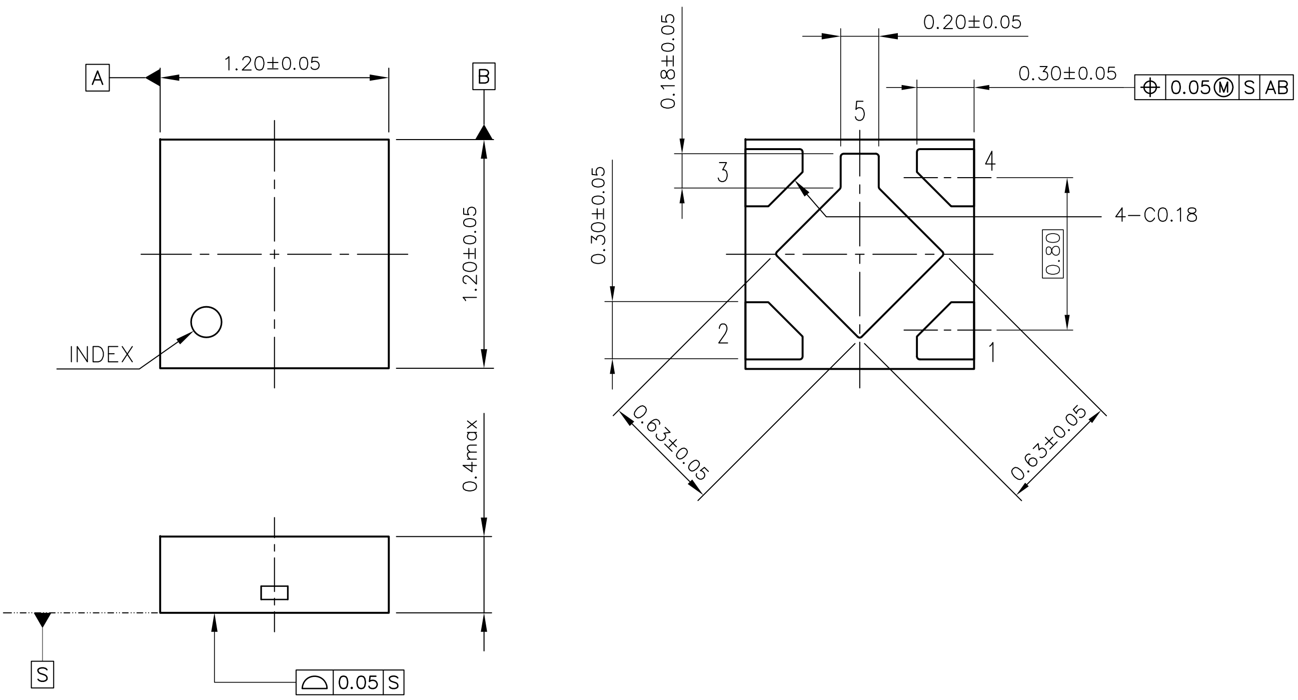


Power Dissipation vs. Ambient Temperature



Measurement Board Pattern

Ver. A



DFN1212-5 Package Dimensions (Unit: mm)

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