PICOR

Semiconductor Power Solutions

Cool-Power®

PI354x-00

36 Vin to 60 Vin Cool-Power ZVS Buck Regulator & LED Driver

Product Description

The PI354x-00 is a family of high input voltage, wide input range DC-DC ZVS-Buck regulators integrating controller, power switches, and support components all within a high density System-in-Package (SiP). The integration of a high-performance Zero-Voltage Switching (ZVS) topology, within the PI354x-00 series, increases point of load performance providing best in class power efficiency. The PI354x-00 requires only an external inductor, two voltage selection resistors and minimal capacitors to form a complete DC-DC switching mode buck regulator.

Device	Output Voltage		I_{OUT} Max
	Set	Range	
PI3542-00-LGIZ	2.5 V	2.2 V to 3.0 V	10 A
PI3543-00-LGIZ	3.3 V	2.6 V to 3.6 V	10 A
PI3545-00-LGIZ	5.0 V	4.0 V to 5.5 V	10 A
PI3546-00-LGIZ	12 V	6.5 V to 14 V	9 A

PI354x-00 Family can operate in constant voltage output for typical buck regulation applications in addition to constant current output for LED lighting and battery charging applications.

Features

- High Efficiency HV ZVS-Buck Topology
- Wide input voltage range of 36 V to 60 V
- Very fast transient response
- Constant voltage or constant current operation
- Constant current error amplifier and reference
- Power-up into pre-biased load
- Parallel capable with single wire current sharing
- Two phase interleaving
- Input Over/Undervoltage Lockout (OVLO/UVLO)
- Output Overvoltage Protection (OVP)
- Overtemperature Protection (OTP)
- Fast and slow current limits
- Differential amplifier for output remote sensing
- User adjustable soft-start & tracking
- -40°C to 125°C operating range (T_J)

Applications

- HV to PoL Buck Regulator Applications
- Computing, Communications, Industrial, Automotive Equipment
- Constant current output operation:
  - LED Lighting
  - Battery Charging

Package Information

- 10 mm x 10 mm x 2.6 mm LGA SiP

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Order Information

Cool-Power	Output Range		I_{OUT} Max	Package	Transport Media
	Set	Range			
PI3542-00-LGIZ	2.5 V	2.2 V to 3.0 V	10 A	10 mm x 10 mm LGA	TRAY
PI3543-00-LGIZ	3.3 V	2.6 V to 3.6 V	10 A	10 mm x 10 mm LGA	TRAY
PI3545-00-LGIZ	5.0 V	4.0 V to 5.5 V	10 A	10 mm x 10 mm LGA	TRAY
PI3546-00-LGIZ	12 V	6.5 V to 14 V	9 A	10 mm x 10 mm LGA	TRAY

Thermal, Storage, and Handling Information

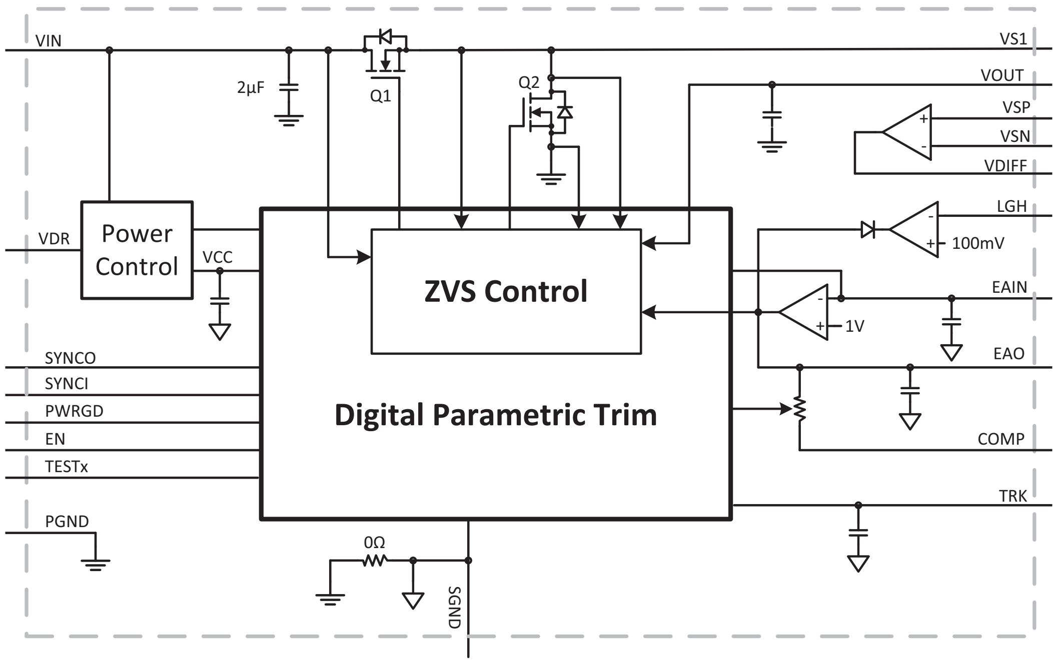
Name	Rating
Storage Temperature	-65°C to 150°C
Operating Junction Temperature	-40°C to 125°C
Soldering Temperature for 20 seconds	245°C
MSL Rating	3

Absolute Maximum Ratings

Name	Rating
V_{IN}	-0.7 V to 75 V
VS1	-0.7 to 75 V, -4 V for 5 ns
V_{OUT}	-0.5 V to 25 V
SGND	100 mA
TRK	-0.3 V to 5.5 V / 30 mA
VDR, SYNCI, SYNCO, PWRGD, EN, LGH, COMP, EAO, EAIN, VDIFF, VSN, VSP, TESTx	-0.3 V to 5.5 V / 5 mA

Notes: At 25°C ambient temperature. Stresses beyond these limits may cause permanent damage to the device. Operation at these conditions or conditions beyond those listed in the Electrical Specifications table is not guaranteed. All voltage nodes are referenced to PGND unless otherwise noted.

Functional Block Diagram

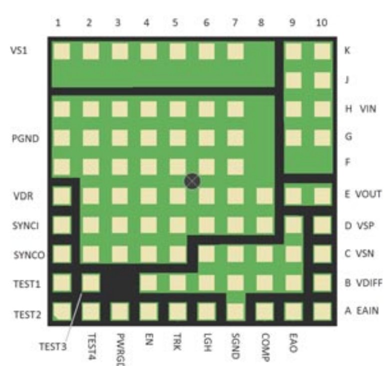


Simplified Block Diagram

Pin Description

Name	Location	I/O	Description
VS1	Block 2 (See Pkg Pin-Out dwg)	I/O	**Switching node:** and ZVS sense for power switches.
VIN	Block 1	I	**Input voltage:** and sense for UVLO, OVLO and feed forward ramp.
VDR	1E	I/O	**Gate Driver V_{CC} :** Internally generated 5.1 V. May be used as reference or low power bias supply for up to 2 mA. Must be impedance limited by the user.
SYNCI	1D	I	**Synchronization input:** Synchronize to the falling edge of external clock frequency. SYNCI is a high impedance digital input node and should always be connected to SGND when not in use.
SYNCO	1C	O	**Synchronization output:** Outputs a high signal for ½ of the minimum period for synchronization of other regulators.
TESTx	1B, 1A, 2B, 2A	I/O	**Test Connections:** Use only with factory guidance. Connect to SGND for proper operation.
PWRGD	3A	O	**Power Good:** High impedance when regulator is operating and V_{OUT} is in regulation. May also be used as "Parallel Good" – see applications section.
EN	4A	I	**Enable Input:** Regulator enable control. Asserted high or left floating – regulator enabled; asserted low, regulator output disabled.
TRK	5A	I	**Soft-start and track input:** An external capacitor may be connected between TRK pin and SGND to decrease the rate of rise during soft-start.
LGH	6A	I	**Lighting (LGH)/Constant Current (CC) Sense Input:** Input with a 100 mV threshold. Used for lighting and constant current type applications.When not using the constant current mode (CC mode), the LGH pin should be connected to SGND.
COMP	8A	O	**Compensation Capacitor:** Connect capacitor for control loop dominant pole.
EAO	9A	O	**Error amp output**: External connection for additional compensation and current sharing.
EAIN	10A	I	**Error Amp Inverting Input:** Connection for the feedback divider tap.
VDIFF	10B	O	**Independent Amplifier Output:** If unused connect in unity gain with VSP connected to SGND.
VSN	10C	I	**Independent Amplifier Inverting Input**
VSP	10D	I	**Independent Amplifier Non-Inverting Input**
VOUT	9E, 10E	I/O	**Output voltage:** and sense for power switches and feed-forward ramp.
SGND	Block 4	-	**Signal ground:** Internal logic ground for EA, TRK, SYNCI, SYNCO communication returns. SGND and PGND are star connected within the regulator package.
PGND	Block 3	-	**Power ground:** V_{IN} and V_{OUT} power returns.

Package Pin-Out



85 Pad LGA Sip (10 mm x 10mm)
(Top through view)

Block 1: V_{IN}; K9-10, J9-10, H9-10, G9-10

Block 2: VS1; K1-7

Block 3: PGND; H1-7, G1-7,F1-7, E2-8, D2-8, C2-5

Block 4: SGND; D9, C6-9, B4-9, A7

PI354x-00 Common Electrical Characteristics

Specifications apply for -40°C <T_J < 125°C, V_{IN} = 48 V, EN = High, V_{VDR} = 5.1 V +/- 2%, L1 = 340 nH [1] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential Amp						
Open Loop Gain			96	120	140	dB
Small Signal Gain-bandwidth			5	7	12	MHz
Offset			-1	0.5	1	mV
Common Mode Input Range			-0.1		2.5	V
Differential Mode Input Range					2	V
Input Bias Current			-1		1	µA
Maximum V_{OUT}		I_{DIFF} = -1 mA	V_{VDR} -0.2			V
Minimum V_{OUT}					20	mV
Capacitive Load Range for Stability			0		50	pF
Slew Rate Rising				11		V/µsec
Slew Rate Falling				11		V/µsec
Sink/Source Current			-1		1	mA
Current Source Function (LGH)						
Reference			95	100	105	mV
Input Offset				0.5		mV
Gain-Bandwidth Product			3			MHz
Internal Feedback Capacitance				20		pF
Gain Amp						
Gain				10		V/V
Intermediate Reference				1		V
Gain-Bandwidth Product			3			MHz
Transconductance				1		mS
Output Current Capability		Sink current only	1			mA
PGD						
PGD Rising Threshold	$V_{PG\_HI\%}$	[2]	79	85	91	% V_{OUT_DC}
PGD Falling Threshold	$V_{PG\_LO\%}$	[2]	77	83	89	% V_{OUT_DC}
PGD Output Low	V_{PG_SAT}	Sink = 4 mA [2]			0.4	V
PGD Sink Current	I_{PG_SAT}	[2]		4		mA

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

PI3542-00 (2.5 V_{OUT}) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, V_{IN} = 48 V, V_{VDR} = 5.1 V +/- 2%, L1 = 340 nH [1] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		36	48	60	V
Input Current	I_{IN_DC}	V_{IN} = 48 V, T_C = 25°C, I_{OUT} = 10 A		0.597		A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	Short at terminals		3.1	-	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		1.27		mA
		Enabled (no load)		2.42		
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
EAIN Voltage Total Regulation	V_{OUT_DC}	[2]	0.985	1.00	1.015	V
Output Voltage Trim Range	V_{OUT_DC}	[2][3]	2.2	2.5	3.0	V
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$	@ 25°C, 36 V < V_{IN} < 60 V		0.10		%
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$	@ 25°C, 0.5 A < I_{OUT} < 10 A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 10 A, C_{OUT} = 6 x 100 µF, 20 MHz BW [4]		47		mVp-p
Output Current	I_{OUT_DC}	[5]	0		10	A
Current Limit	I_{OUT_CL}	L1 = 340 nH ±1%	-	12	-	A
Protection						
Input UVLO Start Threshold	V_{UVLO_START}		33.8	34.8	35.8	V
Input UVLO Stop Hysteresis	V_{UVLO_HYS}			0.9		V
Input UVLO Response Time				1.25		usec
Input OVLO Stop Threshold	V_{OVLO}		62	64.3	66.2	V
Input OVLO Start Hysteresis	V_{OVLO_HYS}			1.3		V
Input OVLO Response Time	t_f			1.25		usec
Output Overvoltage Protection	V_{OVP}	Above set V_{OUT}		20		%
Overtemperature Fault Threshold	T_{OTP}			130		°C
Ovetemperature Restart Hysteresis	T_{OTP_HYS}			30		°C
Timing						
Switching Frequency	f_S	[6] 48 V_{IN} to 2.5 V_{OUT}, 3 A out, L1 = 30 nH ±1%	-	400	-	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [3]	50		110	%
SYNCI Threshold	V_{SYNCI}			$V_{VDR}/2$		V

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

PI3542-00 (2.5 V_{OUT}) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, V_{IN} = 48 V, V_{VDR} = 5.1 V +/- 2%, L1 = 340 nH [1] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1 mA	V_{VDR}–0.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1 mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20 pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20 pF load		10		ns
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.08	V
TRK Enable Threshold	V_{TRK_OV}		20	40	60	mV
TRK to EAIN Offset	V_{EIAN_OV}		50	80	110	mV
Charge Current (Soft – Start)	I_{TRK}		-70	-50	-30	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5 V		10		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0	0.6	.94	1.6	mS
Error Amplifier Trans-Conductance	GMeao	[2]		5.1		ms
PSM Skip Threshold	PSM_{SKIP}	[2]		0.8		V
Error Amplifier Output Impedance	R_{OUT}	[2]	1			MOhm
Internal Compensation Capacitor	Chf	[2]		56		pf
Internal Compensation Resistor	Rzi	[2]		5k		Ohm
Enable						
High Threshold	V_{EN_HI}		0.9	1	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Enable Pull-Up Voltage (floating, no faulted)	V_{EN_PU}			2		V
Enable Pull-Down Voltage (floating, fault)	V_{EN_PD}			0		V
Source Current	I_{EN_SO}			-50		µA
Sink Current	I_{EN_SK}			50		µA

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

PI3542-00 (2.5 V_{OUT}) Electrical Characteristics

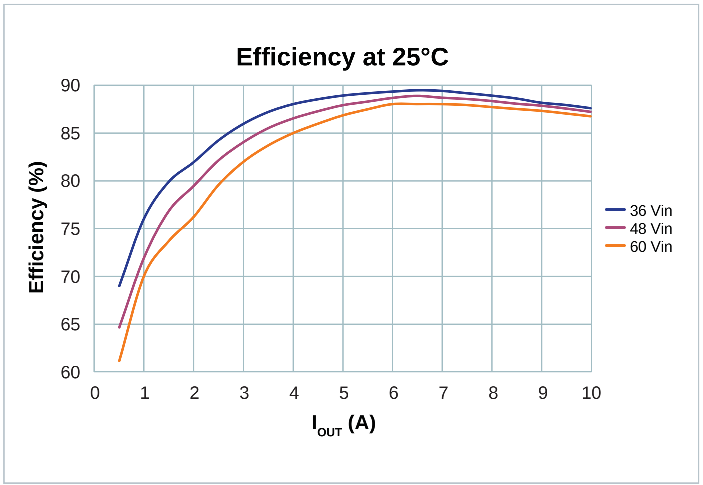


Figure 1 — Regulator Efficiency

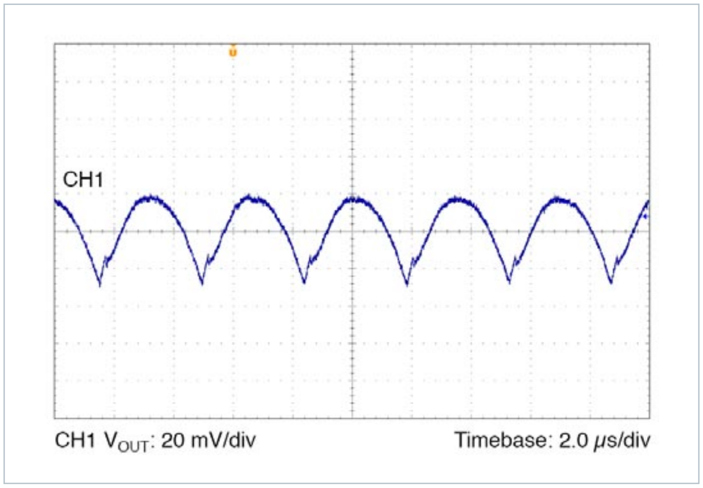


Figure 4 — Output Ripple: 48 V_{IN}, 2.5 V_{OUT} at 10 A. V_{OUT} = 20 mV/Div, 2.0 µs/Div; C_{OUT} = 6 x 100 µF Ceramic

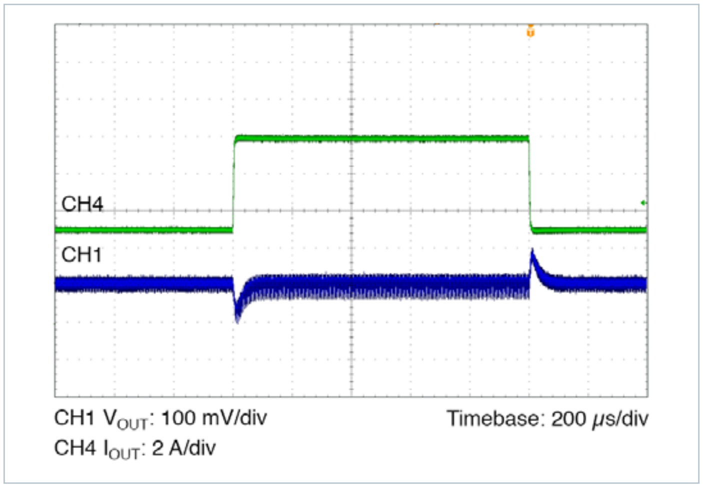


Figure 2 — Transient Response: 5 A to 10 A, at 1 A/µs. 48 V_{IN} to 2.5 V_{OUT}, C_{OUT} = 6 x 100 µF Ceramic

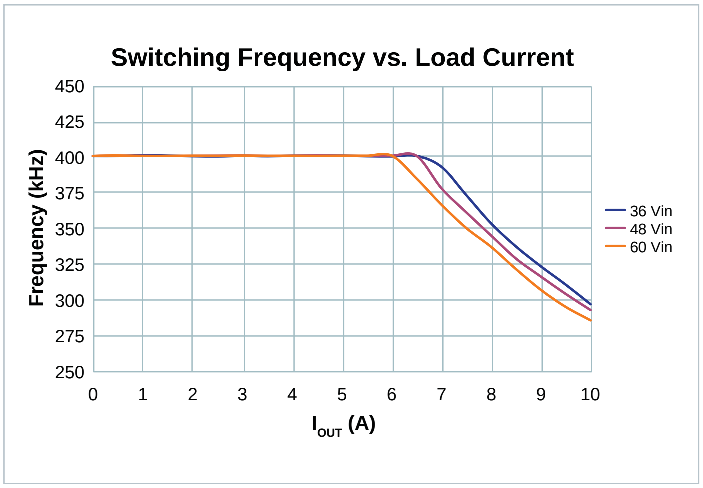


Figure 5 — Switching Frequency vs. Load Current

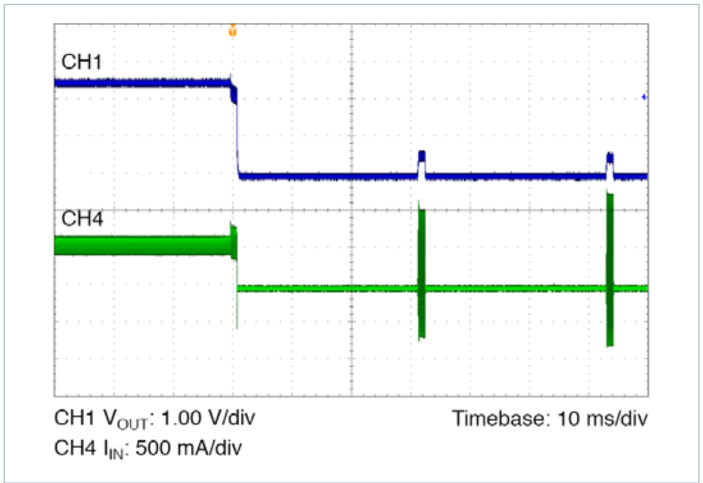


Figure 3 — Output Short Circuit @ V_{IN} = 48 V

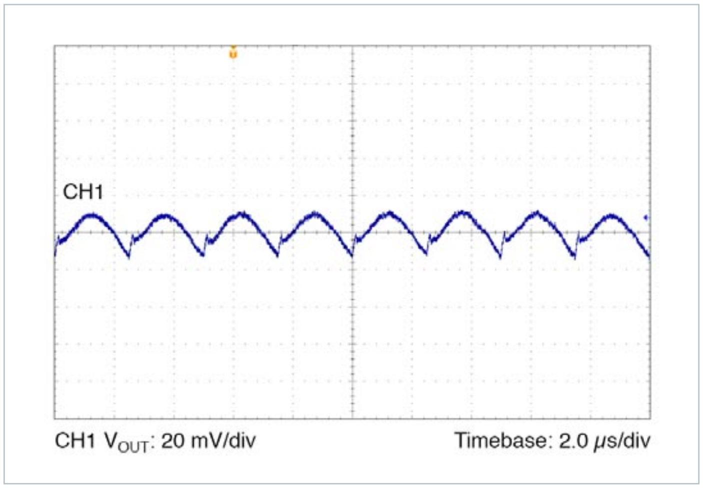


Figure 6 — Output Ripple: 48 V_{IN}, 2.5 V_{OUT} at 5 A. V_{OUT} = 20 mV/Div, 2.0 µs/Div; C_{OUT} = 6 x 100 µF Ceramic

PI3542-00 (2.5 V_{OUT}) Electrical Characteristics

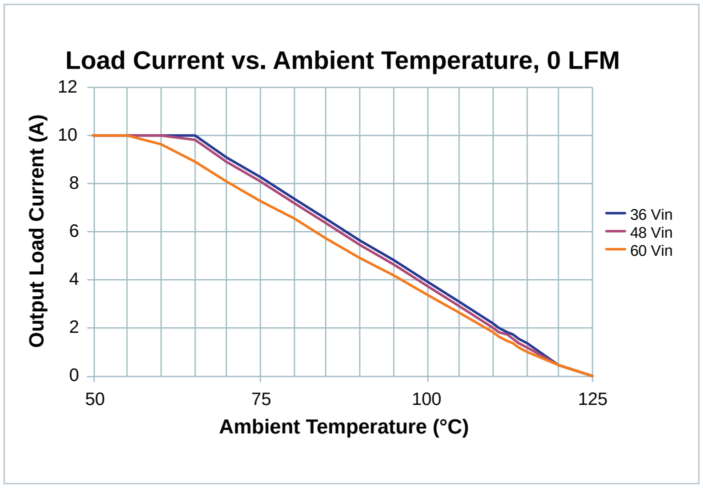


Figure 7 — Load Current vs. Ambient Temperature, 0 LFM

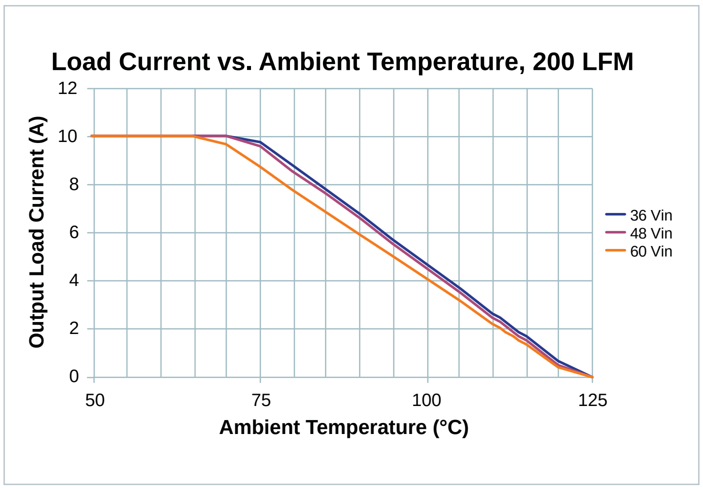


Figure 8 — Load Current vs. Ambient Temperature, 200 LFM

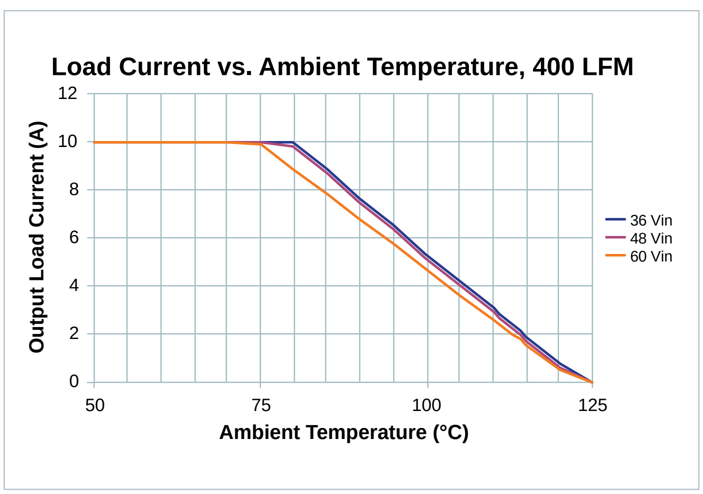


Figure 9 — Load Current vs. Ambient Temperature, 400 LFM

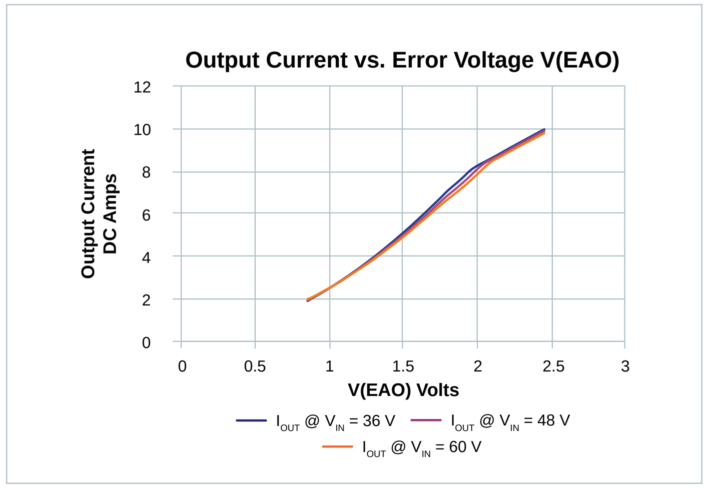


Figure 10 — Output Current vs. Error Voltage V(EAO)

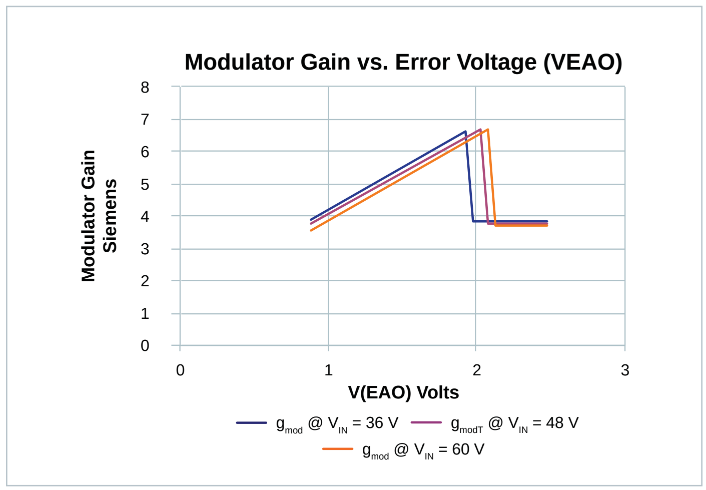


Figure 11 — Modulator Gain vs. Error Voltage (VEAO)

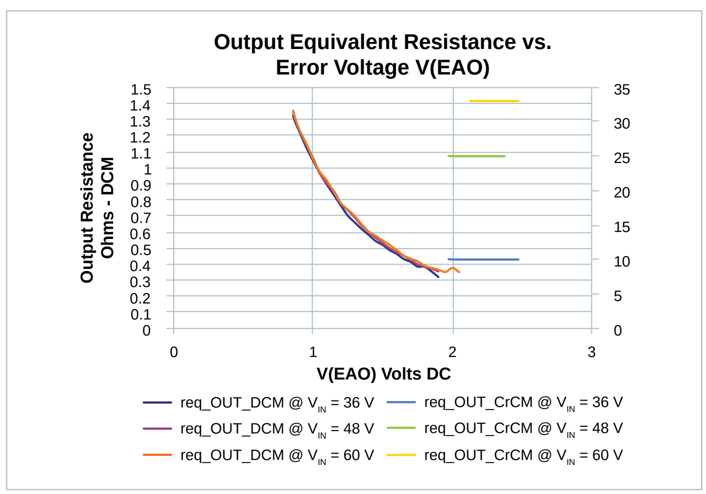


Figure 12 — Output Equivalent Resistance vs.Error Voltage V(EAO)

PI3543-00 (3.3 V_{OUT}) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, V_{IN} = 48 V, V_{VDR} = 5.1 V +/- 2%, L1 = 420 nH [1] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		36	48	60	V
Input Current	I_{IN_DC}	V_{IN} = 48 V, T_C = 25°C, I_{OUT} = 10 A		0.762		A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	Short at terminals		3	-	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		1.265		mA
		Enabled (no load)		2.4		
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
EAIN Voltage Total Regulation	V_{OUT_DC}	[2]	0.985	1.00	1.015	V
Output Voltage Trim Range	V_{OUT_DC}	[2][3]	2.6	3.3	3.6	V
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$	@ 25°C, 36 V < V_{IN} < 60 V		0.10		%
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$	@ 25°C, 0.5 A < I_{OUT} < 10 A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 10 A, C_{OUT} = 6 x 100 µF, 20 MHz BW [4]		62		mVp-p
Output Current	I_{OUT_DC}	[5]	0		10	A
Current Limit	I_{OUT_CL}	L1 = 420 nH ±1%	-	11.5	-	A
Protection						
Input UVLO Start Threshold	V_{UVLO_START}		33.8	34.8	35.8	V
Input UVLO Stop Hysteresis	V_{UVLO_HYS}			0.9		V
Input UVLO Response Time				1.25		usec
Input OVLO Stop Threshold	V_{OVLO}		62	64.3	66.2	V
Input OVLO Start Hysteresis	V_{OVLO_HYS}			1.3		V
Input OVLO Response Time	t_f			1.25		usec
Output Overvoltage Protection	V_{OVP}	Above set V_{OUT}		20		%
Overtemperature Fault Threshold	T_{OTP}			130		°C
Ovetemperature Restart Hysteresis	T_{OTP_HYS}			30		°C
Timing						
Switching Frequency	f_S	[6] 48 V_{IN} to 3.3 V_{OUT}, 6 A out, L1 = 420 nH ±1%	-	400	-	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [3]	50		110	%
SYNCI Threshold	V_{SYNCI}			$V_{VDR}/2$		V

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

PI3543-00 (3.3 V_{OUT}) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, V_{IN} = 48 V, V_{VDR} = 5.1 V +/- 2%, L1 = 420 nH [1] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1 mA	V_{VDR} –0.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1 mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20 pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20 pF load		10		ns
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.08	V
TRK Enable Threshold	V_{TRK_OV}		20	40	60	mV
TRK to EAIN Offset	V_{EIAN_OV}		50	80	110	mV
Charge Current (Soft – Start)	I_{TRK}		-70	-50	-30	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5 V		10		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0	0.6	.94	1.6	mS
Error Amplifier Trans-Conductance	GMeao	[2]		5.1		ms
PSM Skip Threshold	PSM_{SKIP}	[2]		0.8		V
Error Amplifier Output Impedance	R_{OUT}	[2]	1			MOhm
Internal Compensation Capacitor	Chf	[2]		56		pf
Internal Compensation Resistor	Rzi	[2]		6k		Ohm
Enable						
High Threshold	V_{EN_HI}		0.9	1	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Enable Pull-Up Voltage (floating, no fault)	V_{EN_PU}			2		V
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}			0		V
Source Current	I_{EN_SO}			-50		µA
Sink Current	I_{EN_SK}			50		µA

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

PI3543-00 (3.3 V_{OUT}) Electrical Characteristics

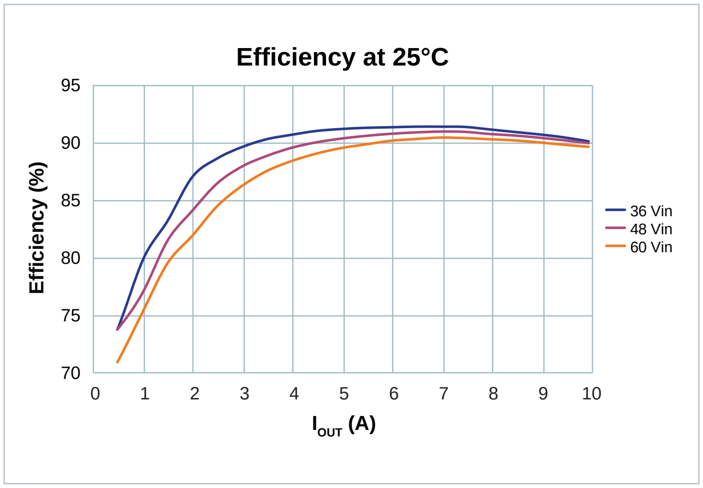


Figure 13 — Regulator Efficiency

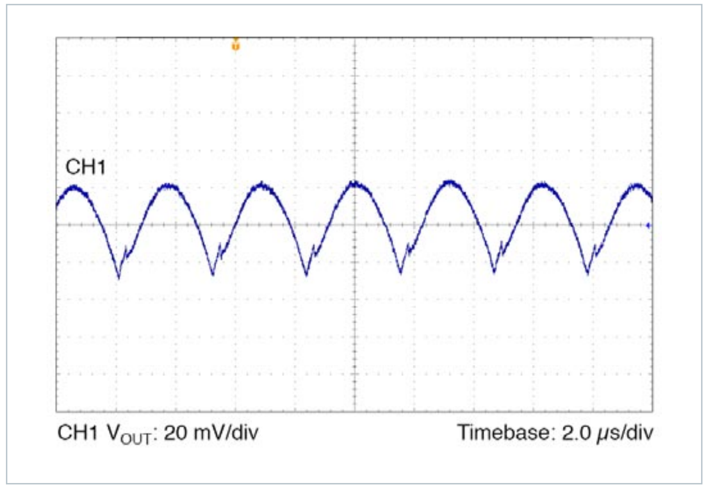


Figure 16 — Output Ripple: 48 V_{IN}, 3.3 V_{OUT} at 10 A. V_{OUT} = 20 mV/Div, 2.0 µs/Div; C_{OUT} = 6 x 100 µF Ceramic

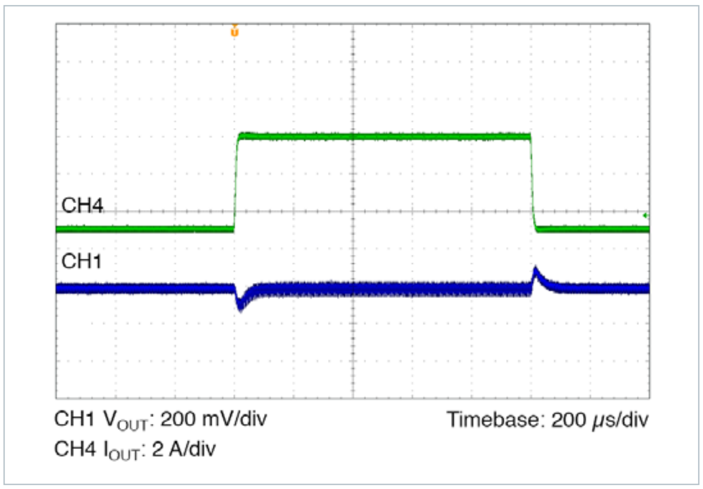


Figure 14 — Transient Response: 5 A to 10 A, at 1 A/µs. 48 V_{IN} to 3.3 V_{OUT},

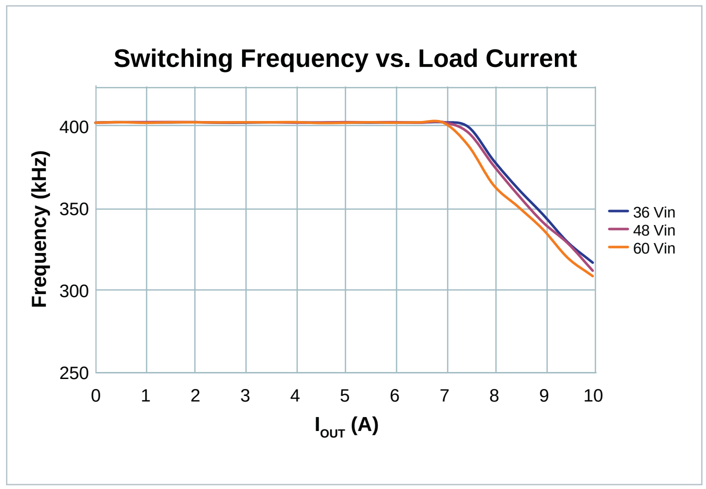


Figure 17 — Switching Frequency vs. Load Current

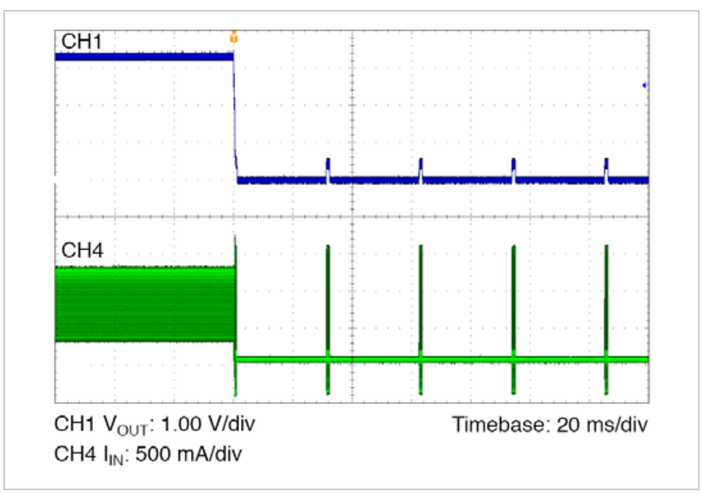


Figure 15 — Output Short Circuit @ V_{IN} = 48 V

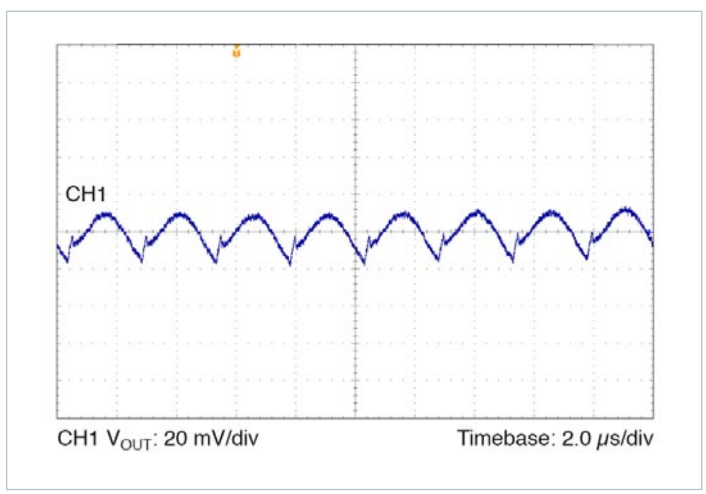


Figure 18 — Output Ripple: 48 V_{IN}, 3.3 V_{OUT} at 5 A. V_{OUT} = 20 mV/Div, 2.0 µs/Div; C_{OUT} = 6 x 100 µF Ceramic

PI3543-00 (3.3 V_{OUT}) Electrical Characteristics

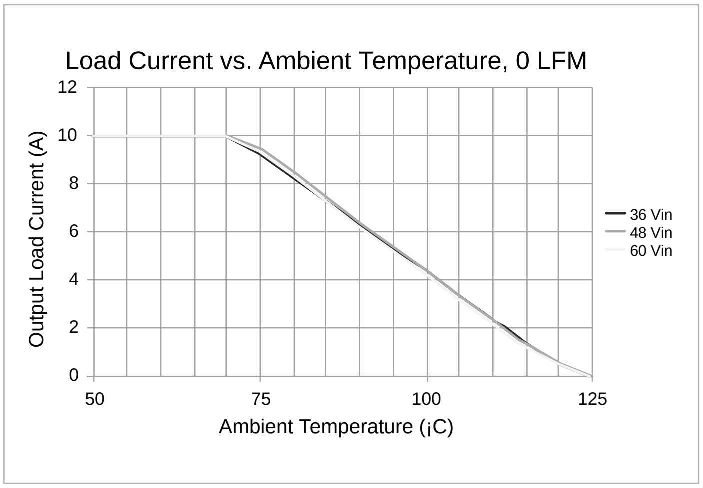


Figure 19 Load Current vs. Ambient Temperature, 0 LFM

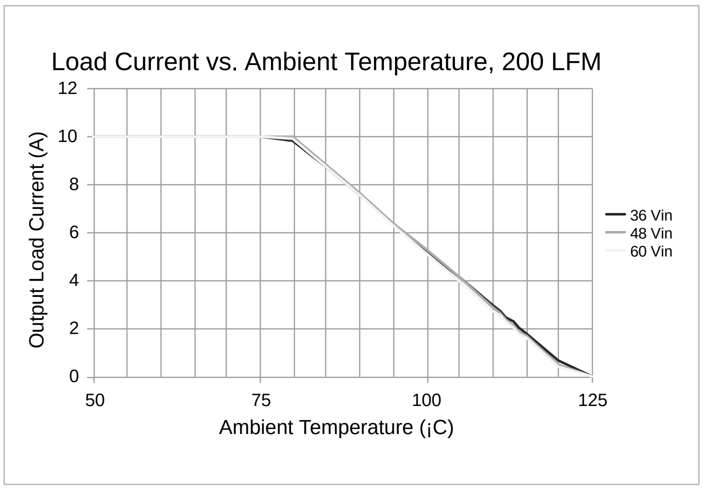


Figure 20 Load Current vs. Ambient Temperature, 200 LFM

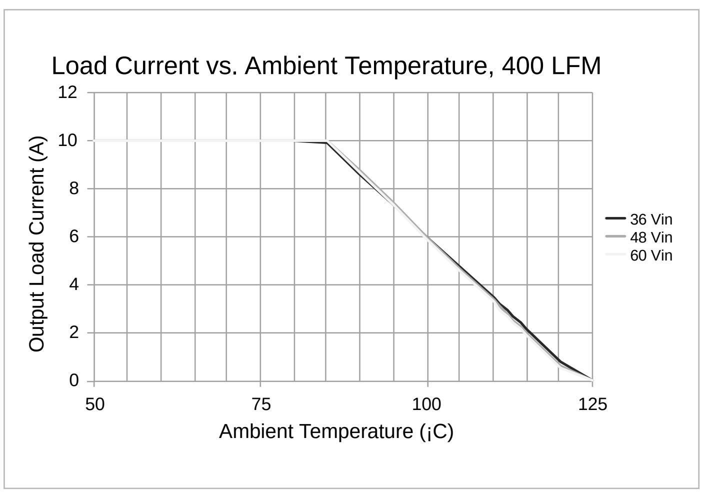


Figure 21 Load Current vs. Ambient Temperature, 400 LFM

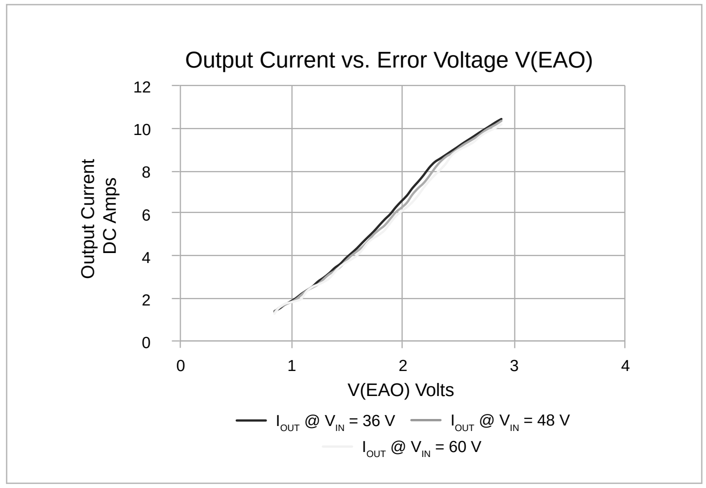


Figure 22 Output Current vs. Error Voltage V(EAO)

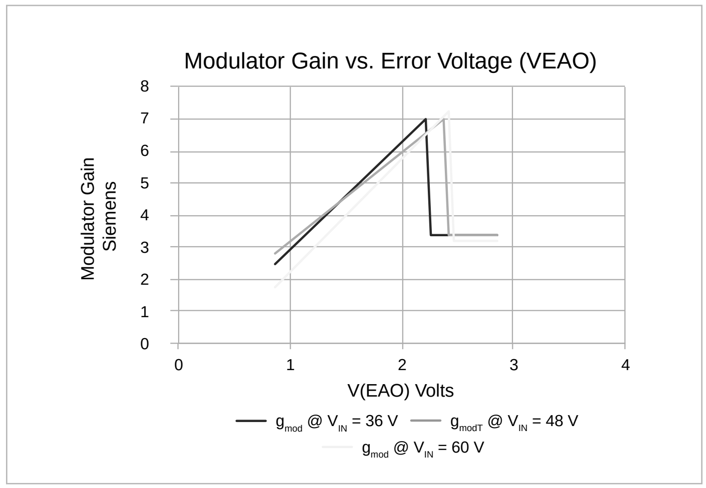


Figure 23 Modulator Gain vs. Error Voltage (VEAO)

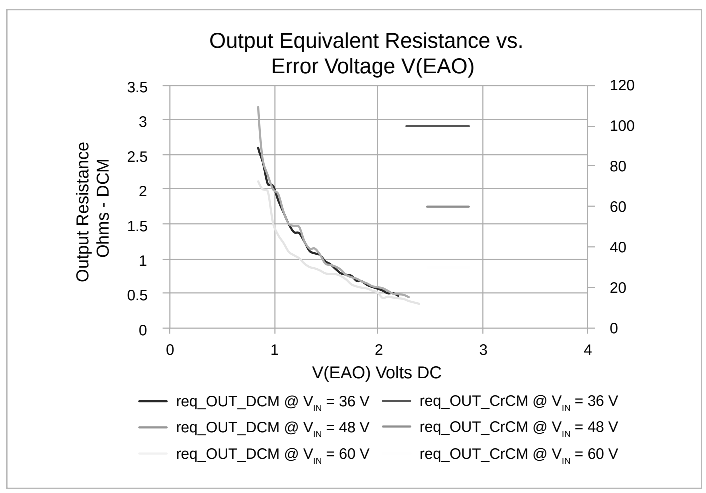


Figure 24 Output Equivalent Resistance vs. Error Voltage V(EAO)

PI3545-00 (5.0 V_{OUT}) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, V_{IN} = 48 V, V_{VDR} = 5.1 V +/- 2%, L1 = 420 nH [1] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		36	48	60	V
Input Current	I_{IN_DC}	V_{IN} = 48 V, T_C = 25°C, I_{OUT} = 10 A		1.126		A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	Short at terminals		3.2	-	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		1.26		mA
		Enabled (no load)		2.42		
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
EAIN Voltage Total Regulation	V_{OUT_DC}	[2]	0.985	1.00	1.015	V
Output Voltage Trim Range	V_{OUT_DC}	[2][3]	4.0	5.0	5.5	V
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$	@ 25°C, 36 V < V_{IN} < 60 V		0.10		%
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$	@ 25°C, 0.5 A < I_{OUT} < 10 A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 10 A, C_{OUT} = 6 x 47 µF, 20 MHz BW [4]		62.4		mVp-p
Output Current	I_{OUT_DC}	[5]	0		10	A
Current Limit	I_{OUT_CL}	L1 = 420 nH ±1%	-	12	-	A
Protection						
Input UVLO Start Threshold	V_{UVLO_START}		33.8	34.8	35.8	V
Input UVLO Stop Hysteresis	V_{UVLO_HYS}			2.6		V
Input UVLO Response Time				1.25		usec
Input OVLO Stop Threshold	V_{OVLO}		62	64.3	66.2	V
Input OVLO Start Hysteresis	V_{OVLO_HYS}			1.3		V
Input OVLO Response Time	t_f			1.25		usec
Output Overvoltage Protection	V_{OVP}	Above set V_{OUT}		20		%
Overtemperature Fault Threshold	T_{OTP}			130		°C
Ovetemperature Restart Hysteresis	T_{OTP_HYS}			30		°C
Timing						
Switching Frequency	f_S	[6] 48 V_{IN} to 55 V_{OUT}, 3 A out, L1 = 420 nH ±1%	-	600	-	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [3]	50		110	%
SYNCI Threshold	V_{SYNCI}			$V_{VDR}/2$		V

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

PI3545-00 (5.0 V_{OUT}) Electrical Characteristics

Specifications apply for -40°C <T_J < 125°C, V_{IN} = 48 V, V_{VDR} = 5.1 V +/- 2%, L1 = 420 nH [1] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Sync Out (SYNCO)						
SYNCO High	V_{SYNCO_HI}	Source 1 mA	V_{VDR} –0.5			V
SYNCO Low	V_{SYNCO_LO}	Sink 1 mA			0.5	V
SYNCO Rise Time	t_{SYNCO_RT}	20 pF load		10		ns
SYNCO Fall Time	t_{SYNCO_FT}	20 pF load		10		ns
Soft Start, Tracking and Error Amplifier						
TRK Active Range (Nominal)	V_{TRK}		0		1.08	V
TRK Enable Threshold	V_{TRK_OV}		20	40	60	mV
TRK to EAIN Offset	V_{EIAN_OV}		50	80	110	mV
Charge Current (Soft – Start)	I_{TRK}		-70	-50	-30	µA
Discharge Current (Fault)	I_{TRK_DIS}	V_{TRK} = 0.5 V		10		mA
Soft-Start Time	t_{SS}	C_{TRK} = 0	0.6	.94	1.6	mS
Error Amplifier Trans-Conductance	GMeao	[2]		5.1		ms
PSM Skip Threshold	PSM_{SKIP}	[2]		0.8		V
Error Amplifier Output Impedance	R_{OUT}	[2]	1			MOhm
Internal Compensation Capacitor	Chf	[2]		56		pf
Internal Compensation Resistor	Rzi	[2]		6k		Ohm
Enable						
High Threshold	V_{EN_HI}		0.9	1	1.1	V
Low Threshold	V_{EN_LO}		0.7	0.8	0.9	V
Threshold Hysteresis	V_{EN_HYS}		100	200	300	mV
Enable Pull-Up Voltage (floating, no fault)	V_{EN_PU}			2		V
Enable Pull-Down Voltage (floating, faulted)	V_{EN_PD}			0		V
Source Current	I_{EN_SO}			-50		µA
Sink Current	I_{EN_SK}			50		µA

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

PI3545-00 (5.0 V_{OUT}) Electrical Characteristics

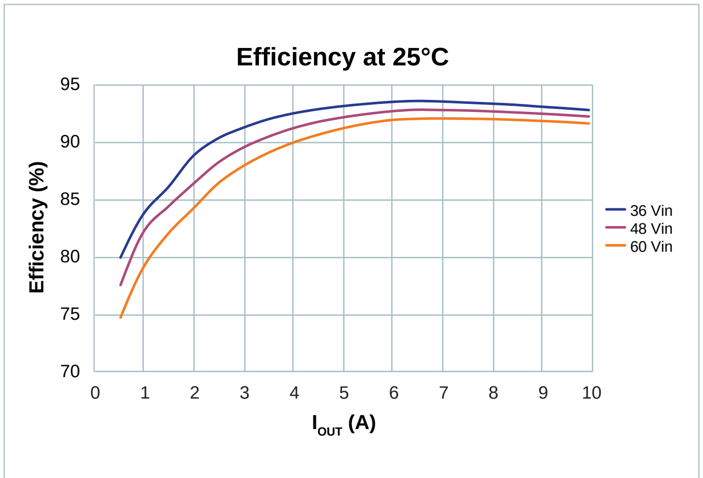


Figure 25 — Regulator Efficiency

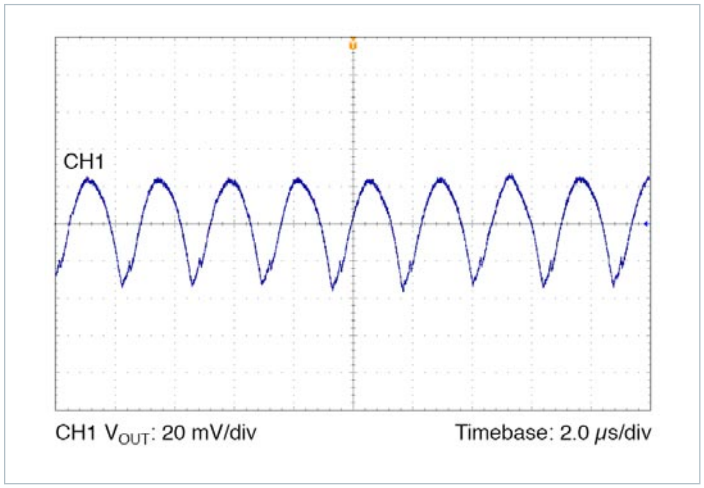


Figure 28 — Output Ripple: 48 V_{IN}, 5.0 V_{OUT} at 10 A. V_{OUT} = 20 mV/Div, 2.0 µs/Div; C_{OUT} = 6 x 47 µF Ceramic

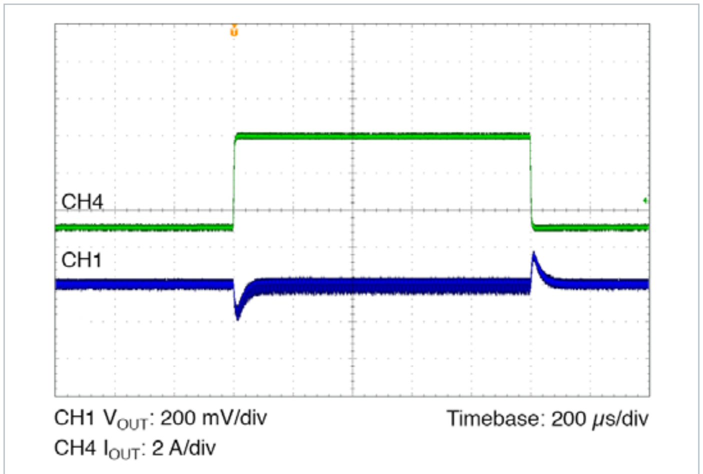


Figure 26 — Transient Response: 5 A to 10 A, at 1 A/µs. 48 V_{IN} to 5.0 V_{OUT} C_{OUT} = 6 x 47 µF Ceramic

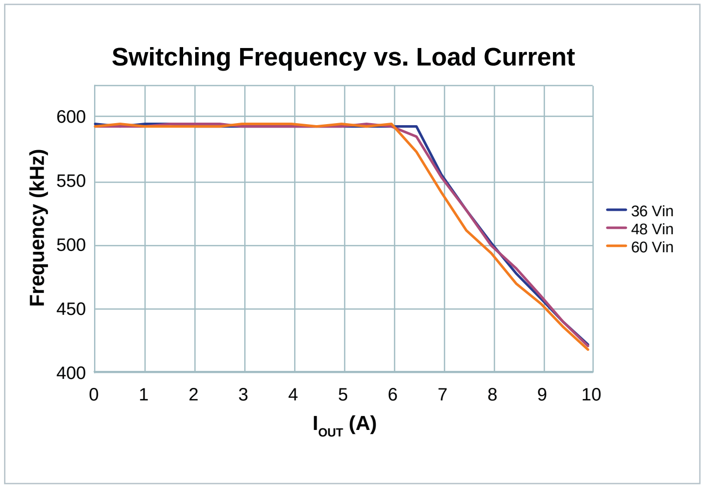


Figure 29 — Switching Frequency vs. Load Current

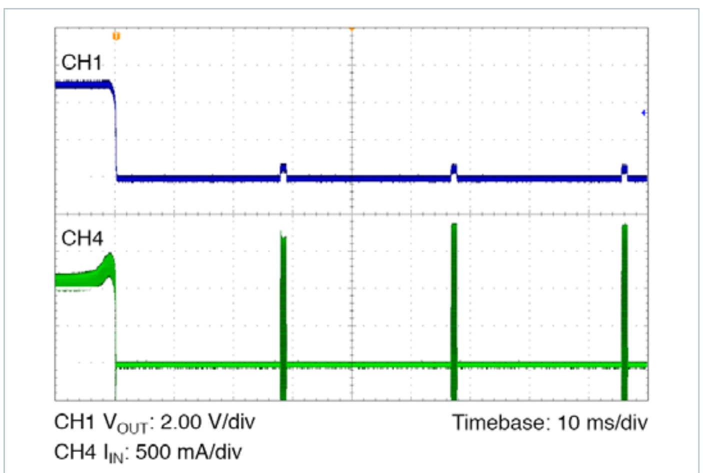


Figure 27 — Output Short Circuit @ V_{IN} = 48 V

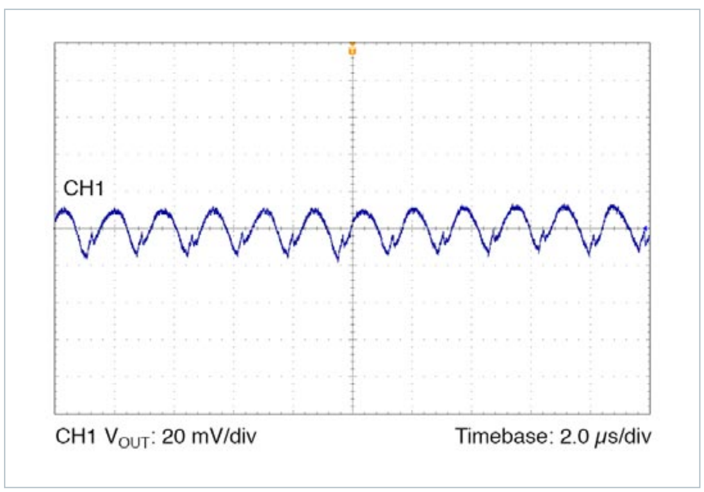


Figure 30 — Output Ripple: 48 V_{IN}, 5.0 V_{OUT} at 5 A. V_{OUT} = 20 mV/Div, 2.0 µs/Div; C_{OUT} = 6 x 47 µF Ceramic

PI3545-00 (5.0 V_{OUT}) Electrical Characteristics

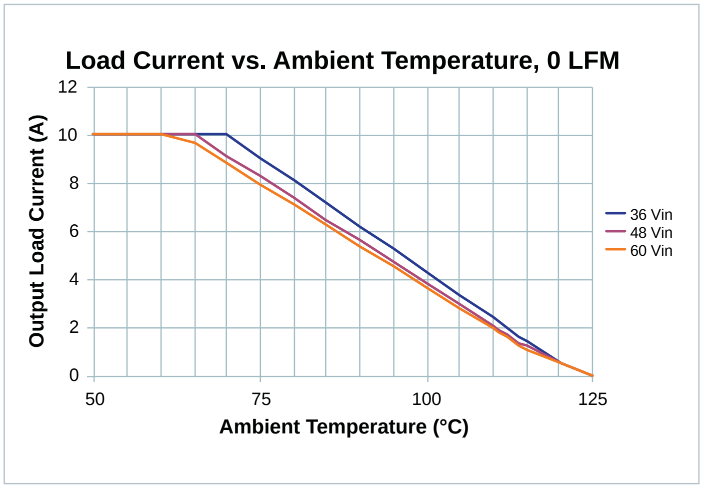


Figure 31 — Load Current vs. Ambient Temperature, 0 LFM

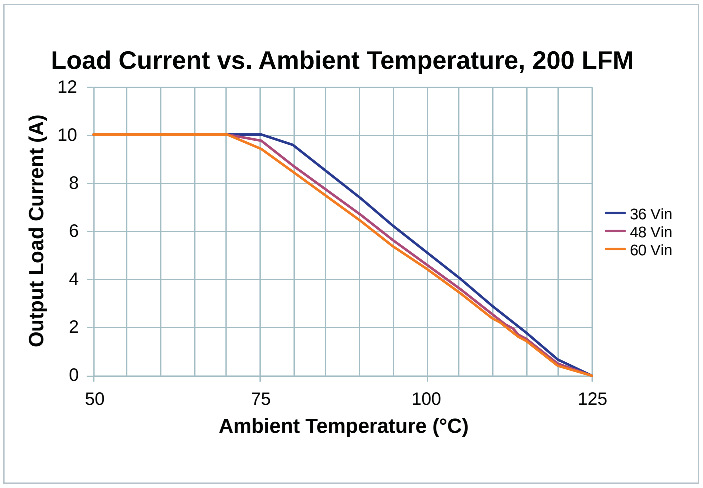


Figure 32 — Load Current vs. Ambient Temperature, 200 LFM

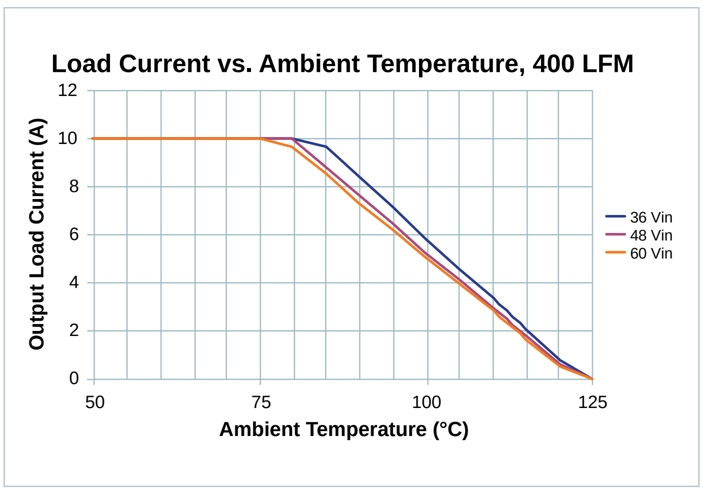


Figure 33 — Load Current vs. Ambient Temperature, 400 LFM

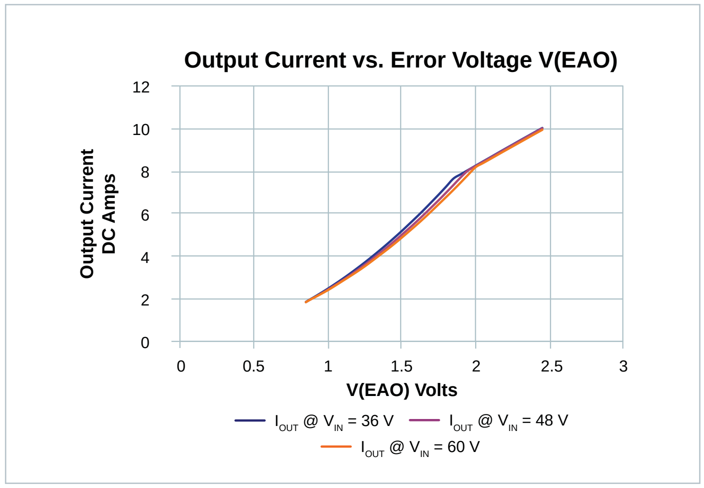


Figure 34 — Output Current vs. Error Voltage V(EAO)

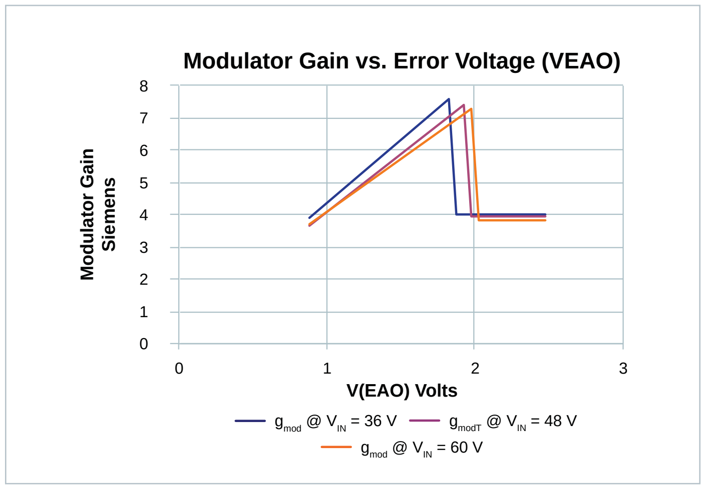


Figure 35 — Modulator Gain vs. Error Voltage (VEAO)

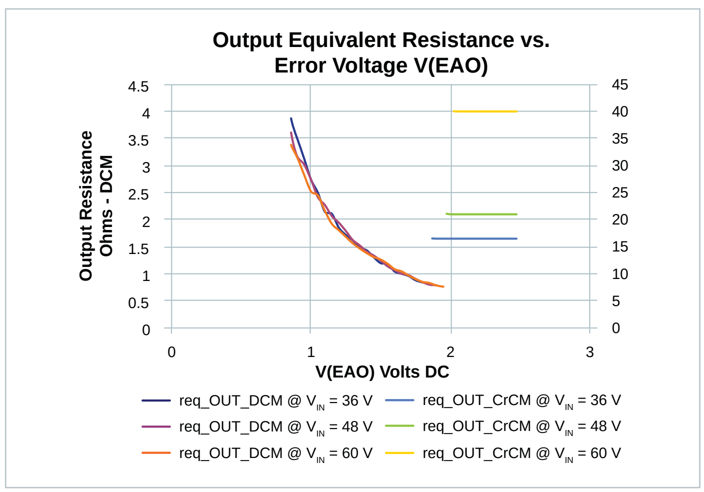


Figure 36 — Output Equivalent Resistance vs. Error Voltage V(EAO)

PI3546-00 (12.0 V_{OUT}) Electrical Characteristics

Specifications apply for -40°C < T_J < 125°C, V_{IN} = 48 V, V_{VDR} = 5.1 V +/- 2%, L1 = 900 nH [1] unless other conditions are noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage	V_{IN_DC}		36	48	60	V
Input Current	I_{IN_DC}	V_{IN} = 48 V, T_C = 25°C, I_{OUT} = 9 A		2.33		A
Input Current At Output Short (fault condition duty cycle)	I_{IN_Short}	Short at terminals		3.3	-	mA
Input Quiescent Current	I_{Q_VIN}	Disabled		1.26		mA
		Enabled (no load)		2.9		
Input Voltage Slew Rate	V_{IN_SR}				1	V/µs
Output Specifications						
EAIN Voltage Total Regulation	V_{OUT_DC}	[2]	0.985	1.00	1.015	V
Output Voltage Trim Range	V_{OUT_DC}	[2][3]	6.5	12	14	V
Line Regulation	$\Delta V_{OUT}(\Delta V_{IN})$	@ 25°C, 36 V < V_{IN} < 60 V		0.10		%
Load Regulation	$\Delta V_{OUT}(\Delta I_{OUT})$	@ 25°C, 0.5 A < I_{OUT} < 9 A		0.10		%
Output Voltage Ripple	V_{OUT_AC}	I_{OUT} = 9 A, C_{OUT} = 6 x 10 µF, 20 MHz BW [4]		114		mVp-p
Output Current	I_{OUT_DC}	[5]	0		9	A
Current Limit	I_{OUT_CL}	L1 = 900 nH ±1%	-	10.5	-	A
Protection						
Input UVLO Start Threshold	V_{UVLO_START}		33.8	34.8	35.8	V
Input UVLO Stop Hysteresis	V_{UVLO_HYS}			2.6		V
Input UVLO Response Time				1.25		usec
Input OVLO Stop Threshold	V_{OVLO}		62	64.3	66.2	V
Input OVLO Start Hysteresis	V_{OVLO_HYS}			1.3		V
Input OVLO Response Time	t_f			1.25		usec
Output Overvoltage Protection	V_{OVP}	Above set V_{OUT}		20		%
Overtemperature Fault Threshold	T_{OTP}			130		°C
Ovetemperature Restart Hysteresis	T_{OTP_HYS}			30		°C
Timing						
Switching Frequency	f_S	[6] 48 V_{IN} to 12 V_{OUT}, 2 A out, L1 = 900 nH ±1%	-	800	-	kHz
Fault Restart Delay	t_{FR_DLY}			30		ms
Sync In (SYNCI)						
Synchronization Frequency Range	Δf_{SYNCI}	Relative to set switching frequency [3]	50		110	%
SYNCI Threshold	V_{SYNCI}			$V_{VDR}/2$		V

[1] All parameters reflect regulator and inductor system performance. Measurements were made using a standard PI354x evaluation board with 2.5 x 4" dimensions and 4 layer, 2 oz copper. Refer to inductor pairing table within Application Description section for specific inductor manufacturer and value.
[2] Regulator is assured to meet performance specifications by design, test correlation, characterization, and/or statistical process control. Output voltage is determined by an external feedback divider ratio.
[3] Output current capability may be limited and other performance may vary from noted electrical characteristics when Vout is not set to nominal.
[4] Refer to Output Ripple plots.
[5] Refer to Load Current vs. Ambient Temperature curves.
[6] Refer to Switching Frequency vs. Load current curves.

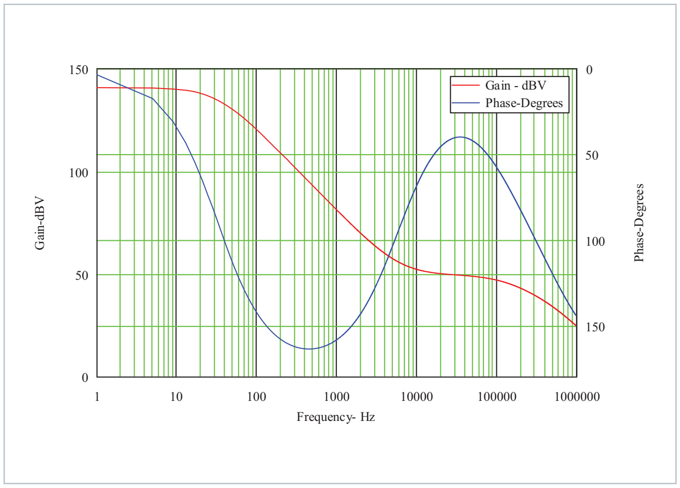


Figure 66 — GMlgh(s) Gain/Phase Plot Compensated

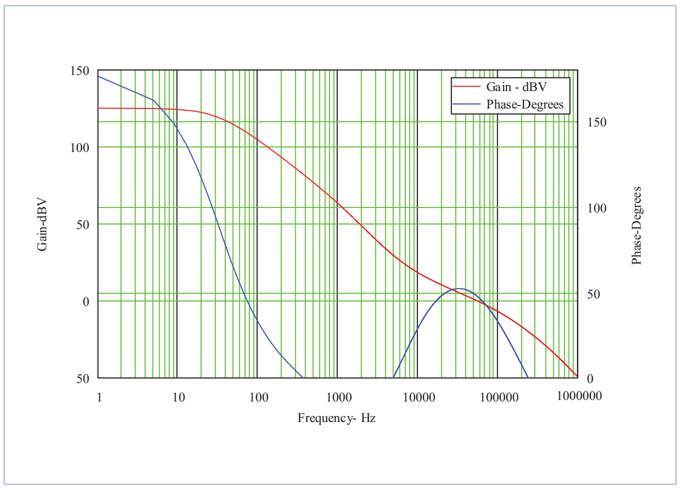


Figure 67 — Lighting Application Loop Gain/Phase Plot

Filter Considerations

The PI354x-00 requires low impedance ceramic input capacitors (X7R/X5R or equivalent) to ensure proper start up and high frequency decoupling for the power stage. The PI354x-00 will draw nearly all of the high frequency current from the low impedance ceramic capacitors when the main high side MOSFET(s) are conducting. During the time the MOSFET(s) are off, the input capacitors are replenished from the source. Table 4 shows the recommended input and output capacitors to be used for the PI354x-00 as well as per capacitor RMS ripple current and the input and output ripple voltages. Table 5 includes the recommended input and output ceramic capacitors.

It is very important to verify that the voltage supply source as well as the interconnecting lines are stable and do not oscillate.

Input Filter Case 1; Inductive source and local, external, input decoupling capacitance with negligible ESR (i.e.: ceramic type):

The voltage source impedance can be modeled as a series R(line) L(line) circuit. The high performance ceramic decoupling capacitors will not significantly damp the network because of their low ESR; therefore in order to guarantee stability the following conditions must be verified:

$$R_{line} > \frac{L_{line}}{(Cin_{int} + Cin_{ext}) \bullet |r\_EQin|} \quad (16)$$

$$R_{line} << |r\_EQin| \quad (17)$$

Where r_EQin can be calculated by dividing the lowest line voltage by the full load input current. It is critical that the line source impedance be at least an octave lower than the converter's dynamic input resistance, Equation (17). However, R_line cannot be made arbitrarily low otherwise Equation (16) is violated and the system will show instability, due to an under-damped RLC input network.

Input Filter case 2; Inductive source and local, external input decoupling capacitance with significant RCIN_EXT ESR (i.e.: electrolytic type):

In order to simplify the analysis in this case, the voltage source impedance can be modeled as a simple inductor Lline.

$$|r\_EQin| > R_{cin_{ext}} \quad (18)$$

$$\frac{L_{line}}{(Cin_{int} \bullet R_{cin_{ext}})} > |r\_EQin| \quad (19)$$

Notice that, the high performance ceramic capacitors CIN_INT within the PI354x-00 should be included in the external electrolytic capacitance value for this purpose. The stability criteria will be:

Equation (19) shows that if the aggregate ESR is too small – for example by using very high quality input capacitors (C_{IN_EXT}) – the system will be under-damped and may even become destabilized. As noted, an octave of design margin in satisfying Equation (18) should be considered the minimum.

When applying an electrolytic capacitor for input filter damping the ESR value must be chosen to avoid loss of converter efficiency and excessive power dissipation in the electrolytic capacitor.

VDR Bias Regulator

The VDR internal bias regulator is a ZVS switching regulator that resides internal to the PI354x-00 product family. It is intended strictly for use to power the internal controller and driver circuitry. The power capability of this regulator is sized only for the PI354x-00, with adequate reserve for the application it was intended for. It may be used for as a pull-up source for open collector applications and for other very low power use with the following restrictions:

1. No direct connection is allowed. Any noise source that can disturb the VDR voltage can also affect the internal controller operation.
2. All loads must be locally de-coupled using a 0.1 µF ceramic capacitor. This capacitor must be connected to the VDR output through a series resistor no smaller than 1 k. which forms a loss pass filter and limits the total current to 5 mA.

System Design Considerations

1. Inductive loads- As with all power electronic applications, consideration must be given to driving inductive loads that may be exposed to a fault in the system which could result in consequences beyond the scope of the power supply primary protection mechanisms. An inductive load could be a filter, fan motor or even excessively long cables. Consider an instantaneous short circuit through an un-damped inductance that occurs when the output capacitors are already at an initial condition of fully charged. The only thing that limits the current is the inductance of the short circuit and any series resistance. Even if the power supply is off at the time of the short circuit, the current could ramp up in the external inductor and store considerable energy. The release of this energy will result in considerable ringing, with the possibility of ringing nodes connected to the output voltage below ground. The system designer should plan for this by considering the use of other external circuit protection such as load switches, fuses, and transient voltage protectors. The inductive filters should be critically damped to avoid excessive ringing or damaging voltages. Adding a high current Schottky diode from the output voltage to PGND close to the PI354x-00 is recommended for these applications.
2. Low voltage operation – there is no isolation from an SELV (Safety-Extra-Low-Voltage) power system. Powering low voltage loads from input voltages as high as 60 V may require additional consideration to protect low voltage circuits from excessive voltage in the event of a short circuit from input to output. A fast TVS (transient voltage suppressor) gating an external load switch is an example of such protection.
3. Use of Lighting Mode (LGH) as a battery charger is certainly very feasible. It is fashionable to design these chargers such that the battery is always connected to it. Since the Buck topology is not isolated, shorting the input terminals or capacitors of an unpowered regulator/charger could allow damaging current flow through the body diode of the high side MOSFET that would be unprotected by a conventional input fuse. It is recommended to connect the PI354x-00 family to the battery using an active ORing device if LGH mode is used as a constant current battery charger. The same should be considered for super-capacitor applications as well.

Device	V_{IN} (V)	I_{LOAD} (A)	C_{INPUT} Ceramic X5R	C_{OUTPUT} Ceramic X5R	C_{INPUT} Ripple Current (I_{RMS})	C_{OUTPUT} Ripple Current (I_{RMS})	Input Ripple (mVpp)	Output Ripple (mVpp)	Transient Deviation (mVpk)	Recovery Time (µs)	Load Step (A) (Slew/µs)
PI3542	48	10	5 x 2.2 µF 100 V	6 x 100 µF	0.7	1.32	416	47	-/+80	40	5 (1 A/µs)
		5					220	22			
PI3543	48	10	5 x 2.2 µF 100 V	6 x 100 µF	0.8	1.3	464	61.6	-/+90	40	5 (1 A/µs)
		5					230	31			
PI3545	48	10	5 x 2.2 µF 100 V	6 x 47 µF	.88	1.37	485	62	-/+150	40	5 (1 A/µs)
		5					245	32			
PI3546	48	9	5 x 2.2 µF 100 V	6 x 10 µF	1.12	1.26	880	114	-/+300	20	5 (1 A/µs)
		4.5					125	33			

Table 3 — Recommended input and output capacitance

Murata Part Number	Description
C3225X7S1H1106M250AB	2.2 µF 100 V 1210 X7R
C3225X7S1H106M250AB	10 µF 50 V 1210 X7R
GRM31CR60J107ME39L	100 µF 6.3 V 1206 X7R
GRM31CR61A476ME15L	47 µF 10 V 1206 X5R
GRM32ER61H106MA12	10 µF 50 V 1210 X7R

Table 4 — Capacitor manufacturer part numbers

Layout Guidelines

To optimize maximum efficiency and low noise performance from a PI354x-00 design, layout considerations are necessary. Reducing trace resistance and minimizing high current loop returns along with proper component placement will contribute to optimized performance.

A typical buck converter circuit is shown in Figure 68. The potential areas of high parasitic inductance and resistance are the circuit return paths, shown as LR below.

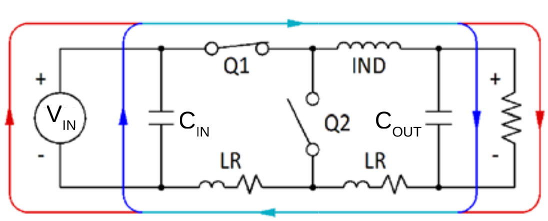


Figure 68 — Typical Buck Regulator

The path between the COUT and CIN capacitors is of particular importance since the AC currents are flowing through both of them when Q1 is turned on. Figure 69, schematically, shows the reduced trace length between input and output capacitors. The shorter path lessens the effects that copper trace parasitics can have on the PI354x-00 performance.

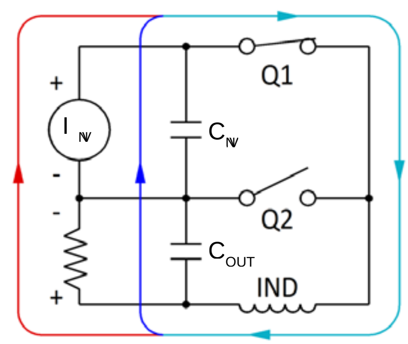


Figure 69 — Current flow: Q1 closed

When Q1 is on and Q2 is off, the majority of C_{IN}'s current is used to satisfy the output load and to recharge the C_{OUT} capacitors. When Q1 is off and Q2 is on, the load current is supplied by the inductor and the C_{OUT} capacitor as shown in Figure 70. During this period C_{IN} is also being recharged by the V_{IN}. Minimizing C_{IN} loop inductance is important to reduce peak voltage excursions when Q1 turns off. Also, the difference in area between the C_{IN} loop and C_{OUT} loop is vital to minimize switching and GND noise.

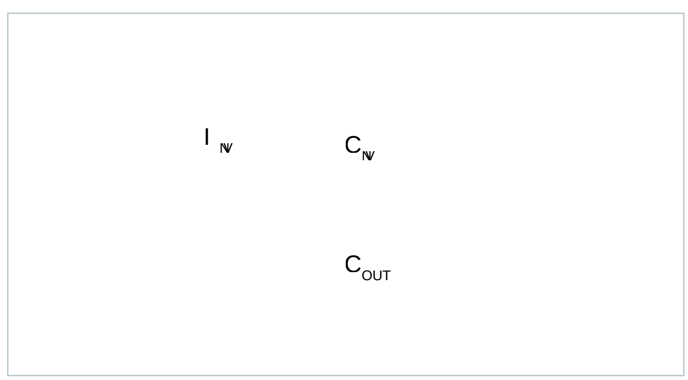


Figure 70 — Current flow: Q2 closed

The recommended component placement, shown in Figure 71, illustrates the tight path between C_{IN} and C_{OUT} (and V_{IN} and V_{OUT}) for the high AC return current. This optimized layout is used on the PI354x-00 evaluation board.

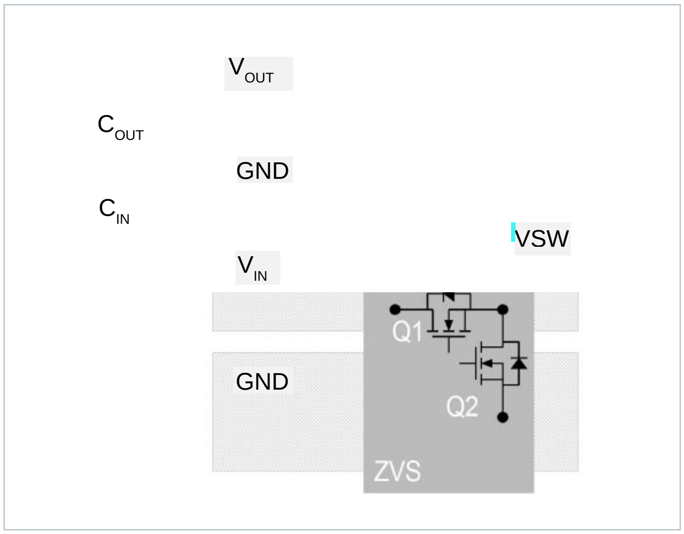


Figure 71 — Recommended component placement and metal routing

Figure 72 details the recommended receiving footprint for PI354x-00 10 mm x 10 mm package. All pads should have a final copper size of 0.55 mm x 0.55 mm, whether they are solder-mask defined or copper defined, on a 1 mm x 1 mm grid. All stencil openings are 0.45 mm when using either a 5 mil or 6 mil stencil.

Recommended PCB Footprint and Stencil

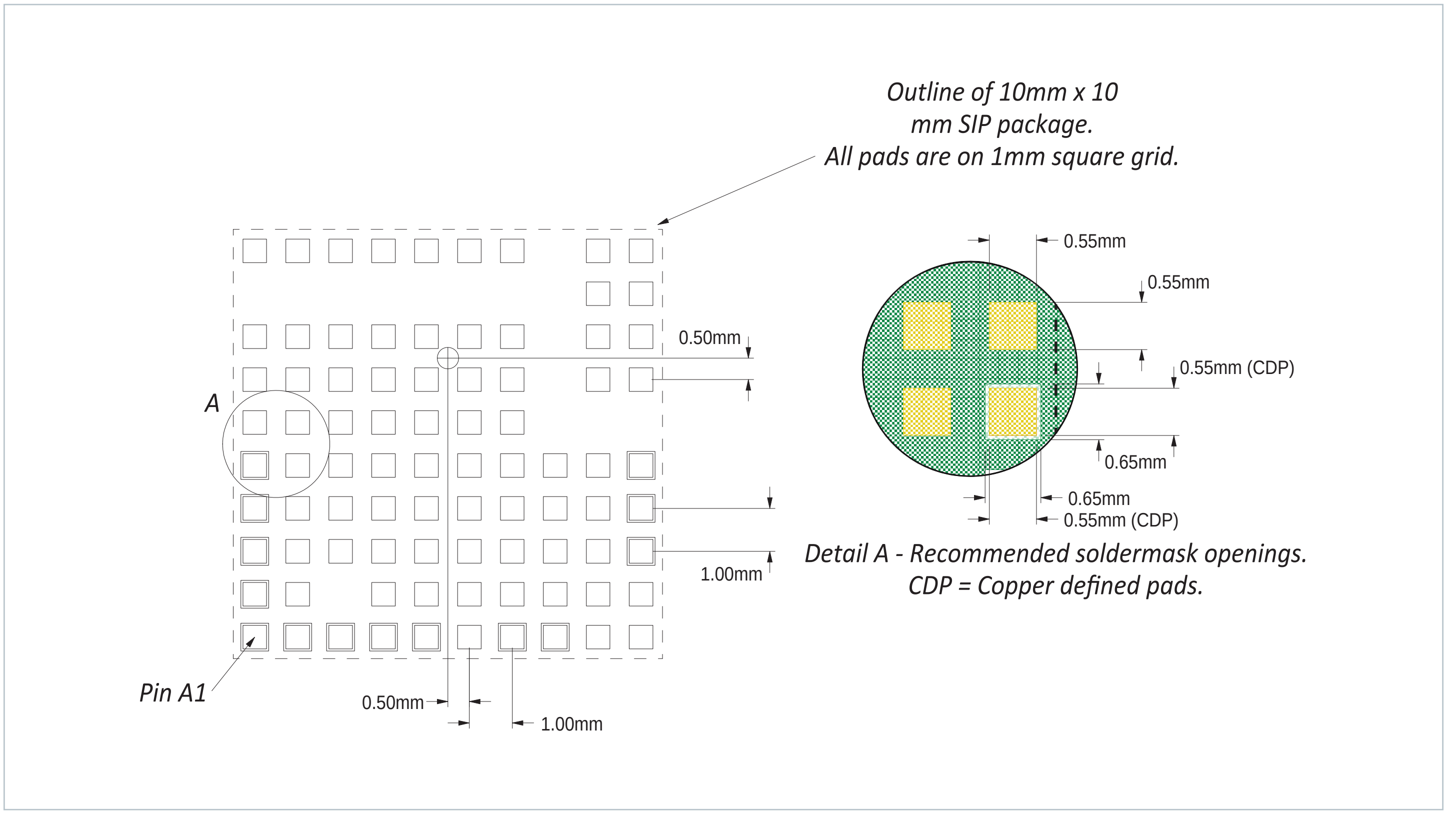
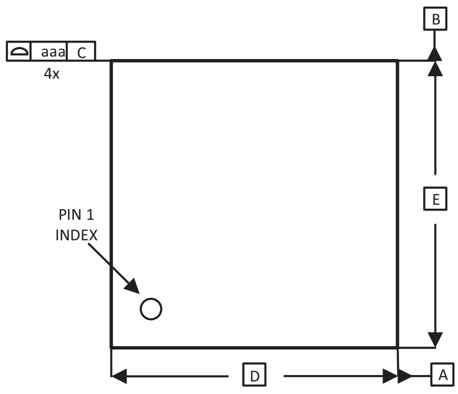
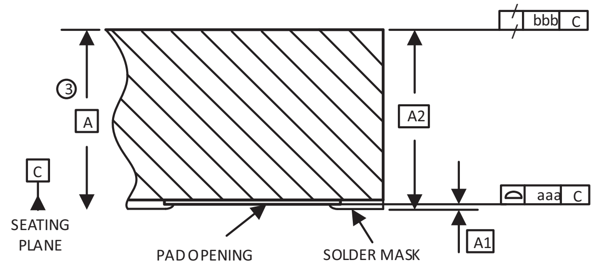


Figure 72 — Recommended Receiving PCB footprint

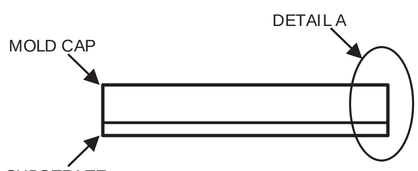
Package Drawings



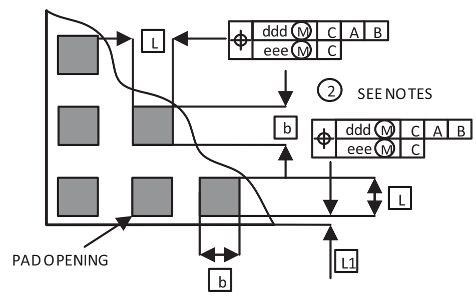
PACKAGE TOP VIEW



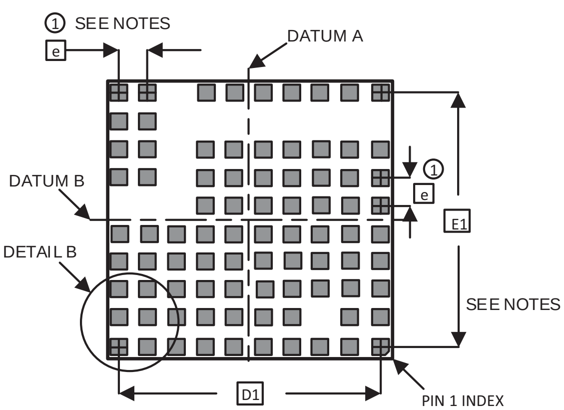
DETAIL A



PACKAGE SIDE VIEW



DETAIL B



PACKAGE BOTTOM VIEW

NOTES

1. 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
2. DIMENSION 'b' APPLIES TO METALLIZED PAD OPENING.
3. DIMENSION 'A' INCLUDES PACKAGE WARPAGE.
4. EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.
5. ALL DIMENSIONS IN MILLIMETERS.

SYMBOL	MIN	NOM	MAX
A	2.49	2.56	2.63
A1	–	–	0.04
A2	–	–	2.59
b	0.50	0.55	0.60
L	0.50	0.55	0.60
D	10.00 BSC		
E	10.00 BSC		
D1	9.00 BSC		
E1	9.00 BSC		
e	1.00 BSC		
L1	0.175	0.225	0.275
aaa			0.10
bbb			0.10
ccc			0.08
ddd			0.10
eee			0.08

DIMENSIONS

Revision History

Revision	Date	Description	Page Number(s)
1.0 - 1.1	05/2015	Released Engineering format/style	n/a
1.2	10/12/15	Reformatted in new template	n/a
1.3	02/19/2016	Updated PCB Footprint	34

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