

20V N-Channel Enhancement Mode MOSFET

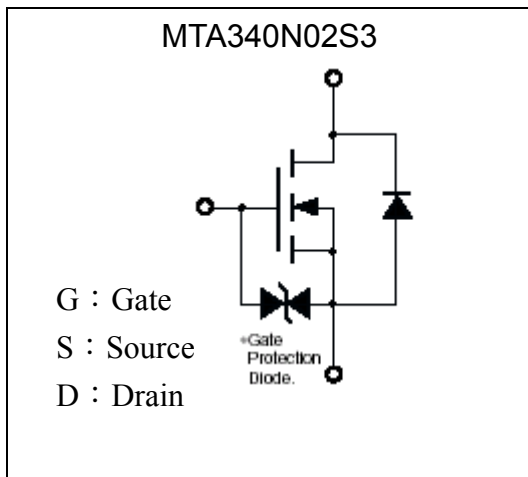
MTA340N02S3

BV_{DSS}	20V
$I_D@V_{GS}=4.5V, T_A=25^\circ C$	0.8A
$R_{DS(on)}@V_{GS}=4.5V, I_D=650mA$	264mΩ (typ)
$R_{DS(on)}@V_{GS}=2.5V, I_D=500mA$	325mΩ (typ)
$R_{DS(on)}@V_{GS}=1.8V, I_D=200mA$	371mΩ (typ)

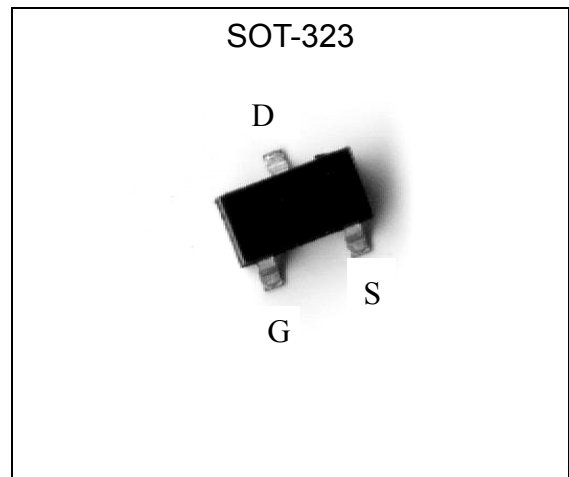
Features

- Simple drive requirement
- Small package outline
- ESD protected gate
- Pb-free lead plating and halogen-free package

Symbol

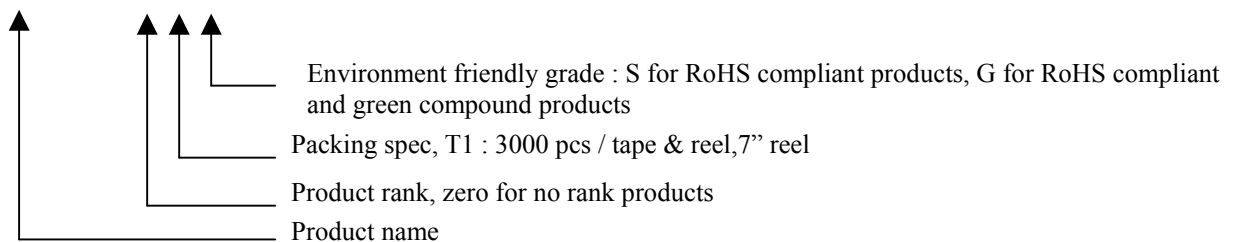


Outline



Ordering Information

Device	Package	Shipping
MTA340N02S3-0-T1-G	SOT-323 (Pb-free lead plating and halogen-free package)	3000 pcs / Tape & Reel





Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V _{DS}	20	V
Gate-Source Voltage	V _{GS}	±12	
Continuous Drain Current @ TA=25°C, VGS=4.5V (Note 3)	I _D	0.8	A
Continuous Drain Current @ TA=70°C, VGS=4.5V (Note 3)		0.64	
Pulsed Drain Current (Notes 1, 2)	I _{DM}	3.2	
Maximum Power Dissipation@ TA=25°C (Note 3)	P _D	0.34	W
Operating Junction and Storage Temperature Range	T _j ; T _{stg}	-55~+150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance, Junction-to-Ambient, max (Note3)	R _{θJA}	367	°C/W
Thermal Resistance, Junction-to-Case, max	R _{θJC}	250	

- Note : 1. Pulse width limited by maximum junction temperature.
 2. Pulse width ≤ 300μs, duty cycle ≤ 2%.
 3. Surface mounted on 1 in² copper pad of FR-4 board; 270°C/W when mounted on minimum copper pad

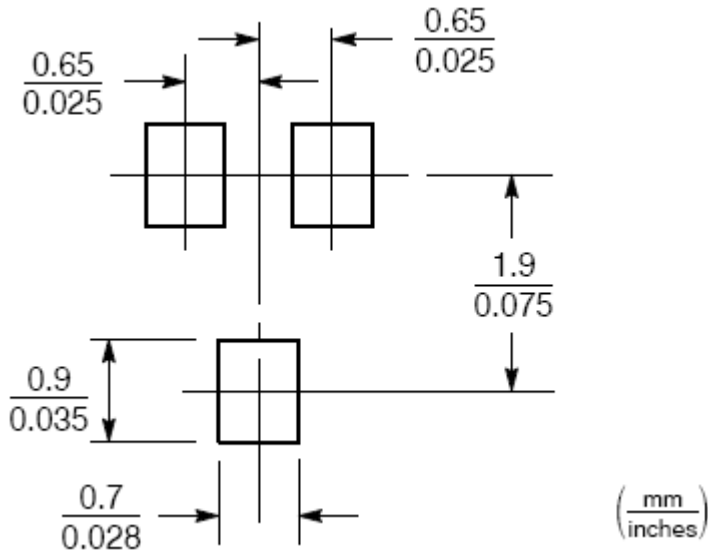
Electrical Characteristics (Tj=25°C, unless otherwise noted)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV _{DSS}	20	-	-	V	V _{GS} =0V, I _D =250μA
V _{GS(th)}	0.45	-	1.0		V _{DS} =V _{GS} , I _D =250μA
I _{GSS}	-	-	±10	μA	V _{GS} =±10V, V _{DS} =0V
I _{DSS}	-	-	1		V _{DS} =20V, V _{GS} =0V
	-	-	25		V _{DS} =16V, V _{GS} =0V (T _j =70°C)
*R _{Ds(ON)}	-	264	350	mΩ	V _{GS} =4.5V, I _D =650mA
	-	325	660		V _{GS} =2.5V, I _D =500mA
	-	371	2000		V _{GS} =1.8V, I _D =500mA
*G _{FS}	-	2.4	-	S	V _{DS} =5V, I _D =1A
Dynamic					
C _{iSS}	-	64	-	pF	V _{DS} =10V, V _{GS} =0V, f=1MHz
C _{oSS}	-	17	-		
C _{rSS}	-	20	-		
t _{d(ON)}	-	2.6	-	ns	V _{DS} =10V, I _D =0.5A, V _{GS} =10V, R _G =1Ω
t _r	-	16	-		
t _{d(OFF)}	-	29.8	-		
t _f	-	11	-		
Q _g	-	1.3	-	nC	V _{DS} =15V, I _D =0.5A, V _{GS} =4.5V
Q _{gs}	-	0.5	-		
Q _{gd}	-	0.1	-		

Source-Drain Diode					
*I _S	-	-	0.8	A	
*I _{SM}	-	-	3.2		
*V _{SD}	-	0.8	1	V	V _{GS} =0V, I _S =150mA
T _{rr}	-	4.9	-	ns	V _{GS} =0V, I _F =0.5A, dI _F /dt=100A/μs
Q _{rr}	-	1.0	-	nC	

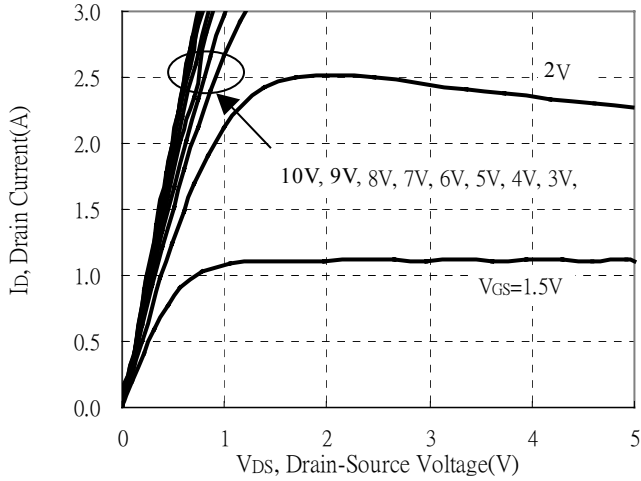
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Recommended Soldering Footprint

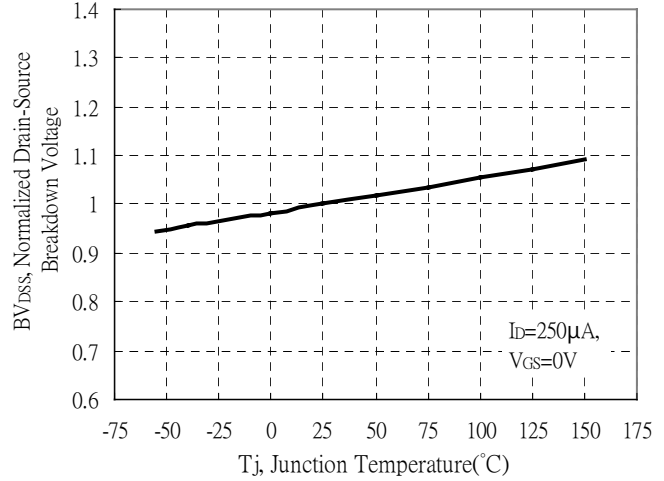


Typical Characteristics

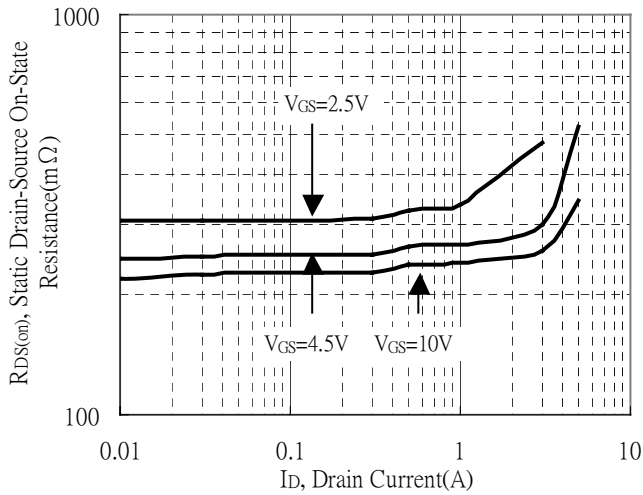
Typical Output Characteristics



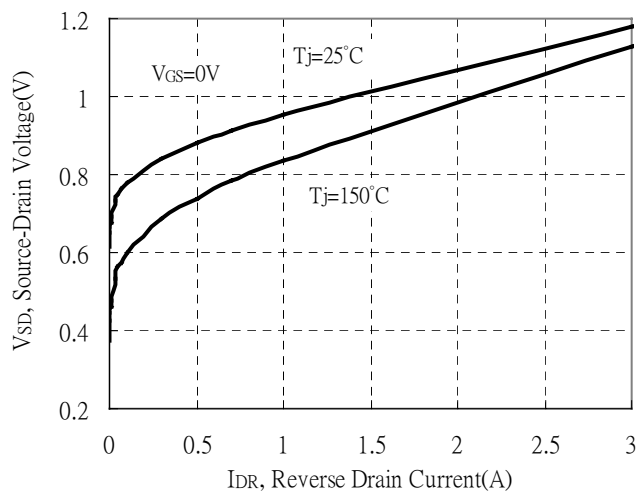
Brekdown Voltage vs Ambient Temperature



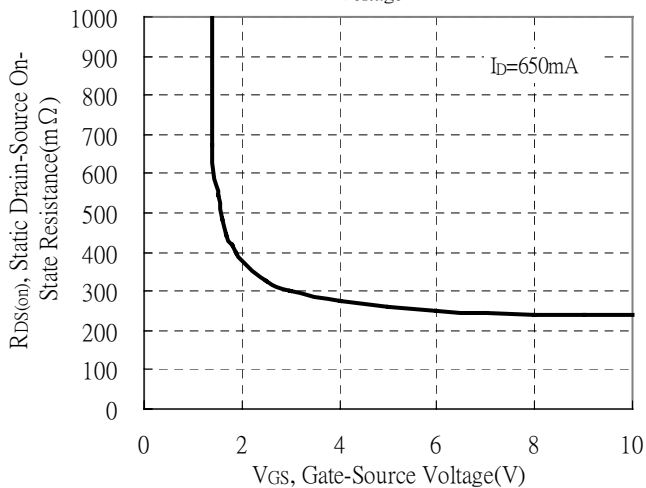
Static Drain-Source On-State resistance vs Drain Current



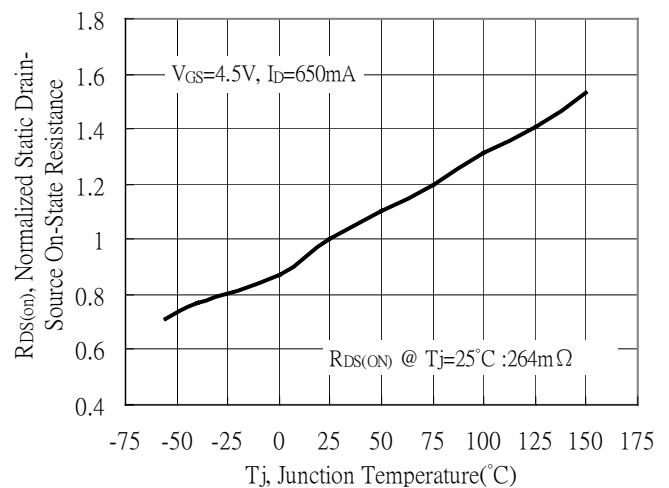
Reverse Drain Current vs Source-Drain Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

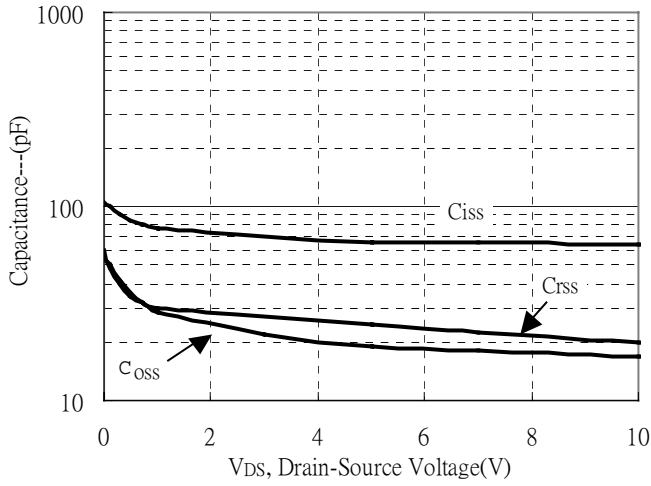


Drain-Source On-State Resistance vs Junction Temperature

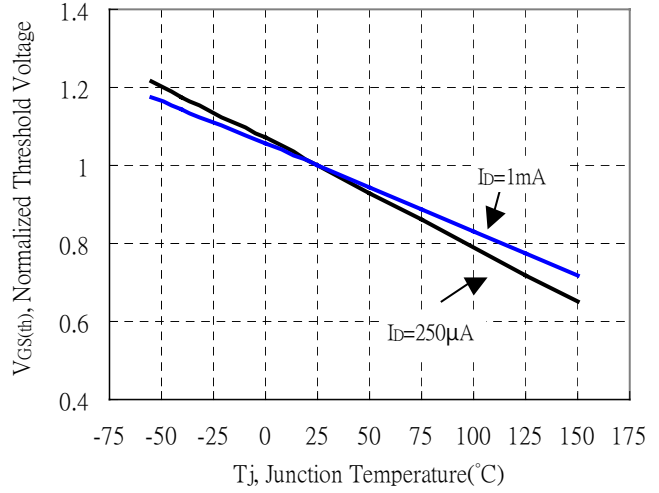


Typical Characteristics(Cont.)

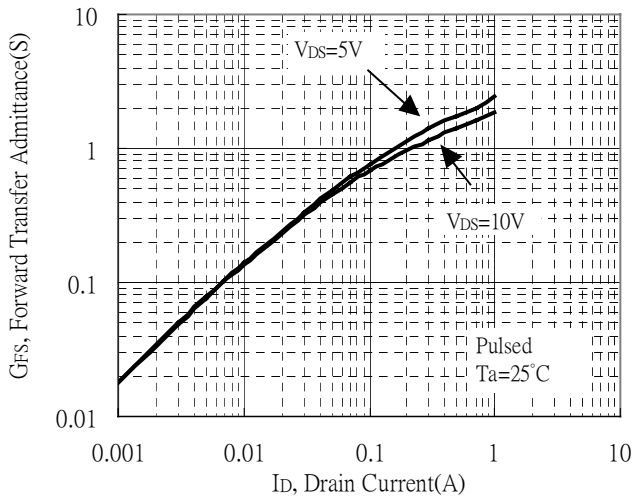
Capacitance vs Drain-to-Source Voltage



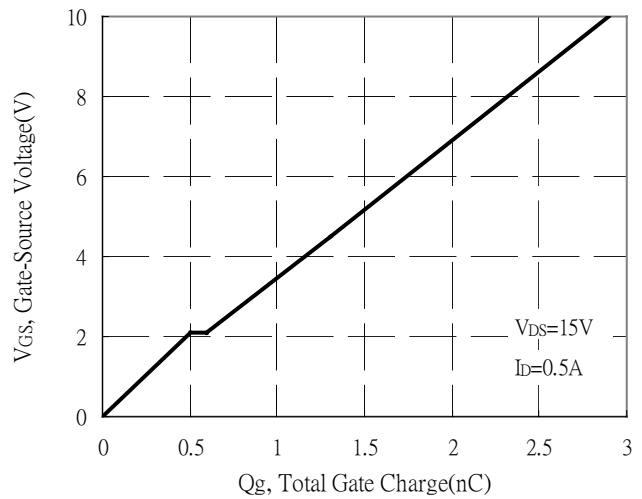
Threshold Voltage vs Junction Temperature



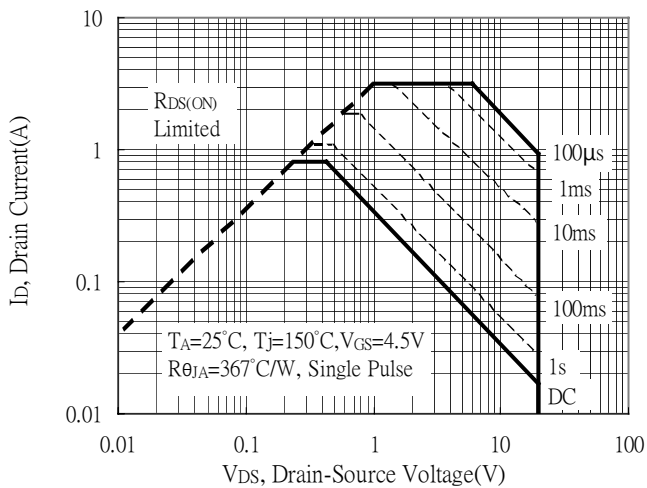
Forward Transfer Admittance vs Drain Current



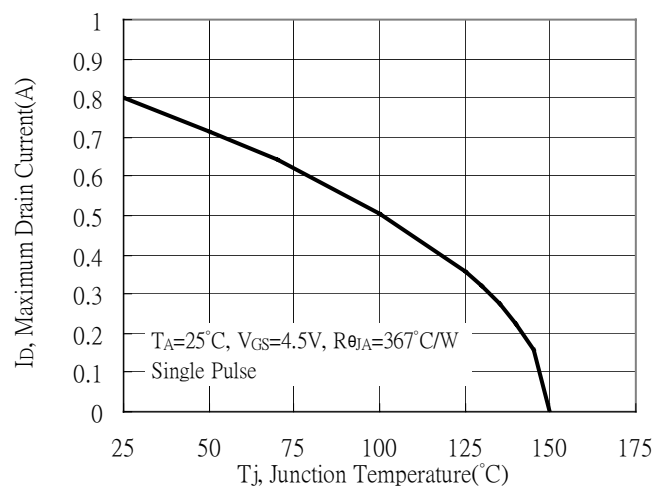
Gate Charge Characteristics



Maximum Safe Operating Area

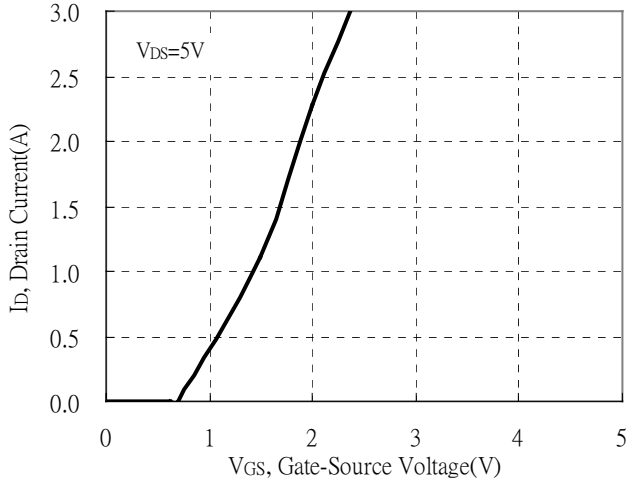


Maximum Drain Current vs Junction Temperature

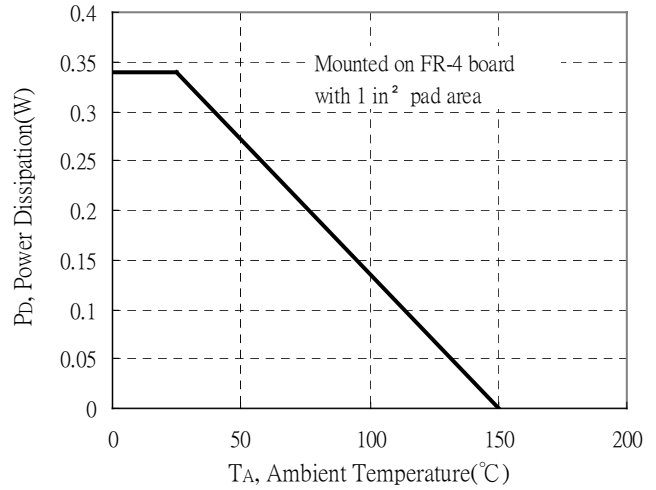


Typical Characteristics(Cont.)

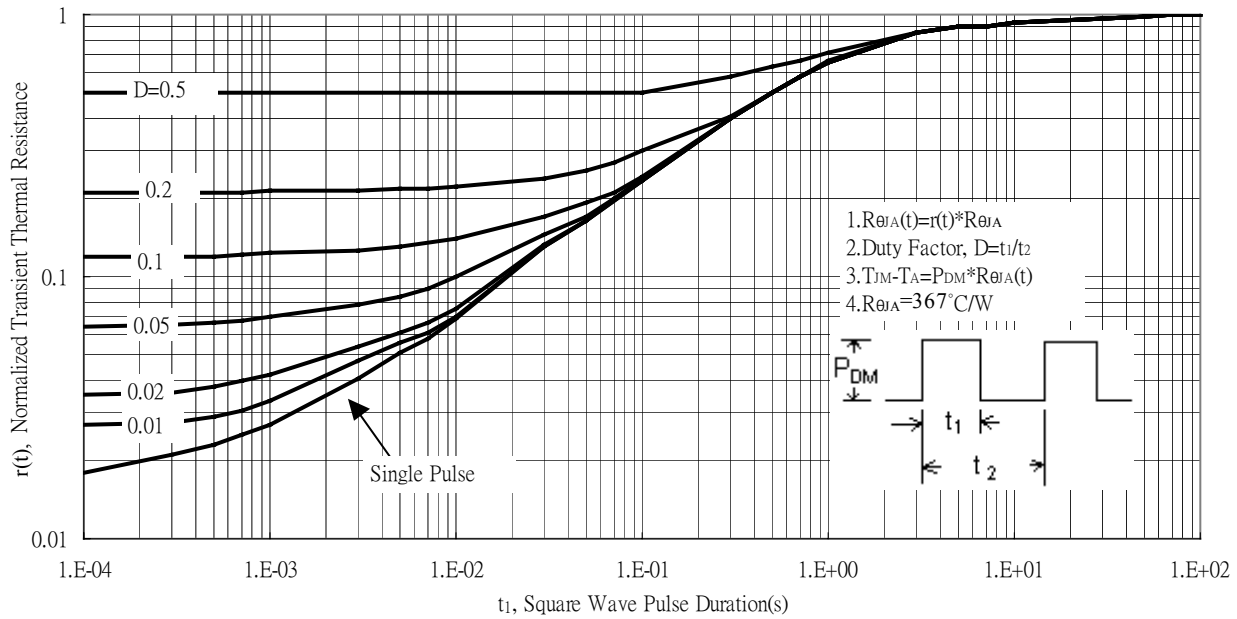
Typical Transfer Characteristics



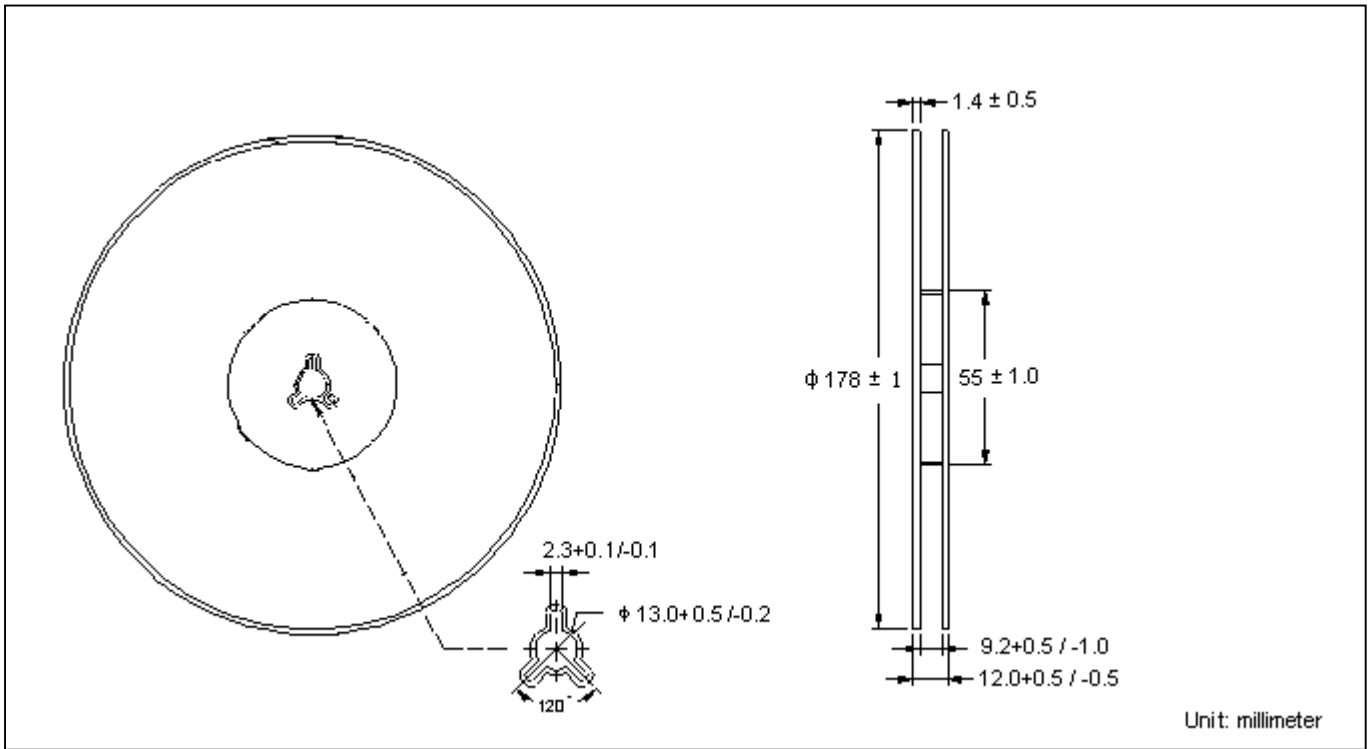
Power Derating Curve



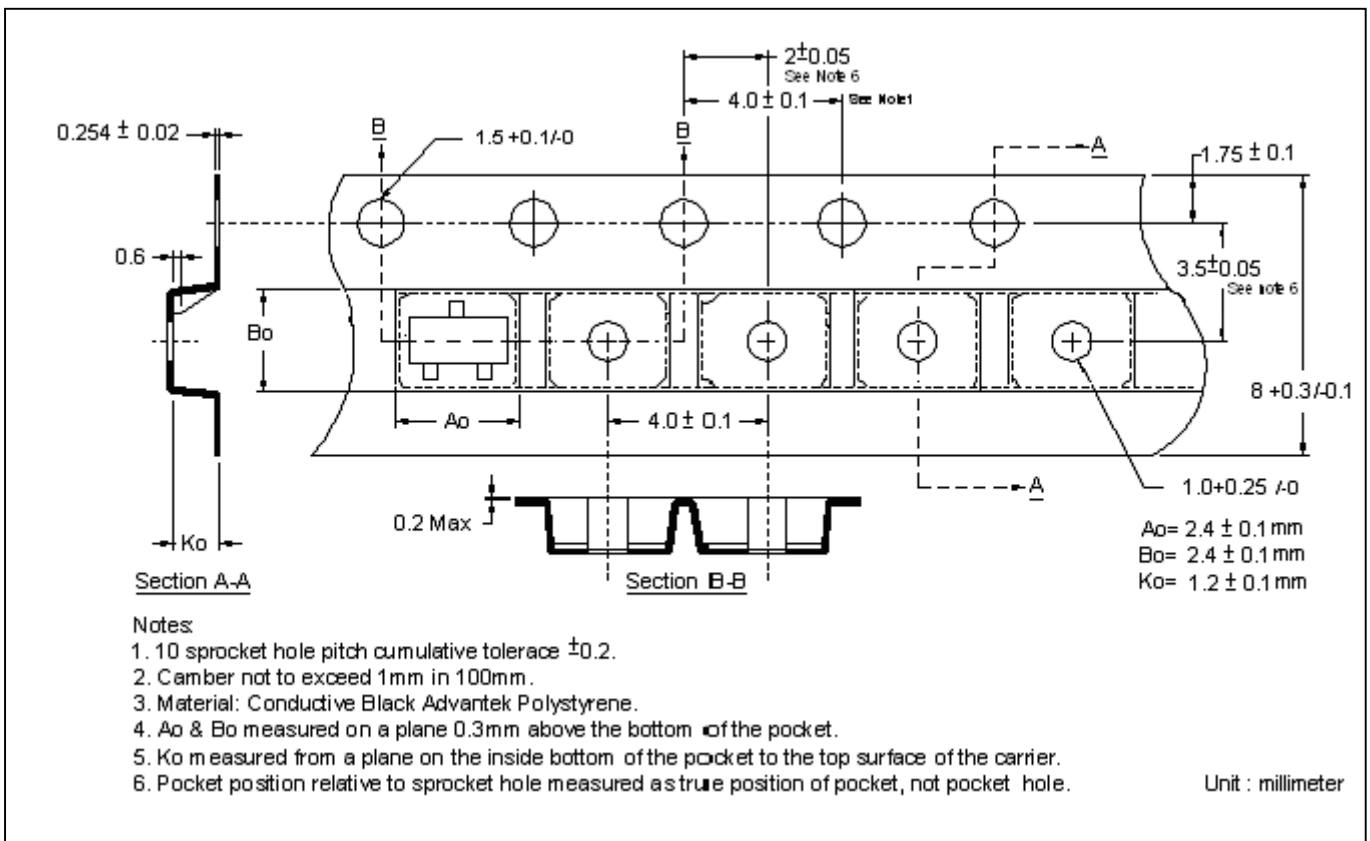
Transient Thermal Response Curves



Reel Dimension



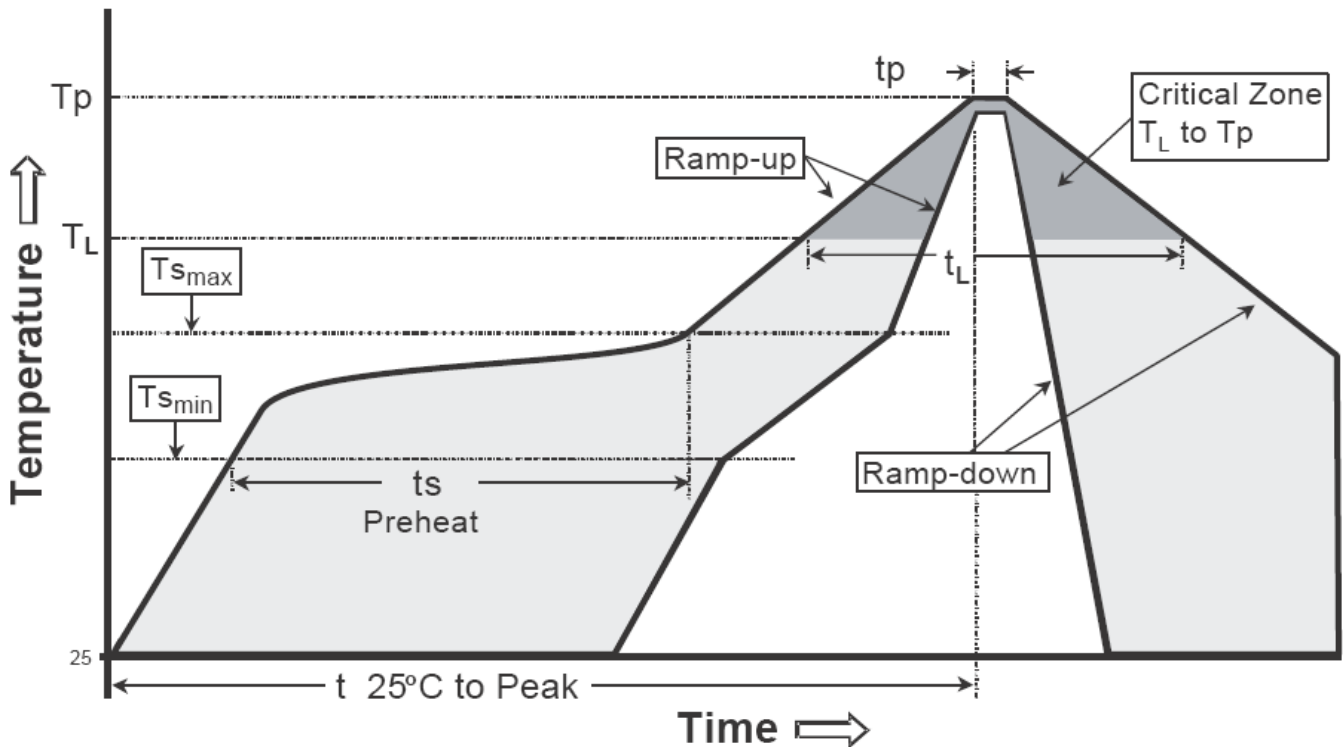
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

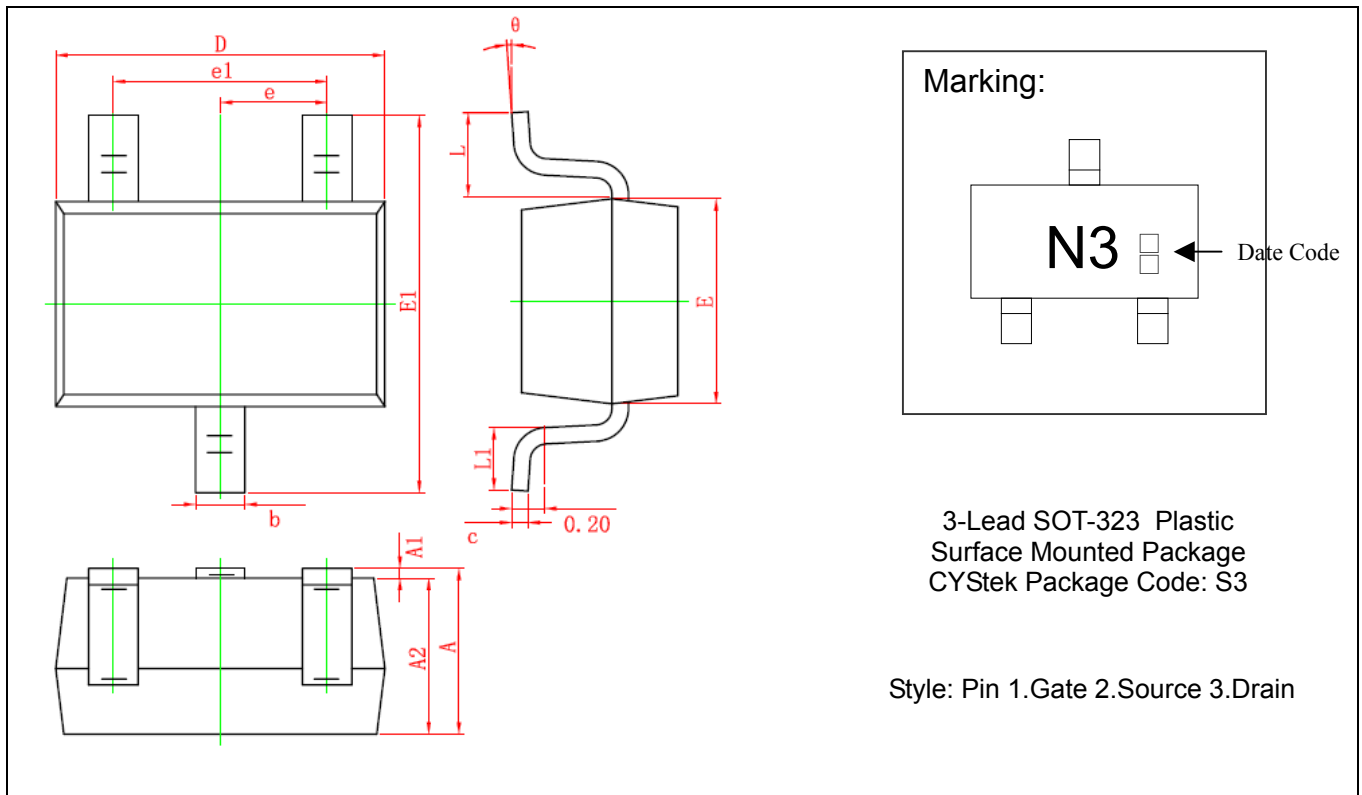
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note :1. All temperatures refer to topside of the package, measured on the package body surface.
 2.For devices mounted on FR-4 PCB of 1.6mm or equivalent grade PCB. If other grade PCB is used, care should be taken to match the coefficients of thermal expansion between components and PCB. If they are not matched well, the solder joints may crack or the bodies of the parts may crack or shatter as the assembly cools.

SOT-323 Dimension



DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043	E1	2.150	2.450	0.085	0.096
A1	0.000	0.100	0.000	0.004	e	0.650	TYP	0.026	TYP
A2	0.900	1.000	0.035	0.039	e1	1.200	1.400	0.047	0.055
b	0.200	0.400	0.008	0.016	L	0.525	REF	0.021	REF
c	0.080	0.150	0.003	0.006	L1	0.260	0.460	0.010	0.018
D	2.000	2.200	0.079	0.087	θ	0°	8°	0°	8°
E	1.150	1.350	0.045	0.053					

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.