For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-integrated.com.

ABSOLUTE MAXIMUM RATINGS

V+ TO GND .....-0.3V, +22V
Oscillator Input to GND (Note 1)
(V- < 12V).....-0.3V, V+ + 0.3V
(V+ > 12V).....V+ - 12.3V, V+ + 0.3V
Power Dissipation (Note 2)
Plastic DIP 300mW
SO 500mW
TO-99 .....500mW
CERDIP 500mW

Operating Temperature Ranges
Commercial (ICL7662C_, Si7661C_).....0°C to +70°C
Extended (ICL7662E__, Si7661D_ or ESA) .....-40°C to +85°C
Military (ICL7662MTV/MJA,
Si7661AA/AK) .....-55°C to +125°C
Storage Temperature.....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: ICL7662

(V_+ = +15V, T_A = +25°C, C_{OSC} = 0, unless otherwise noted. See Test Cuircuit Figure 1.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range-Lo	V+ L	R_L = 10kΩ, LV = GND	-55°C < T_A < +125°C	4.5		11	V
Supply Voltage Range-Hi	V+ H	R_L = 10kΩ, LV = Open	-40°C < T_A <+85°C	9		20	V
			-55°C < T_A < +125°C	9		16.5	V
Supply Current	I+	R_L = ∞, LV = Open	T_A = +25°C		0.25	0.60	mA
			0°C < T_A <+70°C		0.30	0.85	mA
			-55°C < T_A < +125°C		0.40	1.0	mA
Output Source Resistance	R_O	I_O = 20mA, LV = Open	T_A = +25°C		60	100	Ω
			0°C < T_A <+70°C		70	120	Ω
			-55°C < T_A < +125°C		90	150	Ω
Supply Current	I+	V+ = 5V, R_L = ∞, LV = GND	T_A = +25°C		20	150	µA
			0°C < T_A <+70°C		25	200	µA
			-55°C < T_A < +125°C		30	250	µA
Output Source Resistance	R_O	V+ = 5V, I_O = 3mA, LV = GND	T_A = +25°C		125	200	Ω
			0°C < T_A <+70°C		150	250	Ω
			-55°C < T_A < +125°C		200	350	Ω
Oscillator Frequency	f_{OSC}				10		kHz
Power Efficiency	P_{eff}	R_L = 2kΩ	T_A = +25°C	93	96		%
			Min < T_A < Max	90	95		%
Voltage Conversion Efficiency	V_{oEf}	R_L = ∞	Min < T_A < Max	97	99.9		%
Oscillator Sink or Source Current	I_{OSC}	V+ = 5V (V_{OSC} = 0V to +5V)			0.5		µA
		V+ = 15V (V_{OSC} = +5V to +15V)			4.0		µA

Note 1: Connecting any terminal to voltages greater than V+ or less than ground may cause destructive latchup. It is recommended that no input from sources operating from external supplies be applied prior to power-up of the ICL7662.
Note 2: Derate linearly above +50°C by 5.5mW/°C.
Note 3: Pin 1 is a test pin and is not connected in normal use.

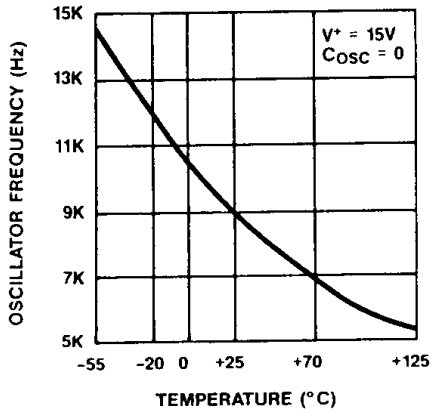
ELECTRICAL CHARACTERISTICS: Si7661

(V_+ = +15V, T_A = +25°C, C_{OSC} = 0, unless otherwise noted. See Test Cuircuit Figure 1.)

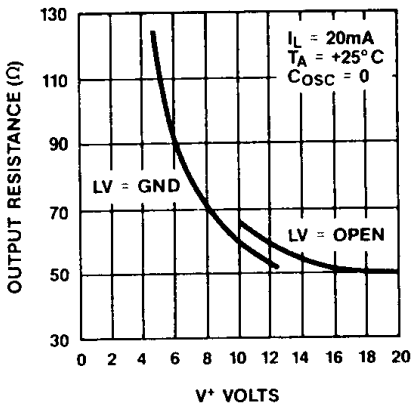
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED: C_{OSC} = 0		LIMITS 1 = 25°C 2 = 125, 85, 70°C 3 = -55, -25, 0°C TEMP	TYP	A, B, C, D, E SUFFIX MIN	MAX	UNITS
INPUT								
Supply Voltage Range (LV)	$V+_{LV}$	R_L = 10kΩ, LV = 0V		1, 2, 3		4.5	9	V
Supply Voltage Range	V+	R_L = 10kΩ, LV = Open	Si7661B, C, D, E	1, 2, 3		8	20	V
			Si7661A	1, 2, 3		8	16.5	V
Supply Current	I+	V+ = 4.5V, R_L = ∞, LV = 0V		1			500	µA
		V+ = 4.5V, R_L = ∞, LV = Open		1			2	mA
OUTPUT								
Output Source Resistance	R_{OUT}	V+ = 4.5V, LV = 0V, I_O = 3mA		1	100			Ω
		V+ = 15V, LV = Open, I_O = 20mA		1, 3	55		100	Ω
				2			120	Ω
Power Conversion Efficiency	PE	V+ = 15V, R_L = 2kΩ		1	92			%
Voltage Conversion Efficiency	$V_{OUT}E$	V+ = 15V, R_L = ∞		1	99.7	97		%
DYNAMIC								
Oscillator Frequency	f_{OSC}	V+ = 15V		1	10			kHz
Oscillator Impedance	Z_{OSC}	V+ = 4.5V, LV = 0V		1	1			MΩ
		V+ = 15V		1	100			kΩ

Typical Operating Characteristics

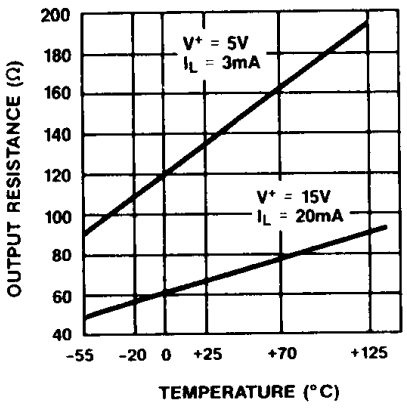
UNLOADED OSCILLATOR FREQUENCY vs. TEMPERATURE



OUTPUT SOURCE RESISTANCE vs. SUPPLY VOLTAGE

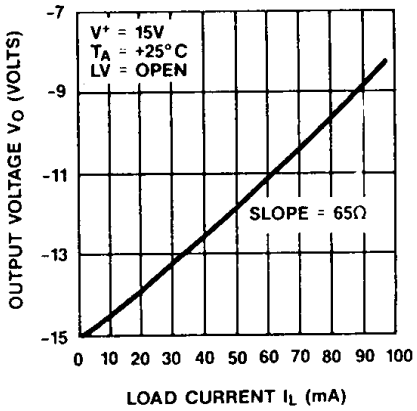


OUTPUT SOURCE RESISTANCE vs. TEMPERATURE

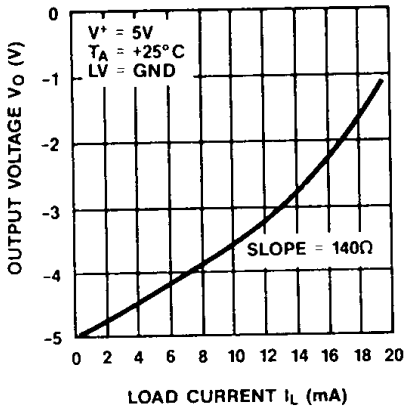


Typical Operating Characteristics (continued)

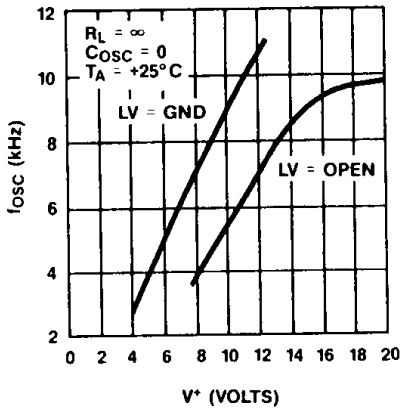
OUTPUT VOLTAGE vs. LOAD CURRENT



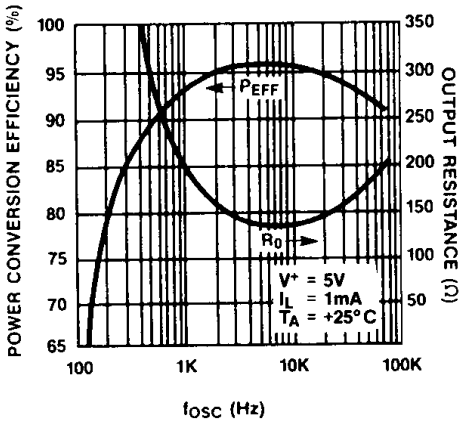
OUTPUT VOLTAGE vs. LOAD CURRENT



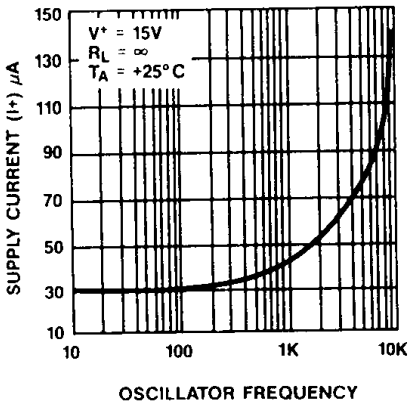
OSCILLATION FREQUENCY vs. SUPPLY VOLTAGE



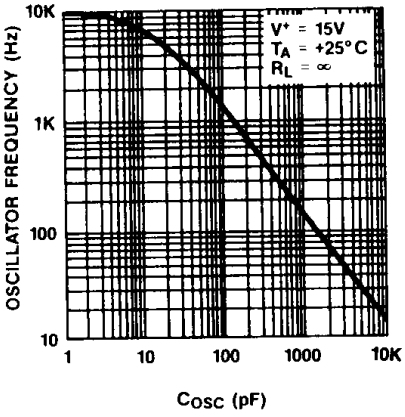
POWER CONVERSION FREQUENCY AND OUTPUT RESISTANCE vs. OSCILLATOR FREQUENCY



SUPPLY CURRENT vs. OSCILLATOR FREQUENCY



OSCILLATION FREQUENCY vs. EXTERNAL OSCILLATOR CAPACITANCE



Detailed Description

All the circuitry necessary to complete a voltage inverter is contained on the ICL7662 (Si7661). Only 2 external capacitors are needed. These may be inexpensive 10µF polarized electrolytic capacitors. Figure 2, an idealized voltage inverter, illustrates the ICL7662 (Si7661) operation. During the first half of the cycle, switches S2 and S4 are open; switches S1 and S3 are closed, and the capacitor C1 is charged to a voltage V_{IN}. During the second half cycle, switches S1 and S3 are opened, and switches S2 and S4 are closed. The capacitor C1 undergoes a negative shift equal to V_{IN}. Assuming ideal switches (R_{ON} = 0) and no load on C2, charge is then transferred from C1 to C2 such that the voltage on C2 is exactly $-V_{IN}$.

The four switches in Figure 2 are MOS power switches. Switch S1 is a P channel switch and switches S2, S3 and S4 are N channel devices.

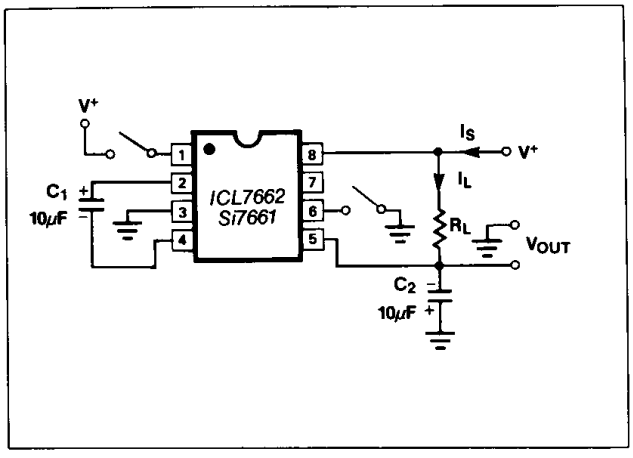


Figure 1. ICL7662/Si7661 Test Circuit

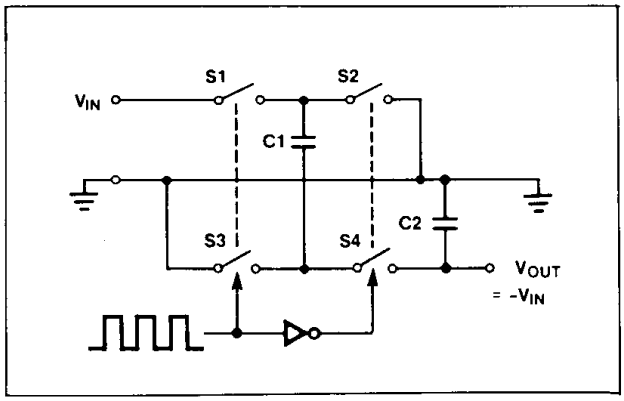


Figure 2. Idealized Negative Voltage Converter

Efficiency Considerations

Theoretically, a voltage multiplier can approach 100% efficiency if certain conditions are met. The ICL7662 (Si7661) approaches the conditions listed below for negative voltage multiplication if large values of C1 and C2 are used.

- The output switches have virtually no offset and extremely low ON resistance.
- Minimal power is consumed by the drive circuitry.
- The impedances of the reservoir and pump capacitors are negligible.

The energy loss per charge pump cycle is:

$$E = \frac{1}{2} \times C1 \times (V_{IN}^2 - V_{OUT}^2)$$

There will be a substantial voltage difference between V_{IN} and V_{OUT} if the impedances of C1 and C2 (at the pump frequency) are high compared to output load R1. To reduce output ripple, make C2 as large in value as is practical. Increasing the value of both C1 and C2 will improve the efficiency.

General Precautions

- The positive terminal of C1 must be connected to Pin 2 of the ICL7662 (Si7661), and the positive terminal of C2 must be connected to Ground.
- Never exceed maximum supply voltages.
- For higher efficiency, connect LV to Ground for supply voltages less than 8 volts.
- V_{OUT} should not be shorted to V^+ for extended periods of time. Transient conditions (including startup) are acceptable.

Applications

Changing Oscillator Frequency

Normally the OSC pin of the ICL7662 (Si7661) is left open, and the 10kHz nominal frequency (5kHz charge pump frequency) is used. The oscillator can be lowered by connecting an external capacitor between OSC and V^+ (see Figure 3). A graph in the Typical Operating Characteristics section shows the nominal frequency versus capacitor value. Lowering the oscillator frequency will improve the conversion efficiency with very low output current values. An undesirable effect of lowering the oscillator frequency is that the impedance level of the pump capacitor will increase. Increasing the value of C1 and C2 will compensate for this effect.

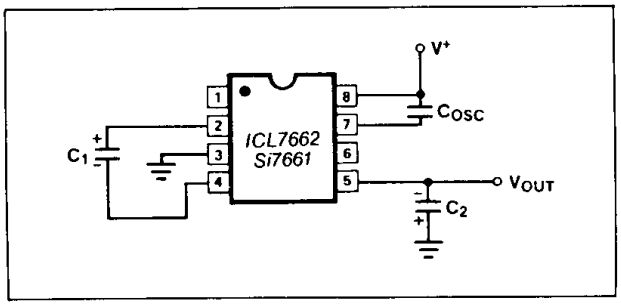


Figure 3. Lowering Oscillator Frequency

In some applications, particularly audio amplifiers, the 5kHz output ripple frequency is objectionable. The oscillator frequency may be increased by one of two methods. The first method is to overdrive the OSC pin with an external oscillator. To eliminate the possibility of latchup, insert a 1kΩ resistor in series with the OSC input (see Figure 4). If the external clock source does not pullup close to V^+, then a 10kΩ pullup resistor is suggested. The pump frequency, and, therefore, the output ripple will be one-half of the external clock frequency. Driving the ICL7662 (Si7661) with a higher frequency clock will slightly increase the supply current, but allows the use of smaller external capacitors and increases the ripple frequency.

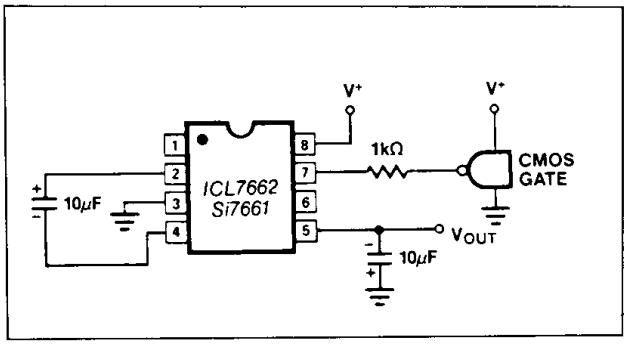


Figure 4. External Clocking

The second method is to tie pin 1 (TEST) to V^+.This disconnects the internal oscillator from the OSC pin. Since there is always a small amount of parasitic capacitance from the OSC pin, tying the TEST pin to V^+ will allow the capacitor to oscillate faster (depending on how much parasitic capacitance there is from the OSC pin).

Cascading Devices

To produce larger negative voltage multiplication of the initial supply voltage, the ICL7662 (Si7661) may be cascaded as shown in Figure 5. The resulting output resistance is approximately equal to the weighted sum of the individual ICL7662 (Si7661) R_{OUT} values. For light loads, the practical limit is 10 devices. The output voltage is defined by $V_{OUT} = -n \times V^+$ (where n is an integer representing the number of cascaded devices).

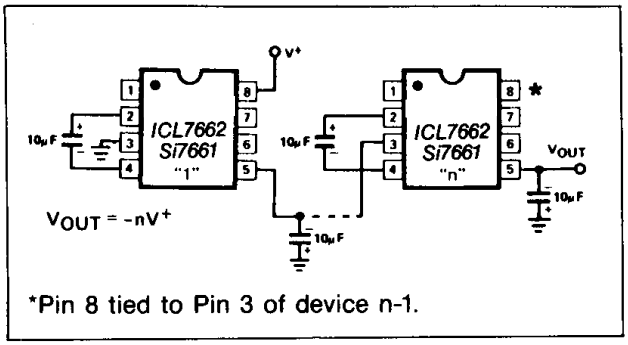


Figure 5. Cascading ICL7662s for Increased Output Voltage

Negative Voltage Converter

The most common application of the ICL7662 (Si7661) is as a charge pump voltage inverter, converting a positive voltage to the corresponding negative equivalent. The simple circuit of Figure 6 shows that only two external components (C1 and C2) are needed. In most applications C1 and C2 are low cost 10µF electrolytic capacitors. The ICL7662 (Si7661) is NOT a voltage regulator, and the output source resistance is approximately 60Ω with a +15V supply. This means that with an input voltage of +15V, the output voltage will be -15V, under light loads (less than 1mA load current), but will decrease to -14.4V with a 10mA load current. The output source impedance of the complete circuit is the sum of the ICL7662 (Si7661) output resistance and the impedance of the pump capacitor at the pump frequency.

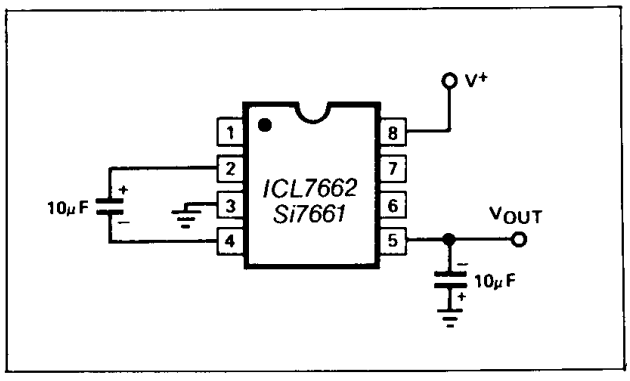


Figure 6. Negative Voltage Converter

The output ripple of the voltage inverter can be calculated by noting that the output current is supplied solely by the reservoir capacitor during one-half of the charge pump cycle. This introduces an output ripple of:

$$V_{RIPPLE} = \frac{1}{2} \times I_{OUT} \times (1/F_{PUMP}) \times (1/C2)$$

For the nominal F_{PUMP} of 5kHz (one-half of the nominal 10kHz oscillator frequency) and a 10µF C2, the output ripple will be approximately 10mV with a load current of 10mA.

Positive Voltage Doubler

The ICL7662 (Si7661) can double a positive voltage as shown in Figure 7. It basically uses the ICL7662 (Si7661) as a power inverter. The only drawback from this circuit is the inevitable voltage drop across the two diodes.

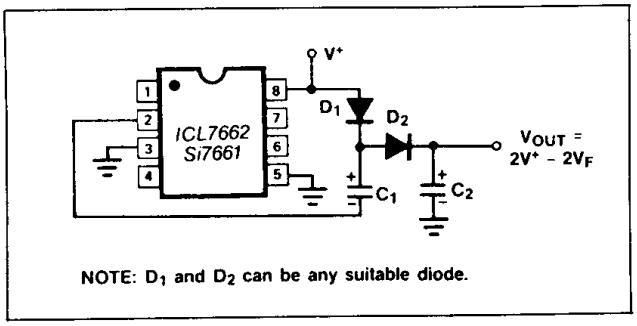


Figure 7. Positive Voltage Doubler

Paralleling Devices

Paralleling ICL7662s (or Si7661s) reduces the output resistance. As illustrated in Figure 8, each device requires its own pump capacitor C1; however, the reservoir capacitor C2 serves all devices. The equation for calculating output resistance is also shown in Figure 8.

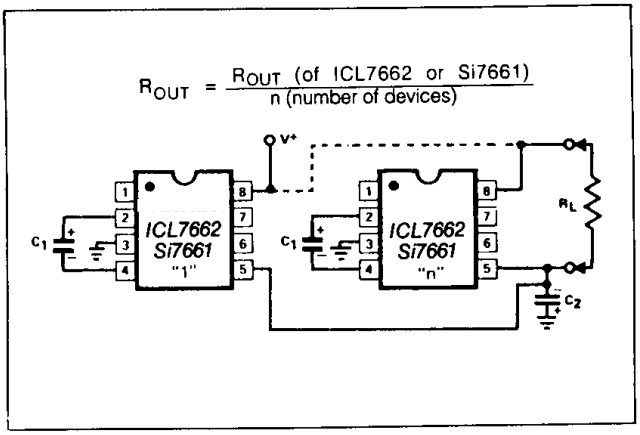


Figure 8. Paralleling ICL7662s to Reduce Output Resistance

Combining Positive Supply Multiplication and Negative Voltage Conversion

This dual function is illustrated in Figure 9. In this circuit, capacitors C1 and C3 perform the pump and reservoir functions respectively for the generation of the negative voltage. Capacitors C2 (pump capacitor) and C4 (reservoir capacitor) are used for the positive voltage converter. The circuit configuration, however, does lead to a higher source impedance of the generated supplies. This is due to the finite impedance of the common charge pump driver.

Voltage Splitting

The ICL7662 (Si7661) can also be used to split a power supply or battery. In Figure 10 the ICL7662 (Si7661) has the positive terminal of the power supply connected to V^+ and the negative terminal connected to V_{OUT}. The midpoint of the power supply is found on Pin 3. The output resistance is much lower than in other applications, and higher currents can be drawn from this configuration.

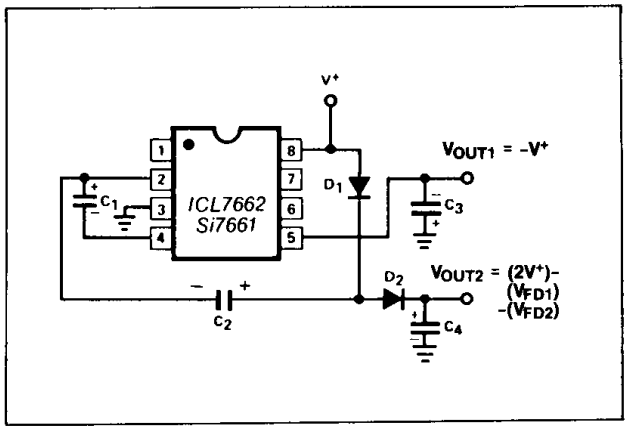


Figure 9. Combined Positive Multiplier and Negative Converter

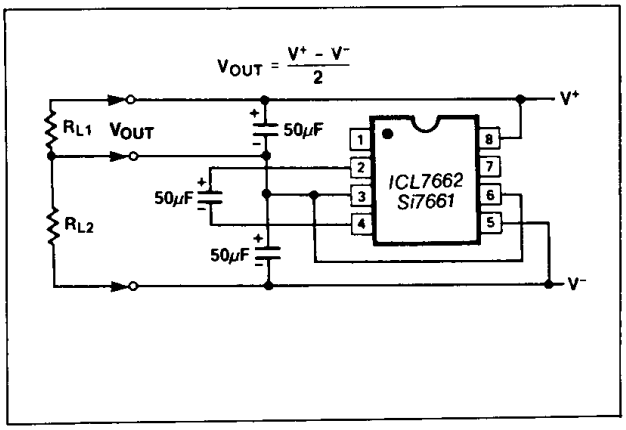
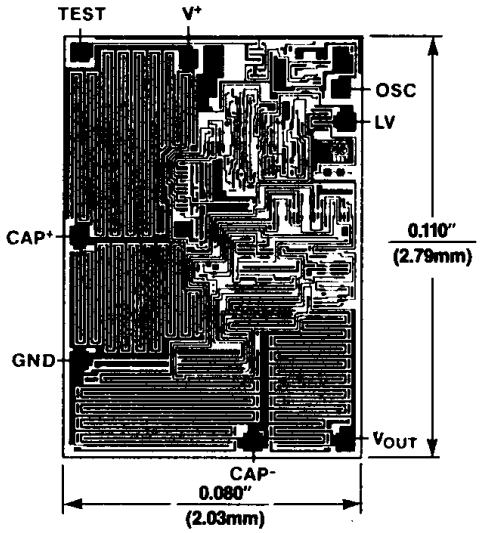


Figure 10. Splitting a Supply in Half

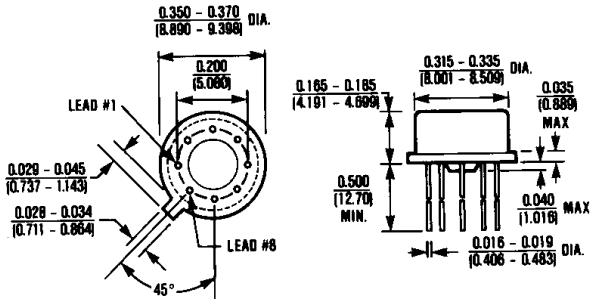
Chip Topography



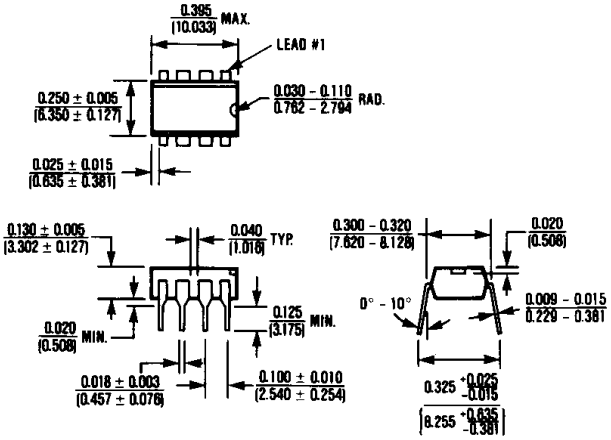
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
Si7661CJ	0°C to +70°C	8 Plastic DIP
Si7661CY	0°C to +70°C	14 SO
Si7661CSA	0°C to +70°C	8 SO
Si7661C/D	0°C to +70°C	Dice
Si7661DJ	-40°C to +85°C	8 Plastic DIP
Si7661DY	-40°C to +85°C	14 SO
Si7661ESA	-40°C to +85°C	8 SO
Si7661AA-4	-55°C to +125°C	8 TO-99
Si7661AK	-55°C to +125°C	8 CERDIP

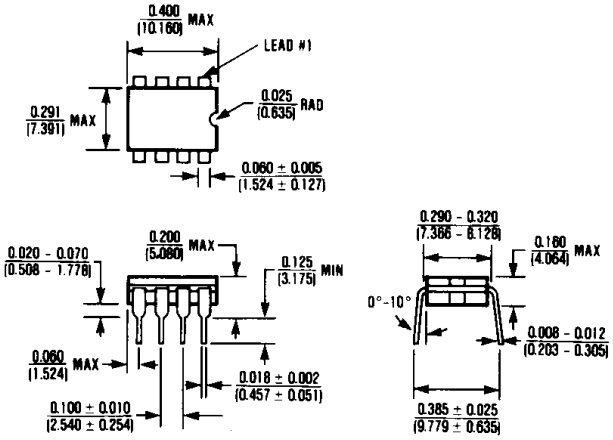
Package Information



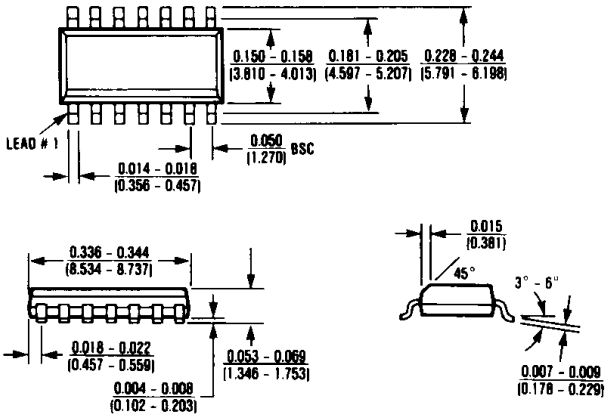
8 Lead TO-99 (TV)
θ_{JA} = 150°C/W
θ_{JC} = 45°C/W



8 Lead Plastic DIP (PA)
θ_{JA} = 160°C/W
θ_{JC} = 75°C/W



8 Lead CERDIP (JA)
θ_{JA} = 125°C/W
θ_{JC} = 55°C/W



14 Lead Small Outline (SD)
θ_{JA} = 115°C/W
θ_{JC} = 60°C/W

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