



August 2014

# FCH077N65F

## N-Channel SuperFET<sup>®</sup> II FRFET<sup>®</sup> MOSFET

650 V, 54 A, 77 mΩ

### Features

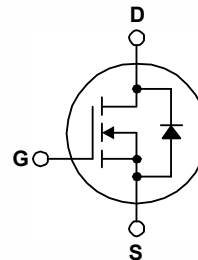
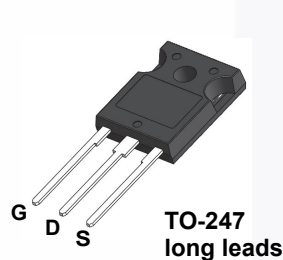
- 700 V @ T<sub>J</sub> = 150°C
- Typ. R<sub>DS(on)</sub> = 68 mΩ
- Ultra Low Gate Charge (Typ. Q<sub>g</sub> = 126 nC)
- Low Effective Output Capacitance (Typ. C<sub>oss(eff.)</sub> = 693 pF)
- 100% Avalanche Tested
- RoHS Compliant

### Applications

- LCD / LED / PDP TV
- Telecom / Server Power Supplies
- Solar Inverter
- AC - DC Power Supply

### Description

SuperFET<sup>®</sup> II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SuperFET II FRFET<sup>®</sup> MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.



### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	FCH077N65F_F155	Unit
V <sub>DSS</sub>	Drain to Source Voltage	650	V
V <sub>GSS</sub>	Gate to Source Voltage	- DC	±20
		- AC (f > 1 Hz)	±30
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 25°C)	54
		- Continuous (T <sub>C</sub> = 100°C)	32
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	162	A
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	1128	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	11	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	4.81	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C)	481	W
		- Derate Above 25°C	3.85
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	°C

### Thermal Characteristics

Symbol	Parameter	FCH077N65F_F155	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction to Case, Max.	0.26	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient, Max.	40	

FCH077N65F — N-Channel SuperFET<sup>®</sup> II FRFET<sup>®</sup> MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH077N65F_F155	FCH077N65F	TO-247 G03	Tube	N/A	N/A	30 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 25^\circ\text{C}$	650	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}, T_J = 150^\circ\text{C}$	700	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1\text{ mA}, \text{Referenced to } 25^\circ\text{C}$	-	0.79	-	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_C = 125^\circ\text{C}$	-	144	-	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 5.4\text{ mA}$	3	-	5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 27\text{ A}$	-	68	77	$\text{m}\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\text{ V}, I_D = 27\text{ A}$	-	42	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	5345	7109	pF
$C_{oss}$	Output Capacitance		-	165	220	pF
$C_{riss}$	Reverse Transfer Capacitance		-	0.8	-	pF
$C_{oss}$	Output Capacitance	$V_{DS} = 380\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	97	-	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	693	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 380\text{ V}, I_D = 27\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	126	164	nC
$Q_{gs}$	Gate to Source Gate Charge		-	28	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		-	53	-	nC
ESR	Equivalent Series Resistance	$f = 1\text{ MHz}$	-	0.7	-	$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 380\text{ V}, I_D = 27\text{ A}, V_{GS} = 10\text{ V}, R_g = 4.7\ \Omega$ (Note 4)	-	40	90	ns
$t_r$	Turn-On Rise Time		-	35	80	ns
$t_{d(off)}$	Turn-Off Delay Time		-	113	236	ns
$t_f$	Turn-Off Fall Time		-	5	20	ns

### Drain-Source Diode Characteristics

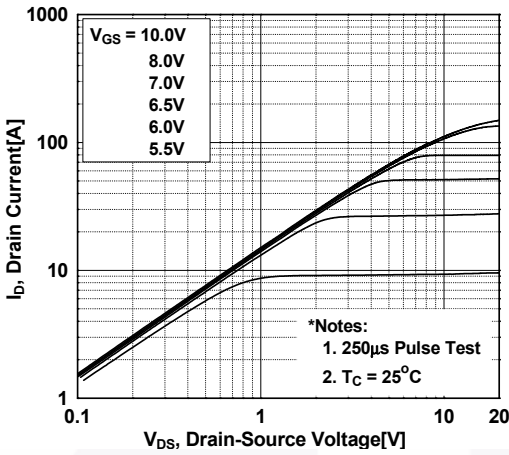
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	54	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	162	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 27\text{ A}$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 27\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}$	-	163	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt = 100\text{ A}/\mu\text{s}$	-	0.9	-	$\mu\text{C}$

#### Notes:

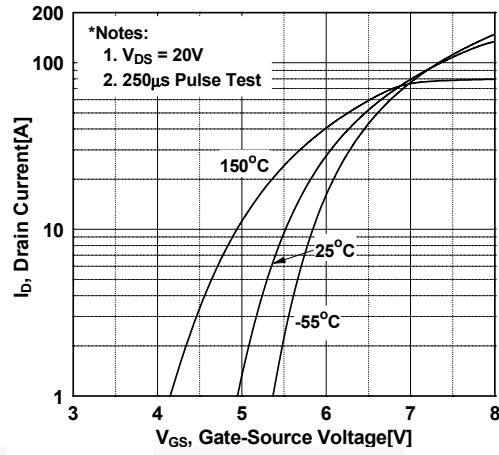
1. Repetitive rating: pulse width limited by maximum junction temperature.
2.  $I_{AS} = 11\text{ A}, R_G = 25\ \Omega, \text{Starting } T_J = 25^\circ\text{C}.$
3.  $I_{SD} \leq 27\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq 380\text{ V}, \text{Starting } T_J = 25^\circ\text{C}.$
4. Essentially independent of operating temperature.

## Typical Performance Characteristics

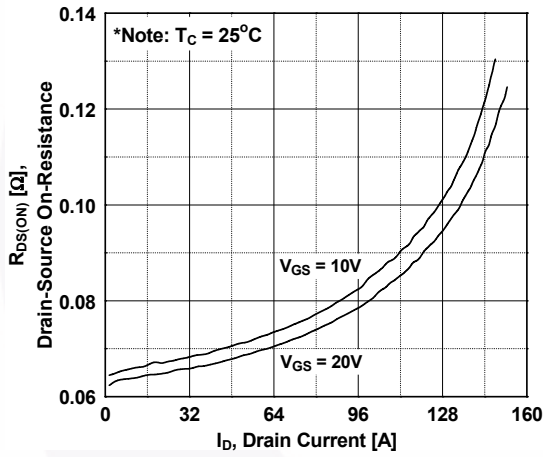
**Figure 1. On-Region Characteristics**



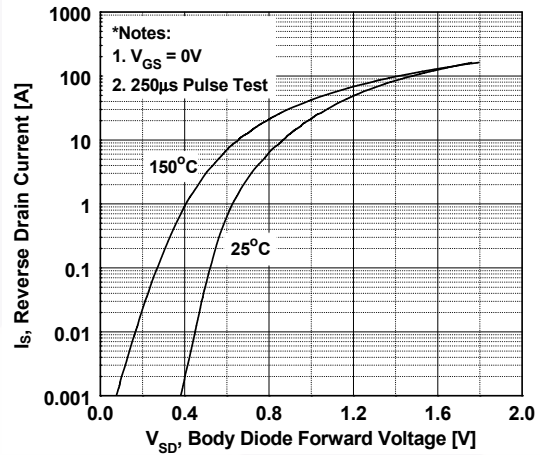
**Figure 2. Transfer Characteristics**



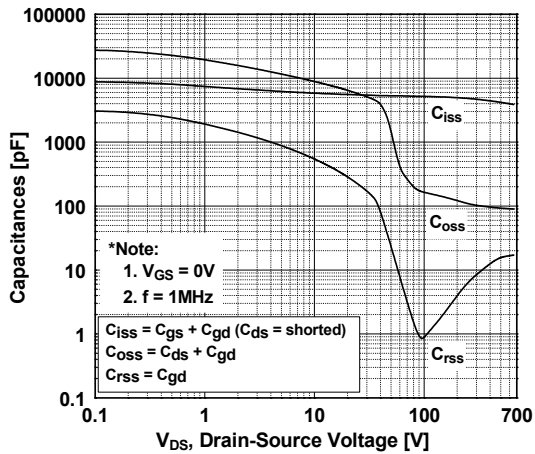
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



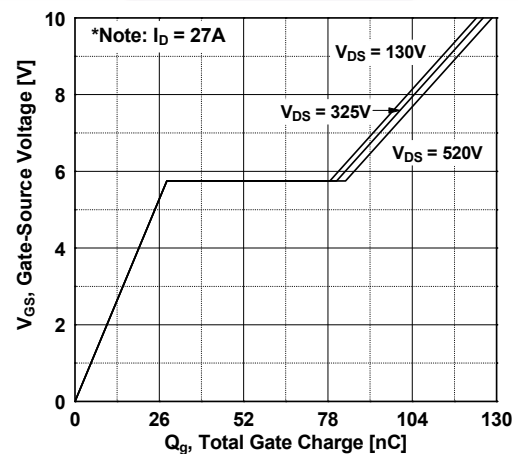
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

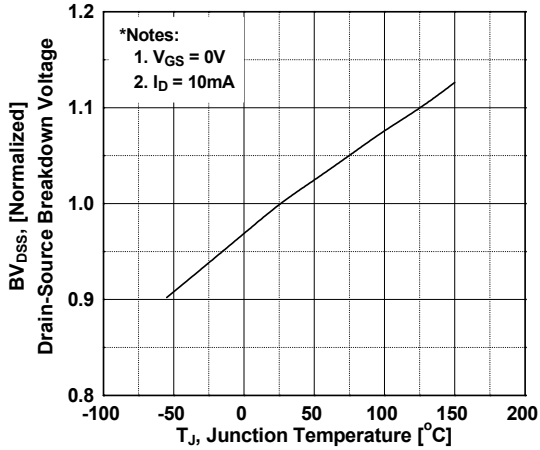


**Figure 6. Gate Charge Characteristics**

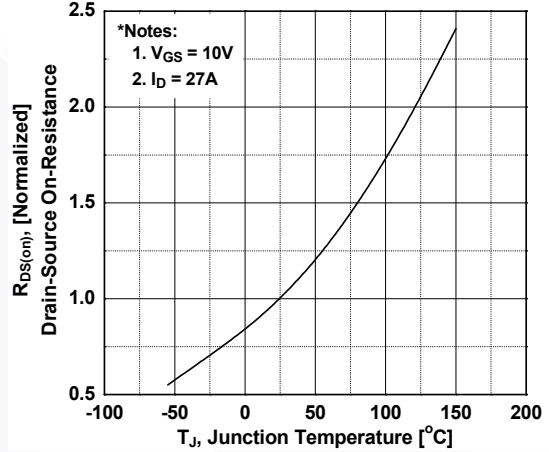


**Typical Performance Characteristics** (Continued)

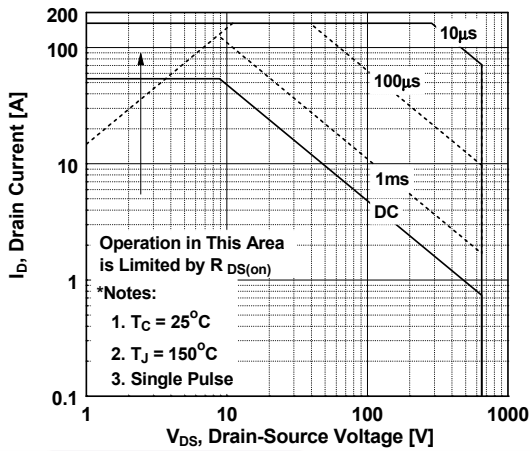
**Figure 7. Breakdown Voltage Variation vs. Temperature**



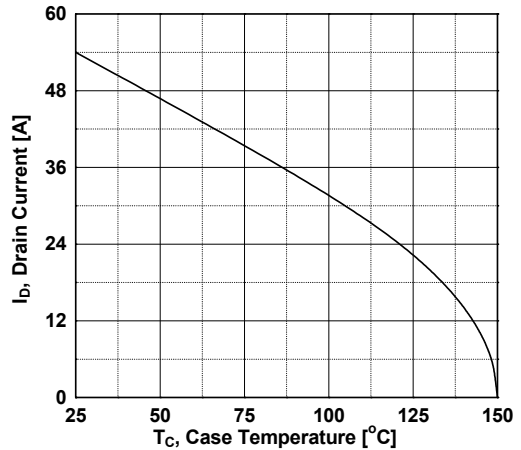
**Figure 8. On-Resistance Variation vs. Temperature**



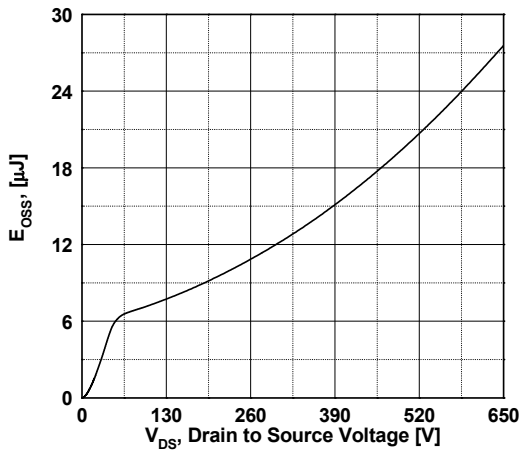
**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**

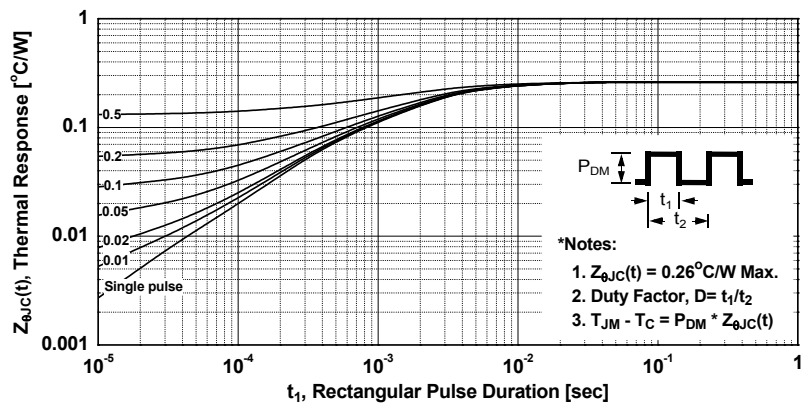


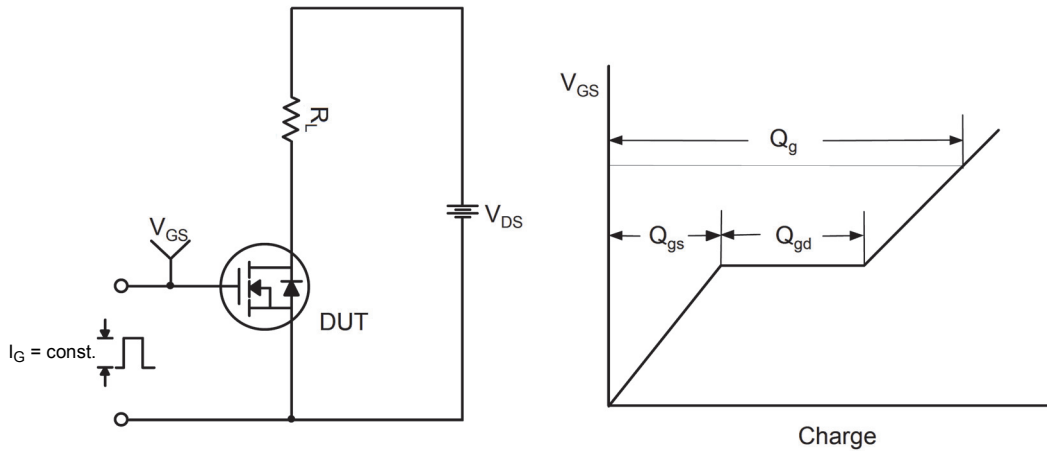
**Figure 11. E\_oss vs. Drain to Source Voltage**



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve





**Figure 13. Gate Charge Test Circuit & Waveform**



**Figure 14. Resistive Switching Test Circuit & Waveforms**

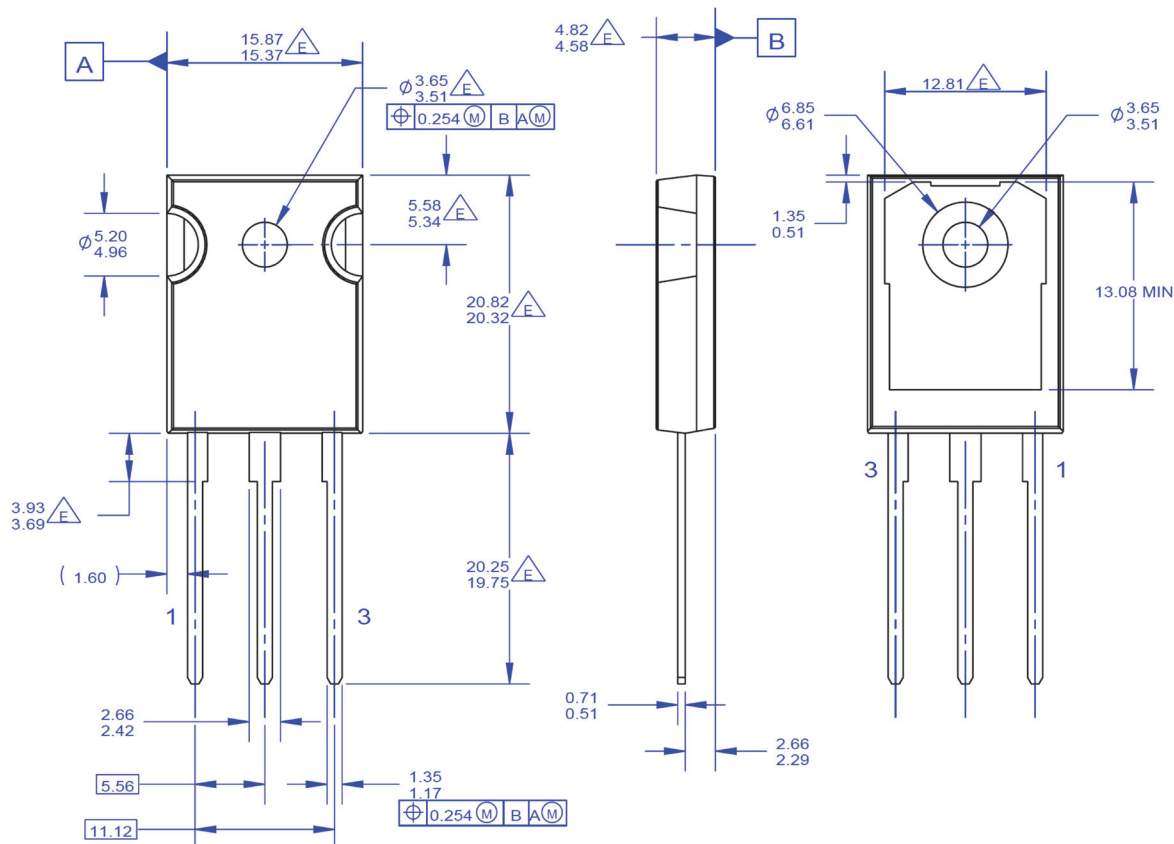


**Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms**



Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. PACKAGE REFERENCE: JEDEC TO-247, ISSUE E, VARIATION AB, DATED JUNE, 2004.
- B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DRAWING CONFORMS TO ASME Y14.5 - 1994

**E** DOES NOT COMPLY JEDEC STANDARD VALUE  
**F**. DRAWING FILENAME: MKT-TO247G03\_REV01

**Figure 17. TO-247, Molded, 3-Lead, Jedec AB Long Leads**

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| Build it Now™  | GreenBridge™                                    | QFET®                                 | TinyCalc™        |
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| FETBench™  | OPTOLOGIC®                                      | Sync-Lock™                            | ? ? ™            |
| FPS™   | OPTOPLANAR®                                     |                                       |                  |

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