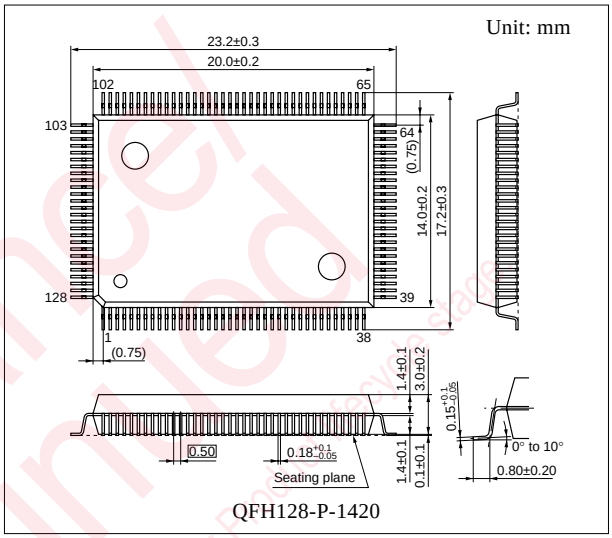
AN2127FHS

Analog signal processor SUPER ONE CHIP IC for CCD camera

■ Overview

The AN2127FHS is SUPER ONE CHIP IC of signal processing circuits for a CCD camera. It incorporates luminance signal processing, color signal processing and encoder, plus Y/C mix., 75 Ω driver and sub carrier generation circuit. In addition, it incorporates an auto white balance control circuit, AGC ope-amp., adjustment DAC and EEPROM auto read circuit at power on, thereby it allows you to constitute a microcomputer system by just mounting EEPROM.



QFH128-P-1420

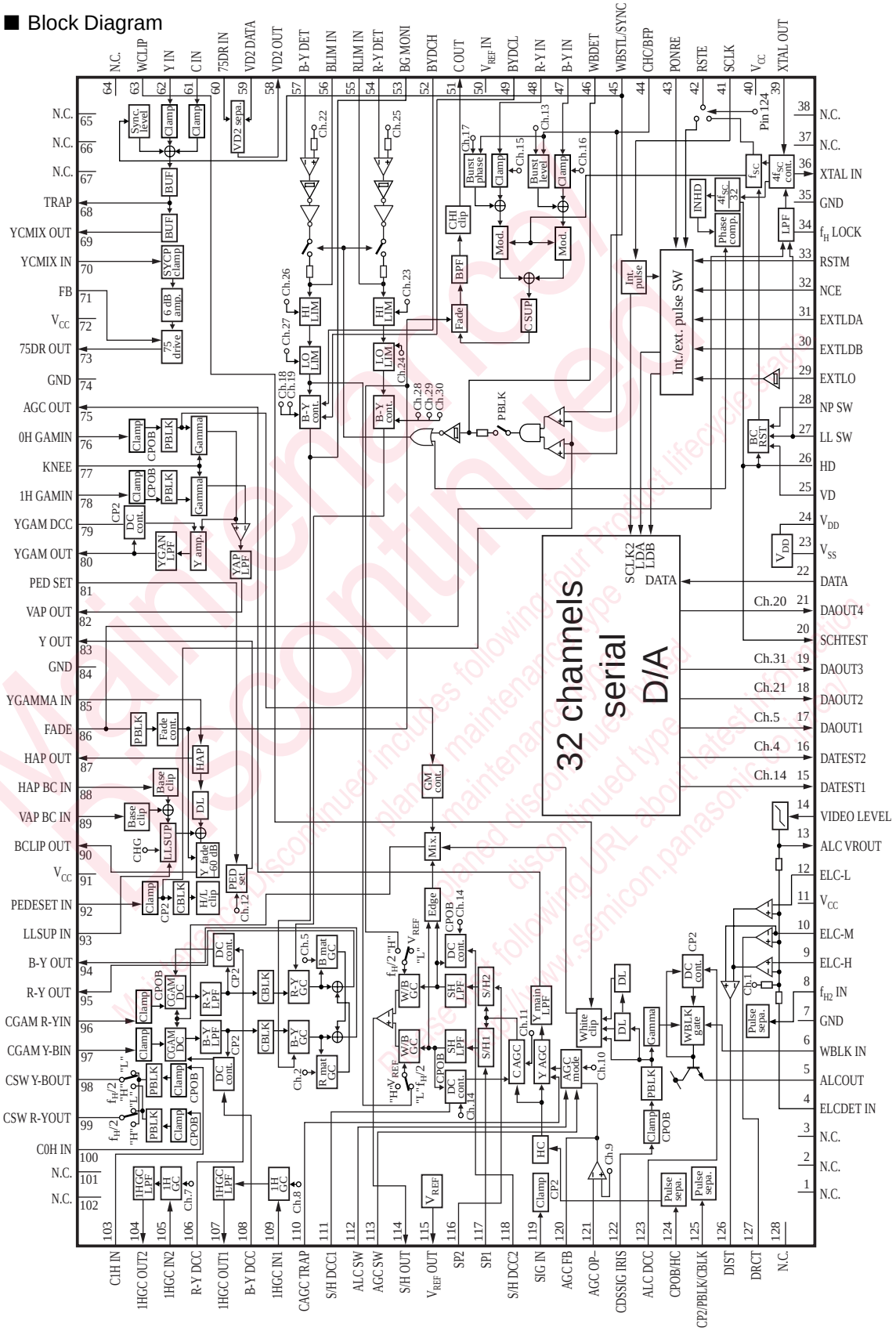
■ Features

- Applicable for 768 H CCD
- Usable commonly for NTSC and PAL
- Built in FH lock system (sub carrier generation circuit)
- Built in automatic EEPROM read circuit at power on
- Built in adjustment DAC (8 bits, 32 channels)
- Built in a circuit for external synchronization
- Built in electronic iris comparator

■ Applications

- A full range of CCD cameras such as surveillance camera, board camera, video camera, television telephone, television conference system, PC input camera

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	N.C.	38	N.C.
2	N.C.	39	XTAL OUT
3	N.C.	40	V_{CC}
4	ELCDET IN	41	SCLK
5	ALCOUT	42	RSTE
6	WBLK IN	43	PONRE
7	GND	44	CHC/BFP
8	f_{H2} IN	45	WBSTL/SYNC
9	ELC-H	46	WBDET
10	ELC-M	47	B-Y IN
11	V_{CC}	48	R-Y IN
12	ELC-L	49	BYDCL
13	ALC VROUT	50	V_{REF} IN
14	VIDEO LEVEL	51	C OUT
15	DATEST1	52	BYDCH
16	DATEST2	53	BG MONI
17	DAOUT1	54	R-Y DET
18	DAOUT2	55	RLIM IN
19	DAOUT3	56	BLIM IN
20	SCHTEST	57	B-Y DET
21	DAOUT4	58	VD2 OUT
22	DATA	59	VD2 DATA
23	V_{SS}	60	75DR IN
24	V_{DD}	61	C IN
25	VD	62	Y IN
26	HD	63	WCLIP
27	LL SW	64	N.C.
28	NP SW	65	N.C.
29	EXTLO	66	N.C.
30	EXTLDB	67	N.C.
31	EXTLDA	68	TRAP
32	NCE	69	YCMIX OUT
33	RSTM	70	YCMIX IN
34	f_H LOCK	71	FB
35	GND	72	V_{CC}
36	XTAL IN	73	75DR OUT
37	N.C.	74	GND

■ Pin Descriptions (continued)

Pin No.	Description	Pin No.	Description
75	AGC OUT	102	N.C.
76	0H GAMIN	103	C1H IN
77	KNEE	104	1HGC OUT2
78	1H GAMIN	105	1HGC IN2
79	YGAM DCC	106	R-Y DCC
80	YGAM OUT	107	1HGC OUT1
81	PED SET	108	B-Y DCC
82	VAP OUT	109	1HGC IN1
83	Y OUT	110	CAGC TRAP
84	GND	111	S/H DCC1
85	YGAMMA IN	112	ALC SW
86	FADE	113	AGC SW
87	HAP OUT	114	S/H OUT
88	HAP BC IN	115	V_{REF} OUT
89	VAP BC IN	116	SP2
90	BCLIP OUT	117	SP1
91	V_{CC}	118	S/H DCC 2
92	PEDESET IN	119	SIG IN
93	LLSUP IN	120	AGC FB
94	B-Y OUT	121	AGC OP–
95	R-Y OUT	122	CDSSIG IRIS
96	CGAM R-YIN	123	ALC DCC
97	CGAM Y-BIN	124	CPOB/HC
98	CSW Y-BOUT	125	CP2/PBLK/CBLK
99	CSW R-YOUT	126	DIST
100	C0H IN	127	DRCT
101	N.C.	128	N.C.

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	5.5	V
Supply current	I_{CC}	170	mA
Power dissipation *2	P_D	876	mW
Operating ambient temperature *1	T_{opr}	–20 to +75	°C
Storage temperature *1	T_{stg}	–55 to +150	°C

Note) 1. *1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
*2: The power dissipation shown is for the IC package in free air at T_a = 75°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC}	4.5 to 5.1	V

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Circuit current	I_{TOT}	V_{CC} = 4.8 V	90	120	150	mA
Reference voltage 1	V_{REF}	V_{CC} = 4.8 V	1.66	1.76	1.86	V
Reference voltage 2	V_{DD}	V_{CC} = 4.8 V	3.21	3.38	3.55	V
YAGC maximum gain	G_{YAX}	V_{119} = 10-step, 20 mV[p-p]	20	24	28	dB
CAGC maximum gain	G_{CAX}	V_{119} = 10-step, 20 mV[p-p]	20	24	28	dB
AGC minimum gain 1	G_{YAN1}	V_{119} = 10-step, 1 200 mV[p-p]	–8.5	–6.5	–4.5	dB
AGC minimum gain 2	G_{YAN2}	V_{119} = 10-step, 1 200 mV[p-p]	–4.5	–2.5	– 0.5	dB
WB characteristics 1	V_{SH2}	V_{119} = sin 500 kHz, 500 mV[p-p]	–470	–400	–330	mV[p-p]
WB characteristics 2	G_{SH6}	V_{119} = sin 500 kHz, 500 mV[p-p]	–2	0	2	dB
S/H characteristics	V_{SH9}	V_{119} = square wave 500 kHz, 1 V[p-p]	700	800	900	mV[p-p]
Iris GC characteristics	V_{TR2}	V_{122} = 10-step, 1 200 mV[p-p] V_6 = GND	1 100	1 300	1 500	mV[p-p]
Iris gate step	V_{WG}	V_{122} = C-GND	–20	0	20	mV[p-p]
Iris gamma 1	V_{IG1}	V_{122} = 10-step, 1 500 mV[p-p]	800	900	1 000	mV[p-p]
Iris gamma 2	G_{IG2}	V_{122} = 10-step, 1 500 mV[p-p]	0.5	1.7	2.9	dB
Iris gamma 3	G_{IG3}	V_{122} = 10-step, 1 500 mV[p-p]	0.5	—	—	dB
Iris BLK step	V_{WB}	V_{122} = C-GND	–20	0	20	mV[p-p]
Delay signal amp. gain 1	G_{IH2}	V_{105} = sin 500 kHz, 500 mV[p-p]	6.5	8.0	—	dB
Delay signal amp. gain 2	G_{IH5}	V_{109} = sin 500 kHz, 500 mV[p-p]	6.5	8.0	—	dB
Luminance gamma characteristics 1	V_{YG1}	V_{76} = 10-step, 700 mV[p-p]	450	550	650	mV[p-p]
Luminance gamma characteristics 2	G_{YG2}	V_{76} = 10-step, 700 mV[p-p]	–13	–11	–9	dB
Luminance gamma characteristics 3	G_{YG3}	V_{76} = 10-step, 1 500 mV[p-p]	1.5	3.5	5.5	dB
Luminance gamma BLK step	V_{YGB}	V_{76} = C-GND	–20	0	20	mV[p-p]
V aperture gain	V_{VA1}	V_{78} = sin 500 kHz, 300 mV[p-p]	–1 250	–1 050	–850	mV[p-p]
V aperture BLK step	V_{VAB}	V_{76} = V_{78} = C-GND	–20	0	20	mV[p-p]
H aperture gain	V_{HA1}	V_{92} = sin 6 MHz, 200 mV[p-p]	1 000	1 200	1 400	mV[p-p]
H aperture base clip	V_{HB1}	V_{88} = sin 500 kHz, 100 mV[p-p]	90	130	160	mV[p-p]
V aperture base clip	V_{VB1}	V_{89} = sin 500 kHz, 100 mV[p-p]	90	130	160	mV[p-p]
Luminance output amp. gain	G_{Y1}	V_{92} = 10-step, 600 mV[p-p]	– 0.5	1.0	2.5	dB
Luminance high clip level	V_{YH}	V_{92} = 10-step, 1 V[p-p]	700	840	980	mV[p-p]
Luminance low clip level	V_{YL}	V_{92} = 10-step, –200 mV[p-p]	–50	–30	–10	mV[p-p]
Synchronizing signal output level 2	V_{SYN2}	V_{62} = C-GND	260	300	340	mV[p-p]

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pedestal control characteristics 1	V_{YP1}	V_{92} = C-GND	60	90	120	mV[p-p]
Pedestal control characteristics 2	V_{YP2}	V_{92} = C-GND	–30	–15	0	mV[p-p]
Luminance fade characteristics	G_{YFB}	V_{85} = 10-step, 600 mV[p-p]	—	–40	–26	dB
CSW (R-Y) gain	G_{CS1}	V_{100} = V_{103} = 10-step, 600 mV[p-p]	–1.5	0	1.5	dB
CSW (B-Y) gain	G_{CS2}	V_{100} = V_{103} = 10-step, 600 mV[p-p]	–1.5	0	1.5	dB
CSW (R-Y) BLK step	V_{CSB1}	V_{100} = V_{103} = C-GND	–20	0	20	mV[p-p]
CSW (B-Y) BLK step	V_{CSB2}	V_{100} = V_{103} = C-GND	–20	0	20	mV[p-p]
CSW (R-Y) f_{H2} step	V_{CSF1}	V_{100} = V_{103} = C-GND	–20	0	20	mV[p-p]
CSW (B-Y) f_{H2} step	V_{CSF2}	V_{100} = V_{103} = C-GND	–20	0	20	mV[p-p]
Color difference gamma characteristics 1	V_{CG1}	V_{76} = 10-step, 700 mV[p-p] V_{96} = 10-step, 350 mV[p-p]	10	80	F0	HEX
Color difference gamma characteristics 2	G_{CG2}	V_{76} = 10-step, 700 mV[p-p] V_{96} = 10-step, 350 mV[p-p]	–13	–10.5	–8	dB
Color difference gamma characteristics 3	G_{CG3}	V_{76} = 10-step, 1 500 mV[p-p] V_{96} = 10-step, 750 mV[p-p]	2.0	3.5	5.0	dB
Color difference gamma characteristics 4	V_{CG4}	V_{76} = 10-step, 700 mV[p-p] V_{96} = 10-step, 350 mV[p-p]	10	80	F0	HEX
Color difference gamma characteristics 5	G_{CG5}	V_{76} = 10-step, 700 mV[p-p] V_{96} = 10-step, 350 mV[p-p]	–13	–10.5	–8	dB
Color difference gamma characteristics 6	G_{CG6}	V_{76} = 10-step, 1 500 mV[p-p] V_{96} = 10-step, 750 mV[p-p]	2.0	3.5	5.0	dB
R-Y gain characteristics	G_{CL1}	V_{96} = sin 500 kHz, 200 mV[p-p]	6.5	10.0	13.5	dB
B-Y gain characteristics	G_{CL3}	V_{97} = sin 500 kHz, 200 mV[p-p]	6.5	10.0	13.5	dB
B-Y matrix characteristics	V_{CM1I}	V_{97} = 10-step, 300 mV[p-p]	–160	–100	–40	mV[p-p]
R-Y matrix characteristics	V_{CM2I}	V_{96} = 10-step, 300 mV[p-p]	40	100	160	mV[p-p]
R-Y BLK step	V_{CB1}	V_{100} = V_{103} = C-GND	–20	0	20	mV[p-p]
B-Y BLK step	V_{CB2}	V_{100} = V_{103} = C-GND	–20	0	20	mV[p-p]
Burst level	V_{BU1}	V_{48} = white 200 mV[p-p], V_{47} = C-GND	253	300	347	mV[p-p]
Chroma output amplitude R	G_{CR1}	V_{48} = white 200 mV[p-p], V_{47} = C-GND	6	8	10	dB
Chroma output amplitude B	G_{CR3}	V_{48} = C-GND ,V_{47} = white 200 mV[p-p]	1	3	5	dB
Chroma high cut characteristics	G_{CH}	V_{48} = white 400 mV[p-p], V_{47} = C-GND	680	760	840	mV[p-p]
Chroma fade characteristics	G_{CF}	V_{48} = white 200 mV[p-p], V_{47} = C-GND	—	–40	–20	dB
High luminance chroma suppress	G_{CS}	V_{48} = V_{92} = white 500 mV[p-p] V_{47} = C-GND	—	–40	–18	dB
FH high-level lock range	f_{FH3}	HD+1 Hz	0.75	—	—	Hz
FH low-level lock range	f_{FH2}	HD–1 Hz	—	—	– 0.75	Hz
VXO free-run oscillation frequency	f_{FR}	V_{27} = V_{CC} , V_{124} = GND	3.579425	3.579545	3.579665	MHz
75 Ω driver gain	G_{DR}	V_{62} = 10-step, 700 mV[p-p]	–1.5	0	1.5	dB
Luminance main LPF characteristics	G_{YM}	V_{119} = V_{76} = sin 7.15 MHz, 500 mV[p-p]	–42	–30	–12	dB

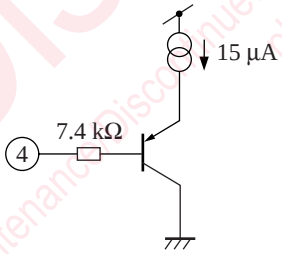
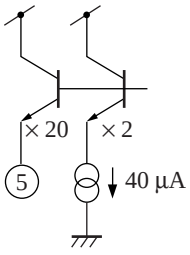
■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data

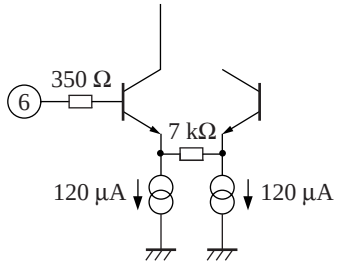
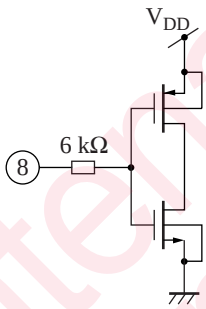
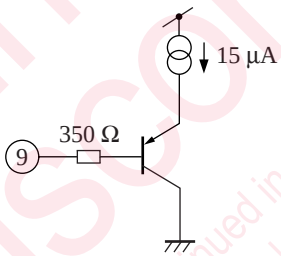
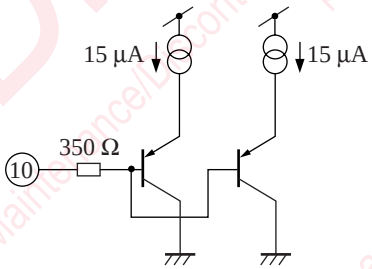
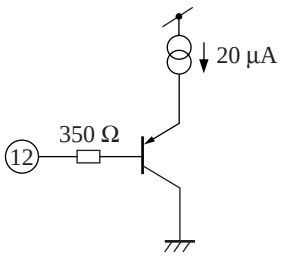
Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pulse separation CPOB	V_{CPOB}	V_{CC} = 4.8 V	3.3	3.6	3.9	V
Pulse separation PBLK	V_{PBLK}	V_{CC} = 4.8 V	1.55	1.8	2.05	V
Pulse separation CP2	V_{CP2}	V_{CC} = 4.8 V	3.6	3.9	4.2	V
Pulse separation CBLK	V_{CBLK}	V_{CC} = 4.8 V	0.6	0.8	1.0	V
Pulse separation f_H /2	V_{FH2}	V_{CC} = 4.8 V	1.15	1.4	1.65	V
Pulse separation sync.	V_{SYNC}	V_{CC} = 4.8 V	0.8	1.0	1.2	V
Pulse separation BFP	V_{BFP}	V_{CC} = 4.8 V	3.35	3.65	3.95	V
Pulse separation SP1	V_{SP1}	V_{CC} = 4.8 V	0.8	1.0	1.2	V
Pulse separation SP2	V_{SP2}	V_{CC} = 4.8 V	0.8	1.0	1.2	V
Pulse separation VD2	V_{VD2}	V_{CC} = 4.8 V	0.8	1.0	1.2	V
Comparator threshold 1	V_{CP1}	V_{CC} = 4.8 V	1.55	1.8	2.05	V
Comparator threshold 2	V_{CP2}	V_{CC} = 4.8 V	2.05	2.3	2.65	V
FH lock detection DC	V_{FHDC}	V_{CC} = 4.8 V	1.9	2.0	2.1	V

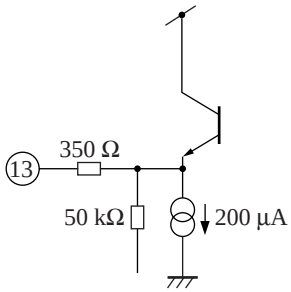
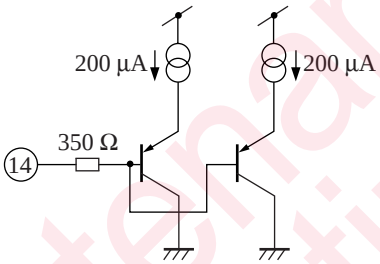
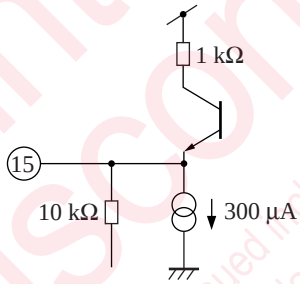
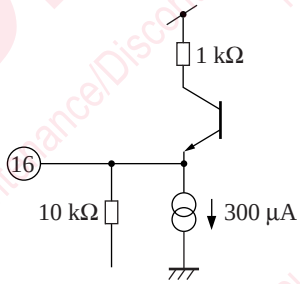
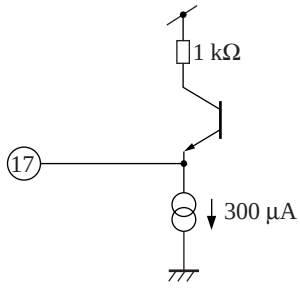
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description
1	—	N.C.
2	—	N.C.
3	—	N.C.
4		ELCDET IN: Comparator detection signal input for ELC
5		ALCOUT: Output for iris detection

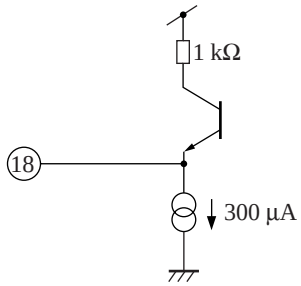
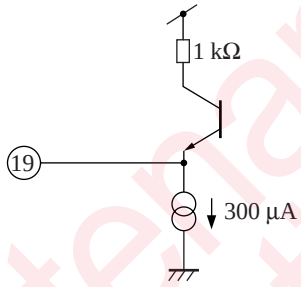
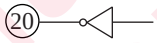
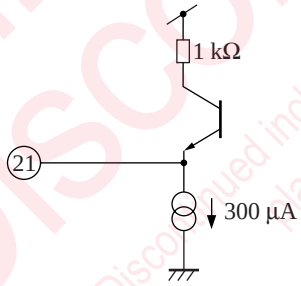
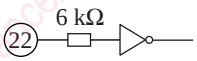
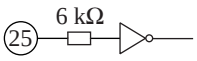
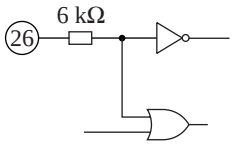
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
6		WBLK IN: Iris signal gate pulse input
7	—	GND: GND for signal processing-system
8		f_{H2} IN: Coincident pulse input for color difference
9		ELC-H: Comparator high threshold for ELC
10		ELC-M: Comparator midium threshold for ELC
11	—	V_{CC} : V_{CC} for signal processing-system
12		ELC-L: Comparator low threshold for ELC

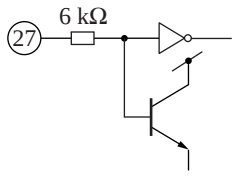
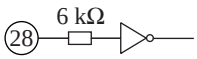
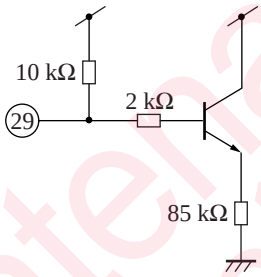
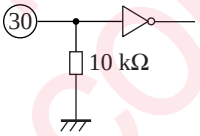
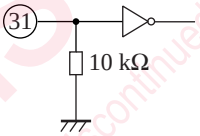
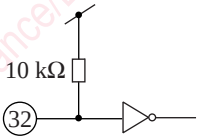
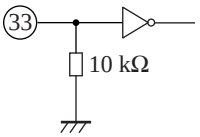
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
13		ALC VROUT: Output for appending dead band to video level.
14		VIDEO LEVEL: VIDEO LEVEL setting DC input
15		DATEST1: Monitor for internal DAC ch.14 output and other channel output DC Ground pin 124 for a test mode
16		DATEST2: Monitor for the internal DAC ch.4 output
17		DAOUT1: External DAC ch.5 output

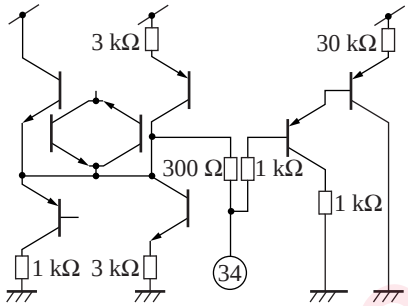
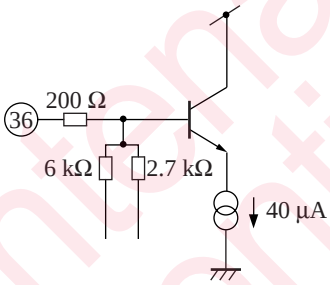
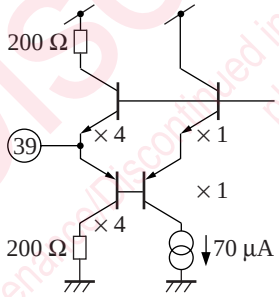
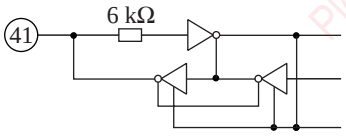
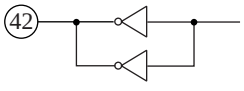
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
18		DAOUT2: External DAC ch.21 output
19		DAOUT3: External DAC ch.31 output
20		SCHTEST: SCH mode monitor
21		DAOUT4: Monitor for external DAC ch.20 output and other channel output DC Ground pin 124 for a test mode
22		DATA: DAC data input
23	—	V_{SS} : Logic-block GND
24	—	V_{DD} : Logic-block power source monitor: approx. 3.5 V
25		VD: Vertical synchronizing pulse input
26		HD: Horizontal synchronizing pulse input

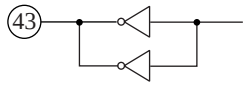
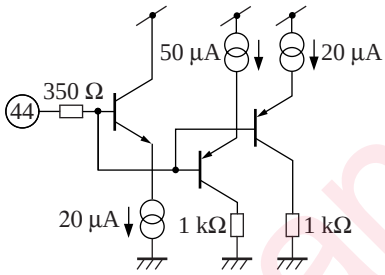
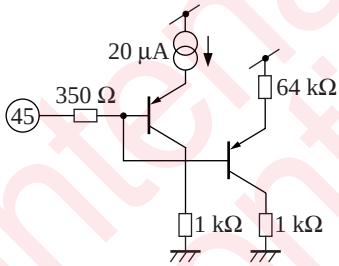
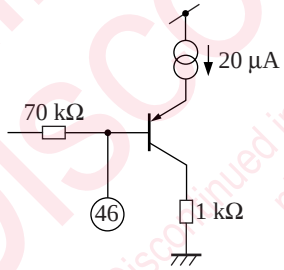
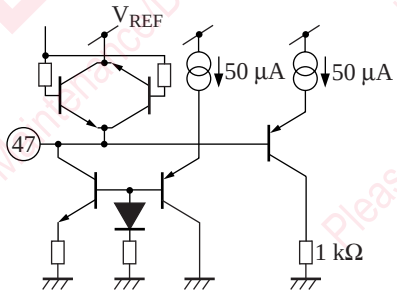
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
27		LL SW: LL/int. setting High: LL mode Low: int. mode
28		NP SW: NTSC/PAL setting
29		EXTLO: Power on lead setting High: DAC fluctuation disabled Low: DAC fluctuation enabled
30		EXTLDB: DAC load pulse input 2 Ch.17 to ch.32 are allocated.
31		EXTLDA: DAC load pulse input 1 Ch.1 to ch.16 are allocated.
32		NCE: CE control input for EEPROM
33		RSTM: RST control input for EEPROM

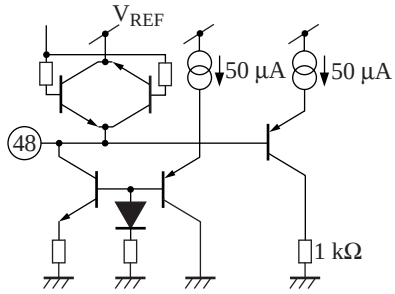
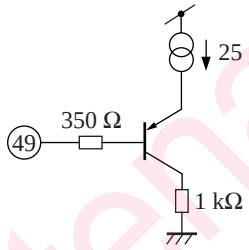
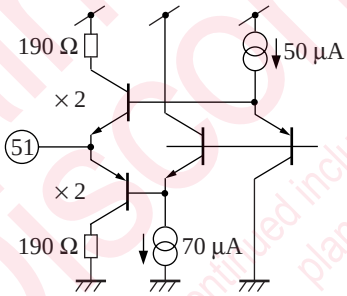
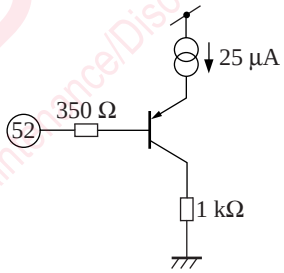
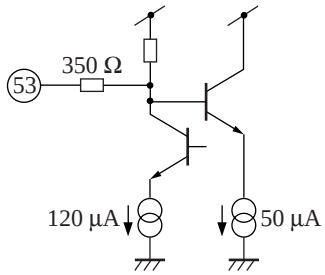
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
34		f_H LOCK: Int. mode error pulse detection output: approx. 2 V_{DC}
35	—	GND: XTAL: encoder-system GND
36		XTAL IN: $4f_{SC}$ input
37	—	N.C.
38	—	N.C.
39		XTAL OUT: $4f_{SC}$ output
40	—	V_{CC} : XTAL: encoder-system V_{CC}
41		SCLK: DAC CLK input/output: CLK input at adjustment CLK output at reading EEPROM data
42		RSTE: RST output for EEPROM

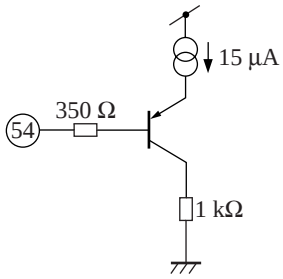
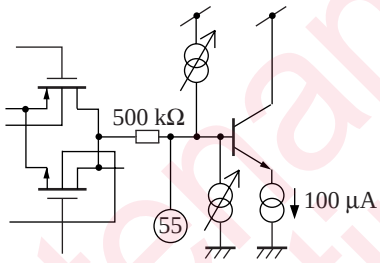
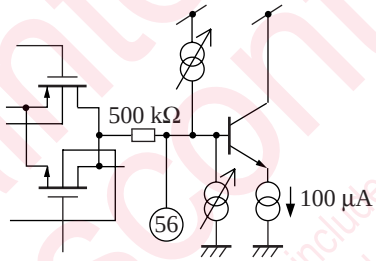
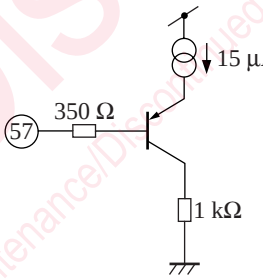
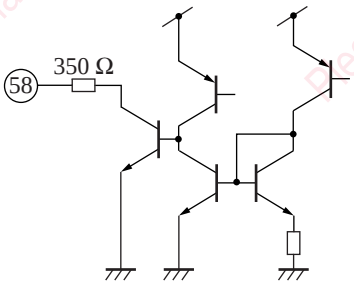
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
43		PONRE: CE output for EEPROM
44		CHC/BFP: Chroma high cut setting/BFP input, jointly used for high luminance threshold in variable setting of WB speed
45		WBSTL/SYNC: Low luminance threshold in variable setting of WB speed Sync. pulse input
46		WBDET: WB variable switch detection output
47		B-Y IN: B-Y signal encoder input

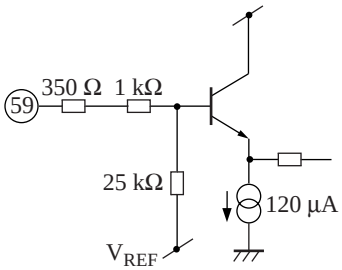
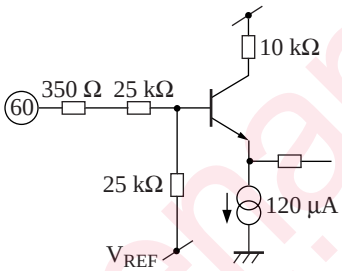
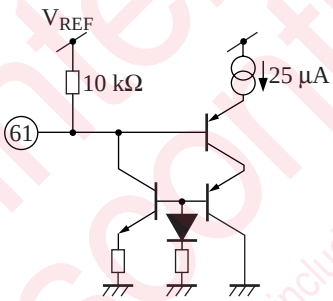
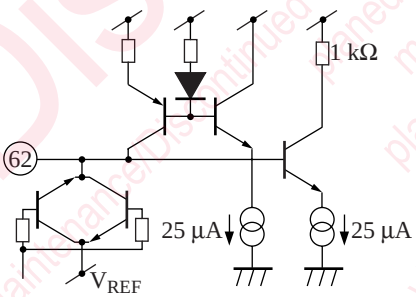
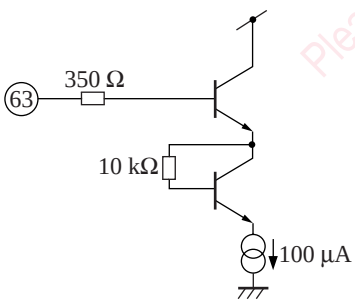
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
48		R-Y IN: R-Y signal encoder input
49		BYDCL: Low color temperature tilt setting for B-Y color regeneration curve
50	—	V_{REF} IN: V_{REF} (pin 115) input
51		C OUT: Encoder chroma output
52		BYDCH: High color temperature tilt setting for B-Y color regeneration curve
53		BG MONI: B-Y color regeneration curve monitor

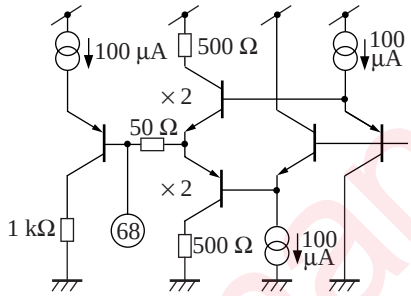
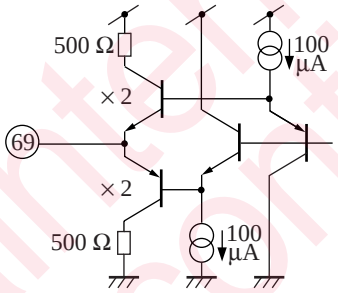
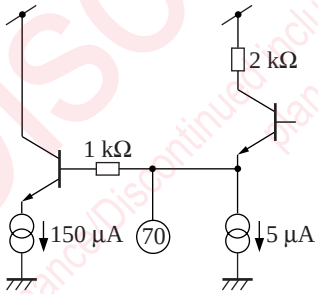
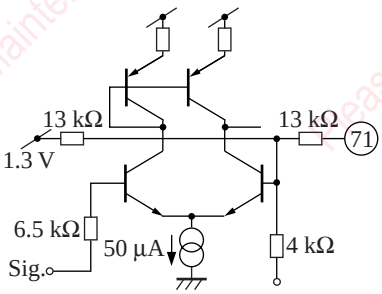
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
54		R-Y DET: R-Y comparator input for WB
55		RLIM IN: RWBDC detection
56		BLIM IN: BWBDC detection
57		B-Y DET: B-Y comparator input for WB
58		VD2 OUT: VD2 pulse separation output

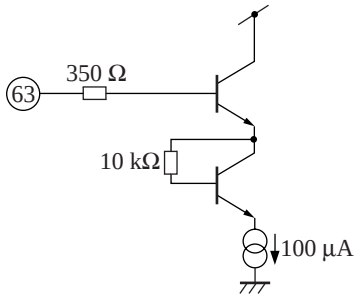
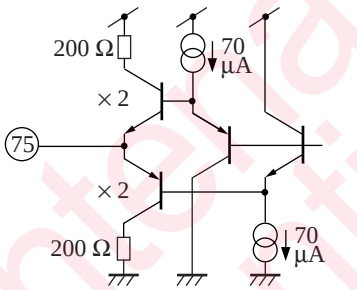
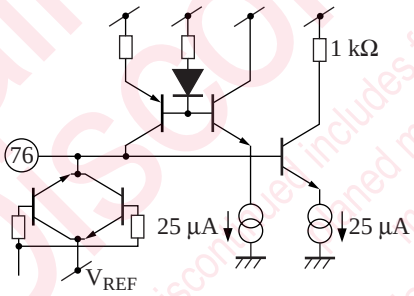
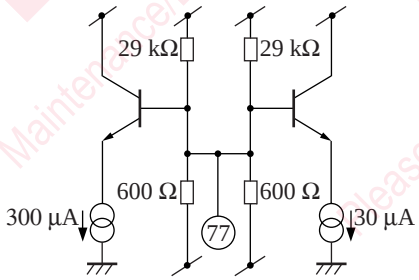
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
59		VD2 DATA: Video signal +VD2 input
60		75DR IN: Video signal input before 75 Ω termination
61		C IN: Chroma signal input For Y/C mix.
62		Y IN: Luminance signal input For Y/C mix.
63		WCLIP: Color difference high brightness clip setting

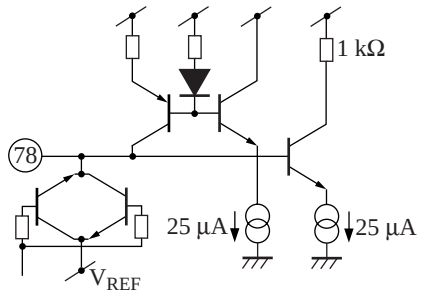
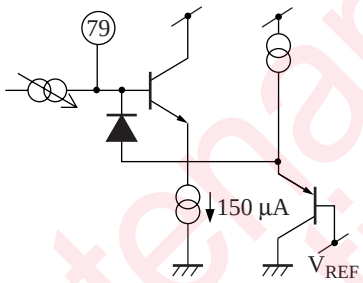
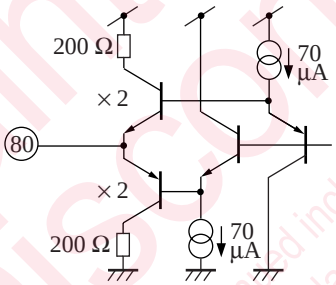
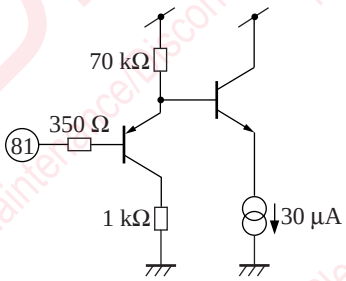
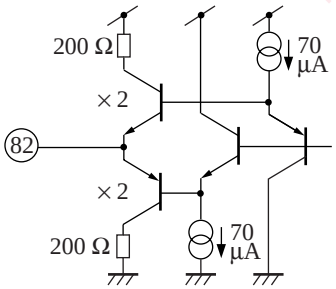
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
64	—	N.C.
65	—	N.C.
66	—	N.C.
67	—	N.C.
68		TRAP: Y/C mix. signal unnecessary frequency characteristics elimination setting
69		YCMIX OUT: Y/C mix. output
70		YCMIX IN: Y/C mix. signal driver input sync. chip clamp
71		FB: FB input for V sag correction
72	—	V_{CC} : V_{CC} for Y/C mix., driver, color regeneration circuit

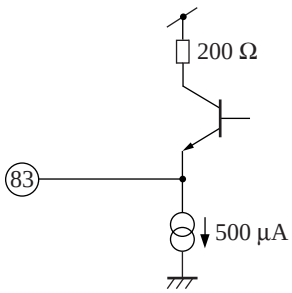
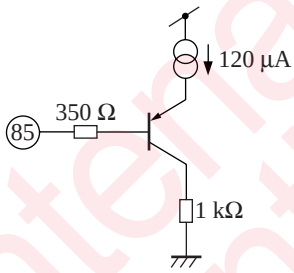
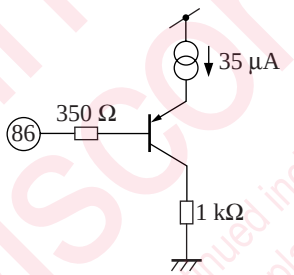
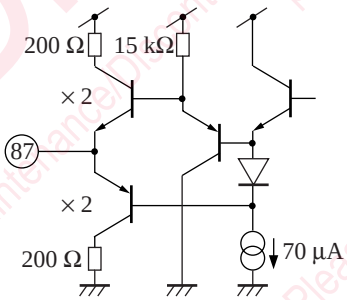
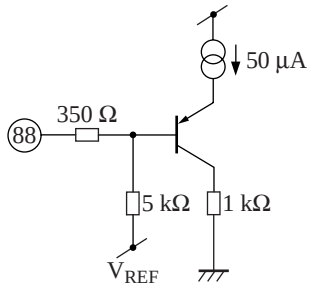
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
73		75DR OUT: 75 Ω driver output
74	—	GND: GND for Y/C mix., driver, color regeneration circuit
75		AGC OUT: YAGC output
76		0H GAMIN: Y gamma input non-delay signal
77		KNEE: Y gamma circuit knee setting: normally open

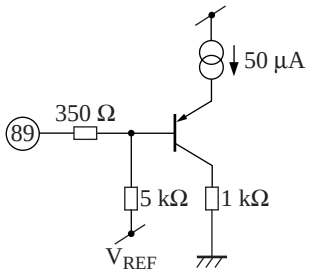
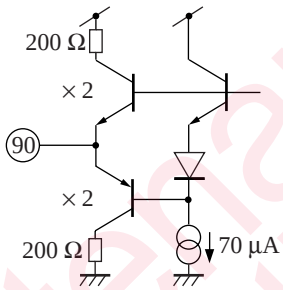
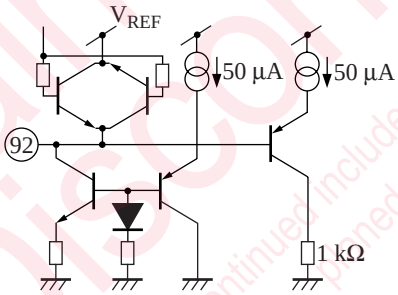
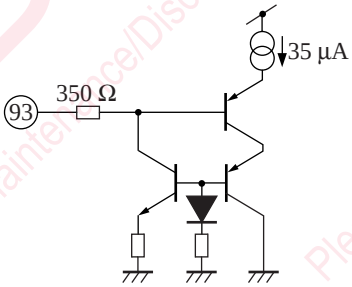
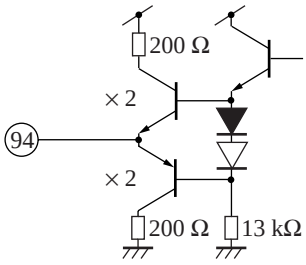
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
78		1H GAMIN: Y gamma input delay signal
79		YGAM DCC: Y gamma output DC stabilizing circuit capacitor pin
80		YGAM OUT: Y gamma output
81		PED SET: Pedestal level setting
82		VAP OUT: V aperture output

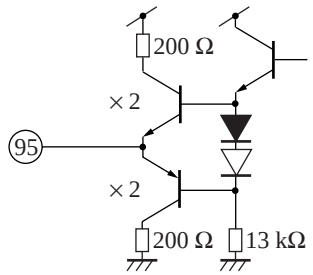
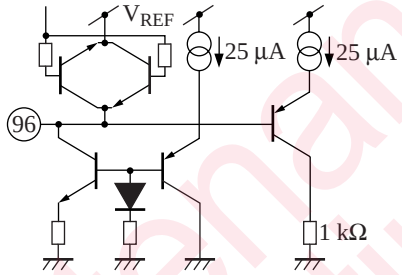
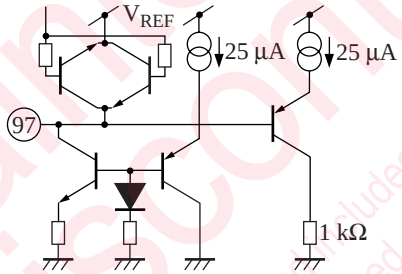
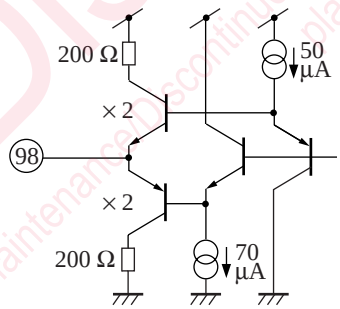
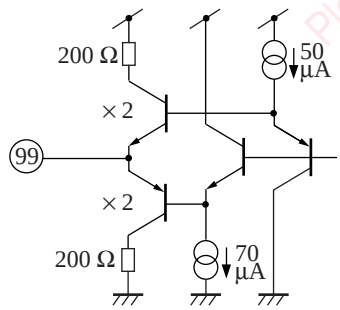
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
83		Y OUT: Luminance signal H/L clip Output with an appended pedestal.
84	—	GND: Signal processing-system GND
85		YGAMMA IN: Y gamma signal H aperture generation circuit input
86		FADE: Fade setting Fade status is 0.5 V or less.
87		HAP OUT: H aperture output
88		HAP BC IN: H aperture coring input

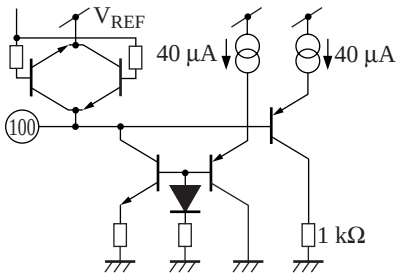
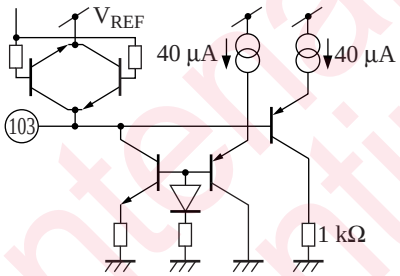
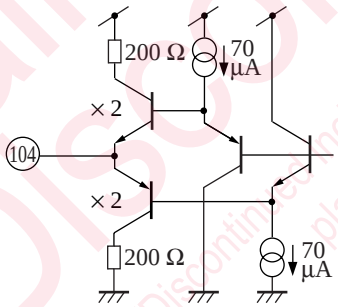
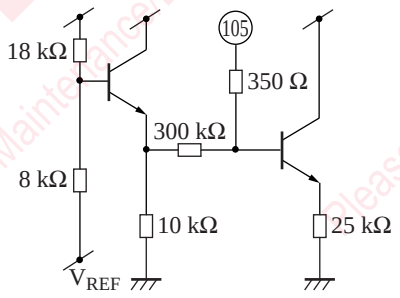
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
89		VAP BC IN: V aperture coring input
90		BCLIP OUT: Luminance signal aperture mix. output
91	—	V_{CC} : Signal processing-system V_{CC}
92		PEDESET IN: Luminance +aperture signal input
93		LLSUP IN: AGC output detection DC input
94		B-Y OUT: B-Y signal output

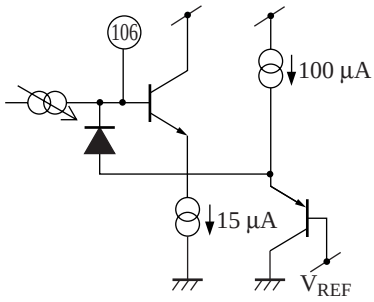
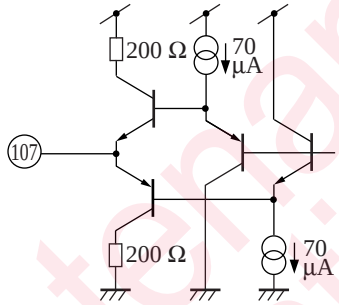
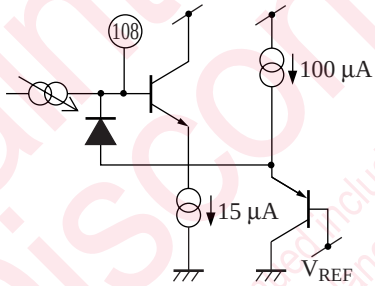
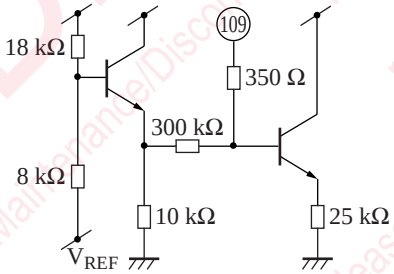
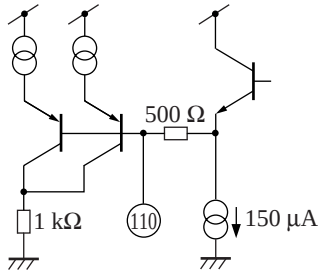
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
95		R-Y OUT: R-Y signal output
96		CGAMMA R-YIN: Color difference input (R-Y) after coincidence
97		CGAMMA Y-BIN: Color difference input (Y-B) after coincidence
98		CSW Y-BOUT: Color difference input (Y-B) for coincidence
99		CSW R-YOUT: Color difference input (R-Y) for coincidence

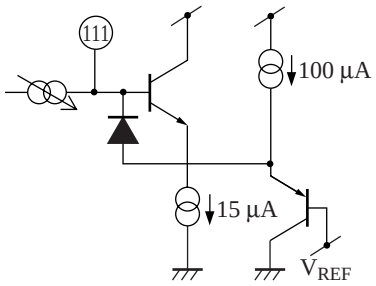
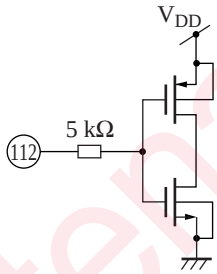
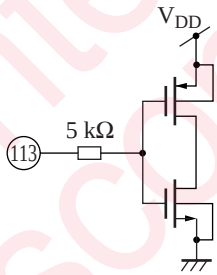
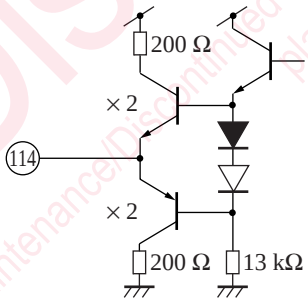
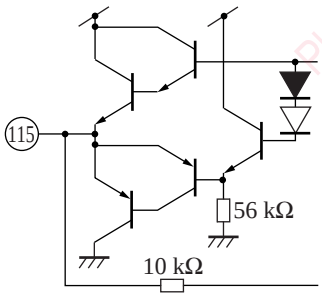
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
100		C0H IN: S/H output non-delay signal input
101	—	N.C.
102	—	N.C.
103		C1H IN: S/H output delay signal input
104		1HGC OUT2: Amplitude adjustment amp. output for CCD DL output (color difference)
105		1HGC IN2: Amplitude adjustment amp. input for CCD DL output (color difference)

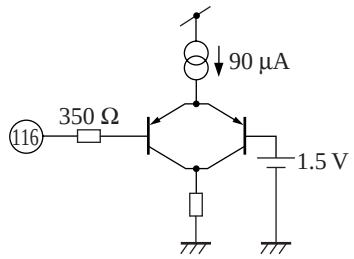
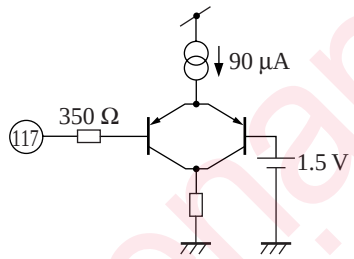
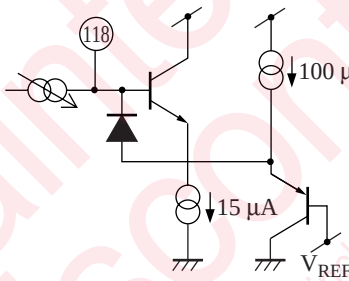
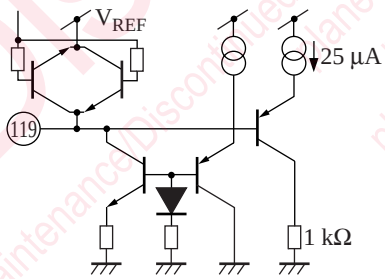
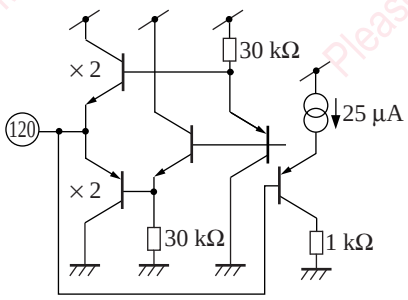
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
106		R-Y DCC: Connect a capacitor for DC control
107		1HGC OUT1: Amplitude adjustment amp. output for CCD DL output (luminance)
108		B-Y DCC: Connect a capacitor for DC control
109		1HGC IN1: Amplitude adjustment amp. input for CCD DL output (luminance)
110		CAGC TRAP: $4f_{SC}$ component elimination setting

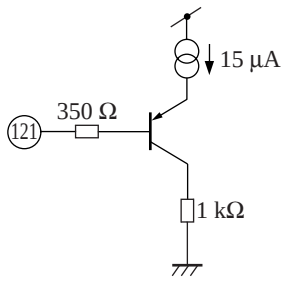
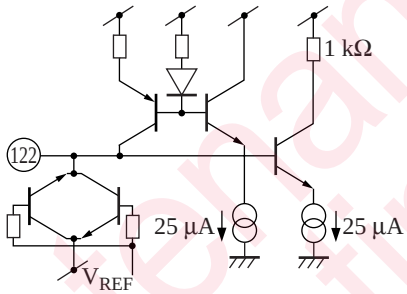
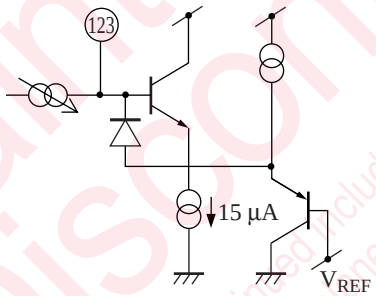
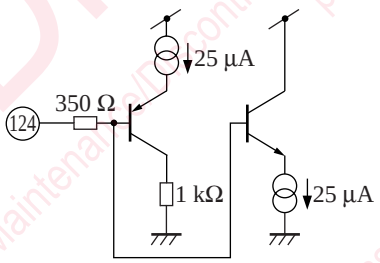
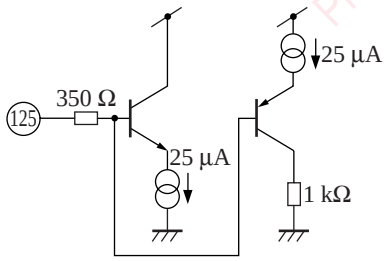
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
111		S/H DCC1: Capacitor connecting pin to stabilize sample hold output DC
112		ALC SW: ALC/ELC changeover SW Low: ALC mode High: ELC mode
113		AGC SW: AGC on/off SW Low: on High: off
114		S/H OUT: Output after color separation, S/H and WB
115		V_{REF} OUT: Reference voltage supply source: approx. 1.75 V Impedance: approx. 1 Ω

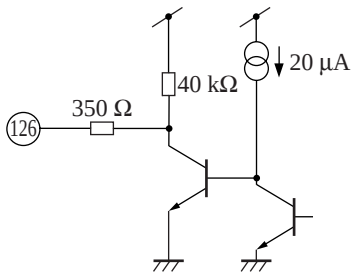
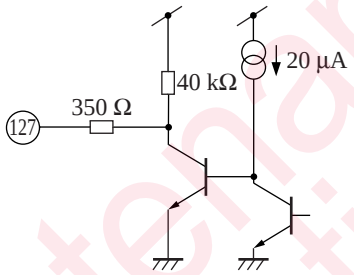
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
116		SP2: Sampling pulse input
117		SP1: Sampling pulse input
118		S/H DCC 2: Capacitor connecting pin to stabilize a sample hold output DC
119		SIG IN: CDS signal input
120		AGC FB: FB pin for AGC OP amp.

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
121		AGC OP−: Negative input for AGC OP amp.
122		CDSSIG IRIS: CDS signal input (for iris)
123		ALC DCC: Iris output stabilizing capacitor connecting pin
124		CPOB/HC: CPOB pulse input Luminance high cut setting
125		CP2/PBLK/CBLK: CP2, PBLK, CBLK pulse input

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description
126		DIST: ELC detection pulse
127		DRCT: ELC detection pulse
128	—	N.C.

■ Usage Notes

1. Turn on power supply

   Voltage supply to each V_{CC} pin (pin 11, pin 40, pin 72 and pin 91) should be done simultaneously.

2. Arrangement by external parts

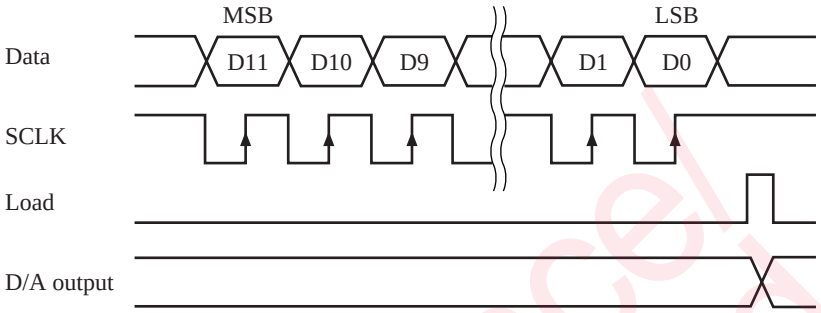
   1) Select a crystal part and adjust trimmer capacitor or variable capacitor so as to be a center frequency at free-running oscillation of $4f_{SC}$ crystal.

   2) The trap to be applied to pin 80 output is intended to eliminate f_{SK} /2, but decide it after studying carefully the use condition of a subject etc..

   3) As a countermeasure against an instantaneous power failure, the power reset circuit should be added to EXTLD pin of pin 29. And be sure to short-circuit it to GND when the power has recovered, and be sure to set the reset circuit so that the power is supplied after a waiting time of 16 V (V: vertical scanning period) or more from the input of stable HD and VD pulses applied at the same time that power supply is applied.

■ Application Notes

1. D/A pulse timing



2. D/A control data format

Last LSB → First MSB

D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11
← For D/A output →								← For channel selection →			

D0	D1	D2	D3	D4	D5	D6	D7	Equation for D/A output calculation arithmetic
0	0	0	0	0	0	0	0	$(V_{DD} / 256) \times 1$
1	0	0	0	0	0	0	0	$(V_{DD} / 256) \times 2$
0	1	0	0	0	0	0	0	$(V_{DD} / 256) \times 3$
1	1	0	0	0	0	0	0	$(V_{DD} / 256) \times 4$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
0	1	1	1	1	1	1	1	$(V_{DD} / 256) \times 255$
1	1	1	1	1	1	1	1	$(V_{DD} / 256) \times 256$

Load A

D8	D9	D10	D11	Selected ch.	Control functions
0	0	0	0	ch.1	ELC level
0	0	0	1	ch.2	R matrix
0	0	1	0	ch.3	B matrix
0	0	1	1	ch.4	External output (pin 16 output)
0	1	0	0	ch.5	External output (pin 17 output)
0	1	0	1	ch.6	LLSP setup
0	1	1	0	ch.7	Delay signal amp. gain control 1
0	1	1	1	ch.8	Delay signal amp. gain control 2
1	0	0	0	ch.9	AGC level
1	0	0	1	ch.10	AGC off gain
1	0	1	0	ch.11	CAGC max. gain
1	0	1	1	ch.12	YHI clip
1	1	0	0	ch.13	Burst level

■ Application Notes (continued)

2. D/A control data format (continued)

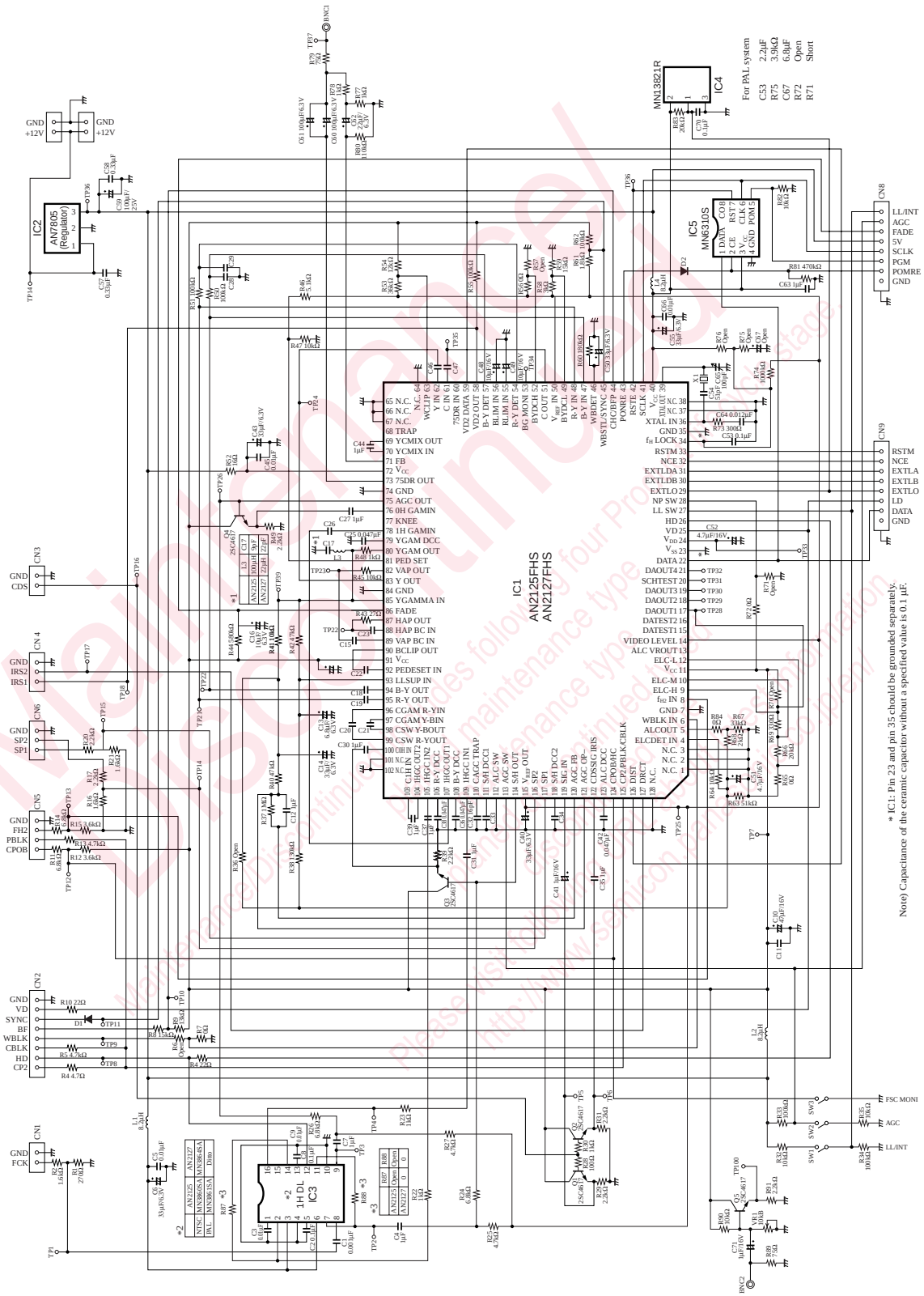
Load A (continued)

D8	D9	D10	D11	Selected ch.	Control functions
1	1	0	1	ch.14	External output (pin 15 test output)
1	1	1	0	ch.15	Carrier balance R (7 bits)
1	1	1	1	ch.16	Carrier balance B (7 bits)

Load B

D8	D9	D10	D11	Selected ch.	Control functions
0	0	0	0	ch.17	Burst phase
0	0	0	1	ch.18	B color regeneration DC
0	0	1	0	ch.19	B color regeneration KNEE
0	0	1	1	ch.20	External output (pin 21 test output)
0	1	0	0	ch.21	External output (pin 18 output)
0	1	0	1	ch.22	BWB offset
0	1	1	0	ch.23	RWB high limit
0	1	1	1	ch.24	RWB low limit
1	0	0	0	ch.25	RWB offset
1	0	0	1	ch.26	BWB high limit
1	0	1	0	ch.27	BWB low limit
1	0	1	1	ch.28	R color regeneration DC
1	1	0	0	ch.29	R color regeneration limit
1	1	0	1	ch.30	R color regeneration tilt
1	1	1	0	ch.31	External output (pin 19 output)
1	1	1	1	ch.32	YAGC max. gain

■ Application Circuit Example (Board camera)



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