

Silicon NPN Power Transistors

2SD820

DESCRIPTION

- With TO-3 package
- High voltage ,high speed
- Low collector saturation voltage

APPLICATIONS

- For color TV horizontal output applications

PINNING(see fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

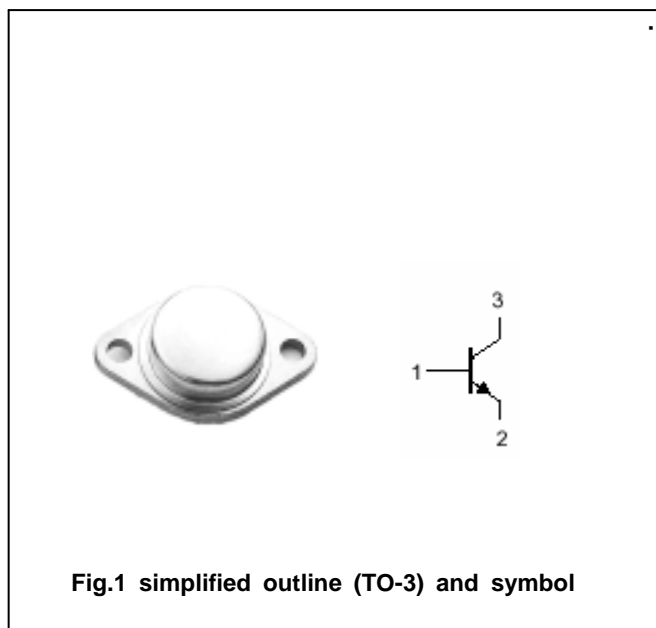


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings($T_a =$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	1500	V
V_{CEO}	Collector-emitter voltage	Open base	600	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		5	A
I_E	Emitter current		-5	A
P_C	Collector power dissipation	$T_C=25$	50	W
T_j	Junction temperature		150	
T_{stg}	Storage temperature		-65~150	

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CHARACTERISTICS

T_j=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CE0(SUS)}	Collector-emitter sustaining voltage	I _C =0.1A; I _B =0	600			V
V _{CEsat}	Collector-emitter saturation voltage	I _C =4 A; I _B =0.8 A		3.0	5.0	V
V _{BEsat}	Base-emitter saturation voltage	I _C =4 A; I _B =0.8 A			1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =500V; I _E =0			10	μ A
I _{EBO}	Emitter cut-off current	V _{EB} =5V; I _C =0			1	mA
h _{FE}	DC current gain	I _C =1A ; V _{CE} =5V	8	20		
C _{OB}	Output capacitance	I _E =0; V _{CB} =10V; f=1MHz		165		pF
f _T	Transition frequency	I _C =0.1A ; V _{CE} =10V		3		MHz
t _f	Fall time	I _{CP} =4A ; I _{B1} =0.8A		0.5	1.0	μ s

PACKAGE OUTLINE

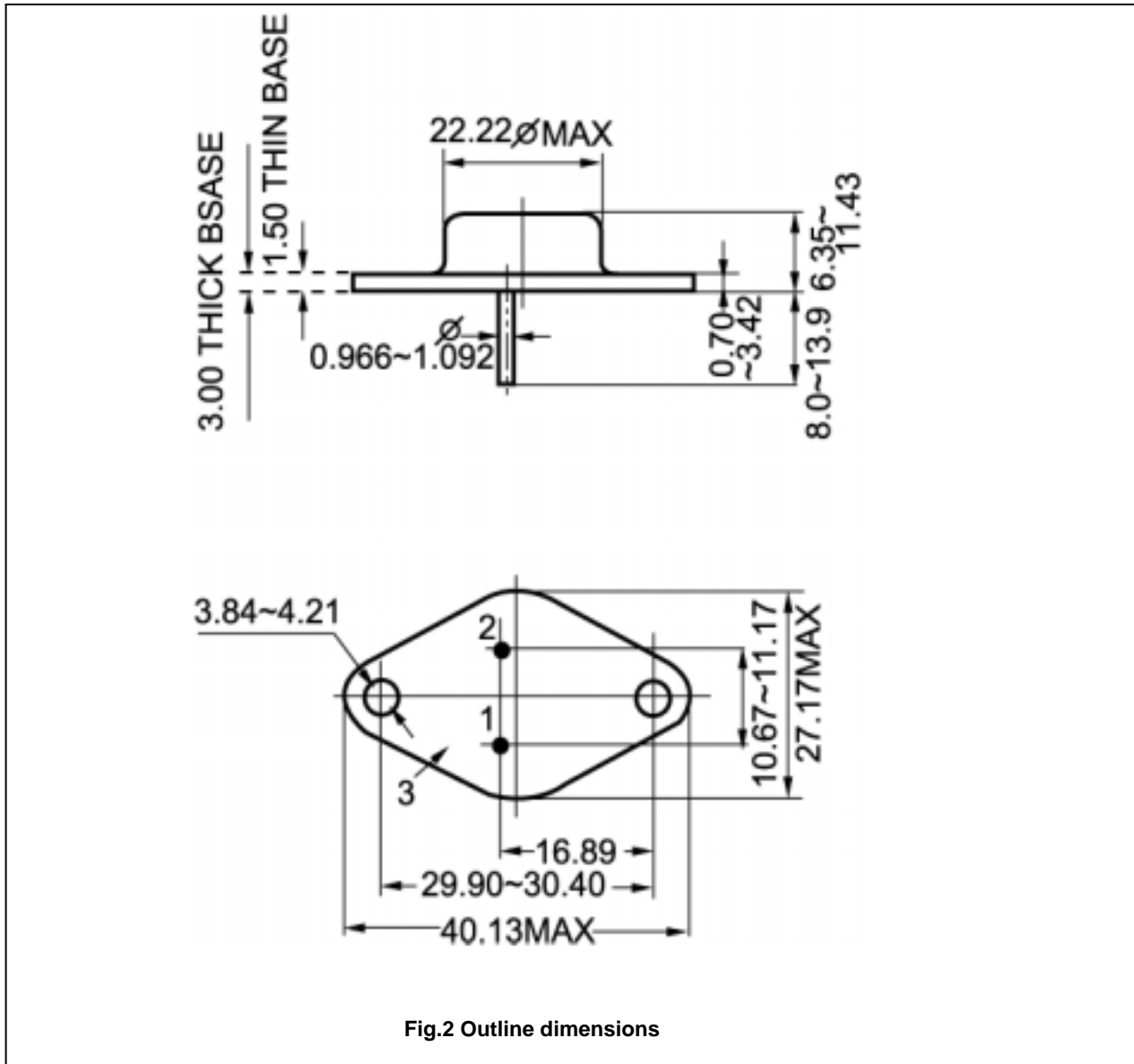


Fig.2 Outline dimensions