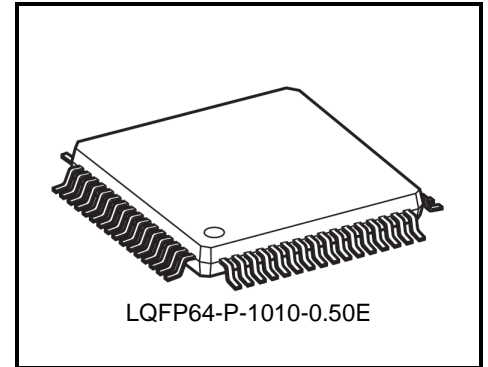TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC90107FG

Single Channel Video Decoder

The TC90107FG is a single chip IC that converts analog video signal to digital video signal. (ITU-R BT.656)
   Additionally, the TC90107FG has one 10bit ADC as analog input interface, and has one 3-line Y/C separation, and multi-system color decoder.

LQFP64-P-1010-0.50E

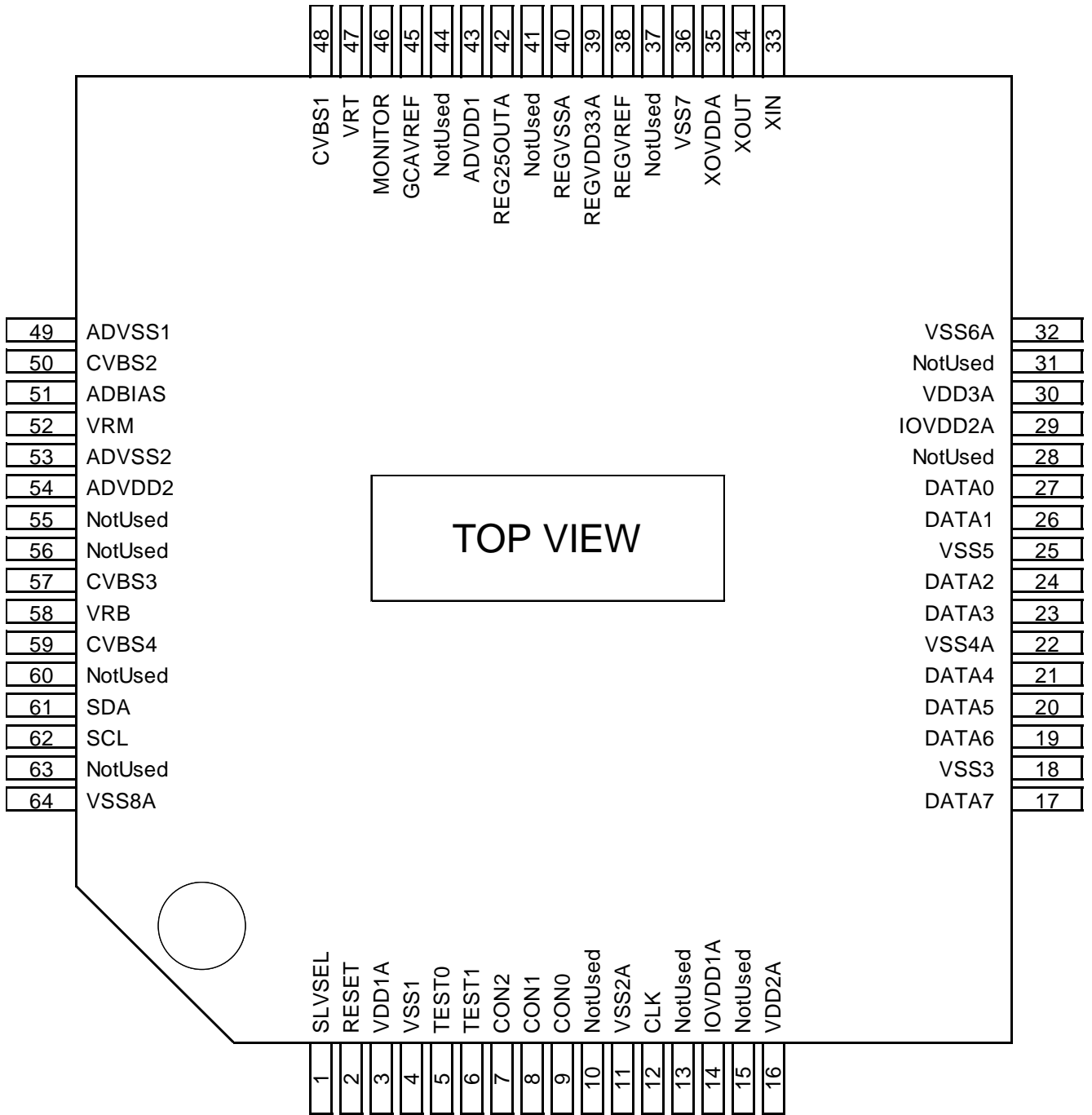Weight**:** 0.40 g (typ.)

1. Features

1. Analog Video signal Input **:**   CVBS

2. Adaptive multi-color decoder (1ch)

3. Sync processing / Video system detection

4. 10bit ADC (1ch)

5. Analog AGC (Sync AGC + Peak AGC)

6. LPF circuit for input analog video signal

7. Y/C separation**:**   3-line YCS (NTSC/PAL)

    Band Pass Filter (SECAM)

8. Picture process   Y**:**   HV enhance, V enhance, LTI, sharpness, noise cancel,
                    Dynamic gamma correction, Static gamma correction
                    Contrast, Brightness

           C**:**   TOF, ACC, Color gain, Color offset, CTI, noise cancel, Tint,
                    Color management, Color gain correction linked to Y-gamma

9. Function   Horizontal aberration correction, Data slice(WSS / Video-ID / CC), S/N detection

10. Digital Video signal output**:**   ITU-R BT.656

11. I^2C-bus control

12. Regulator circuit   (3.3 V input / 2.5 V output)

13. Package**:**   LQFP 64 Pin (0.50 mm pitch)

14. Power supply**:**   3.3 V, 2.5 V, 1.5 V

15. Operation temperature**:** -40°C to 85°C

2. Block Diagram
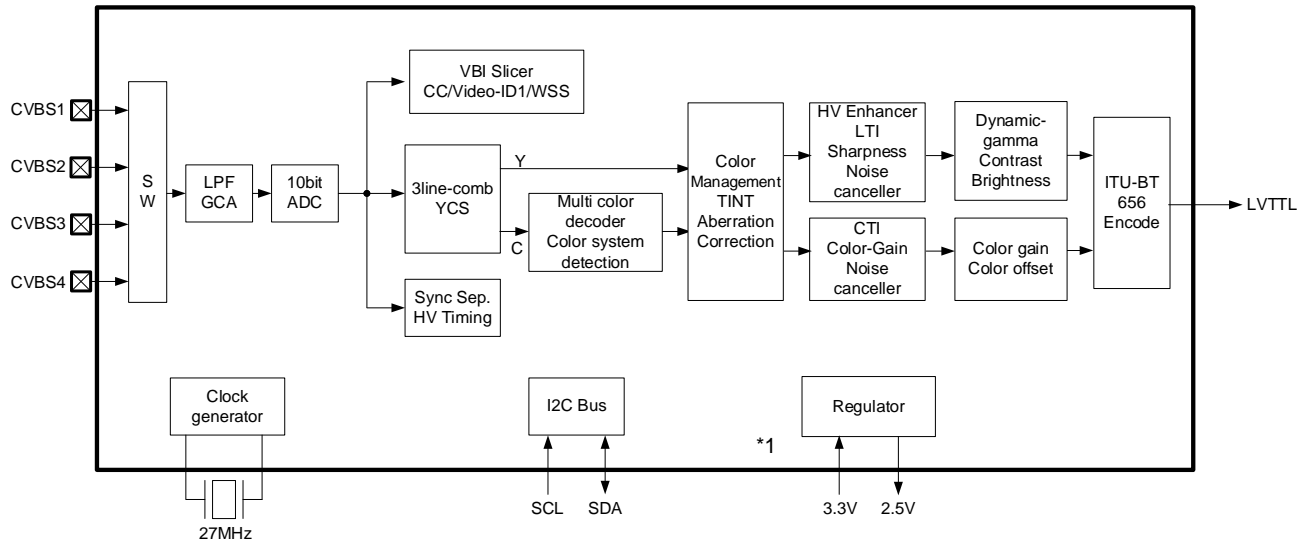
*1**:** Regulator output 2.5 V is not connected in the inside of IC.
When it use built in Regurator, it connected on board.

3. Pin Layout

Top pins (48 to 33):

Pin	Name
48	CVBS1
47	VRT
46	MONITOR
45	GCAVREF
44	NotUsed
43	ADVDD1
42	REG25OUTA
41	NotUsed
40	REGVSSA
39	REGVDD33A
38	REGVREF
37	NotUsed
36	VSS7
35	XOVDDA
34	XOUT
33	XIN

Left pins (49 to 64):

Pin	Name
49	ADVSS1
50	CVBS2
51	ADBIAS
52	VRM
53	ADVSS2
54	ADVDD2
55	NotUsed
56	NotUsed
57	CVBS3
58	VRB
59	CVBS4
60	NotUsed
61	SDA
62	SCL
63	NotUsed
64	VSS8A

TOP VIEW

Right pins (32 to 17):

Pin	Name
32	VSS6A
31	NotUsed
30	VDD3A
29	IOVDD2A
28	NotUsed
27	DATA0
26	DATA1
25	VSS5
24	DATA2
23	DATA3
22	VSS4A
21	DATA4
20	DATA5
19	DATA6
18	VSS3
17	DATA7

Bottom pins (1 to 16):

Pin	Name
1	SLVSEL
2	RESET
3	VDD1A
4	VSS1
5	TEST0
6	TEST1
7	CON2
8	CON1
9	CON0
10	NotUsed
11	VSS2A
12	CLK
13	NotUsed
14	IOVDD1A
15	NotUsed
16	VDD2A

4. Pin Description

No.	Pin Name	I/O	Function	Tolerable Voltage [V]	Circuit	Treatment when not in use
1	SLVSEL	I	I^{2}C slave address select	3.3	Digital	Full-time use
2	RESET	I	System Reset (Reset is Low.)	5	Digital	GND
3	VDD1A	DVDD	Power supply for Logic: 1.5V	1.5	Digital	1.5 V
4	VSS1	DVSS	GND for Logic	0	Digital	GND
5	TEST0	I	Test Terminal 0	3.3	Digital	GND
6	TEST1	I	Test Terminal 1	3.3	Digital	GND
7	CON2	O	Timing Pulse Output 2	3.3	Digital	Open
8	CON1	O	Timing Pulse Output 1	3.3	Digital	Open
9	CON0	O	Timing Pulse Output 0	3.3	Digital	Open
10	NotUsed	N.C.	Not connect	-	Digital	Full-time open
11	VSS2A	DVSS	GND for Logic	0	Digital	GND
12	CLK	O	CLK Output	3.3	Digital	Open
13	NotUsed	N.C.	Not connect	-	Digital	Full-time open
14	IOVDD1A	IOVDD33	Power supply for IO: 3.3 V	3.3	Digital	3.3 V
15	NotUsed	N.C.	Not connect	-	Digital	Full-time open
16	VDD2A	DVDD	Power supply for Logic: 1.5 V	1.5	Digital	1.5 V
17	DATA7	O	Digital data output 7	3.3	Digital	Open
18	VSS3	DVSS	GND for Logic	0	Digital	GND
19	DATA6	O	Digital data output 6	3.3	Digital	Open
20	DATA5	O	Digital data output 5	3.3	Digital	Open
21	DATA4	O	Digital data output 4	3.3	Digital	Open
22	VSS4A	DVSS	GND for Logic	0	Digital	GND
23	DATA3	O	Digital data output 3	3.3	Digital	Open
24	DATA2	O	Digital data output 2	3.3	Digital	Open
25	VSS5	DVSS	GND for Logic	0	Digital	GND
26	DATA1	O	Digital data output 1	3.3	Digital	Open
27	DATA0	O	Digital data output 0	3.3	Digital	Open
28	NotUsed	N.C.	Not connect	-	Digital	Full-time open
29	IOVDD2A	IOVDD33	Power supply for IO: 3.3 V	3.3	Digital	3.3 V
30	VDD3A	DVDD	Power supply for Logic: 1.5 V	1.5	Digital	1.5 V
31	NotUsed	N.C.	Not connect	-	Digital	Full-time open
32	VSS6A	DVSS	GND for Logic	0	Digital	GND

No.	Pin Name	I/O	Function	Tolerable Voltage [V]	Circuit	Treatment when not in use
33	XIN	I	X'tal OSC circuit input terminal	3.3	Digital	Full-time use
34	XOUT	O	X'tal OSC circuit output terminal	3.3	Digital	Full-time use
35	XOVDDA	XOVDD	Power supply for X'tal: 3.3 V	3.3	Digital	2.5 V or 3.3 V
36	VSS7	DVSS	GND for Logic	0	Digital	GND
37	NotUsed	N.C.	Not connect	-	Digital	Open
38	REGVREF	BIAS	Voltage relay for Internal Regulator	2.5	analog	GND via 0.1 µF
39	REGVDD33A	AVDD33	Power supply for Internal Regulator (for ADC block)	3.3	analog	3.3 V
40	REGVSSA	AVSS	Analog GND for Internal Regulator	0	analog	GND
41	NotUsed	N.C.	Not connect	-	Digital	Full-time open
42	REG25OUTA	O	Output of Internal Regulator (For ADC)	2.5	analog	Open
43	ADVDD1	AVDD25	Power supply for ADC&GCA: 2.5 V	2.5	analog	2.5 V
44	NotUsed	N.C.	Not connect	-	Digital	Full-time open
45	GCAVREF	BIAS	Reference voltage output for GCA	2.5	analog	GND via 0.1 µF
46	MONITOR	O	Monitor terminal for GCA	2.5	analog	Full-time open
47	VRT	BIAS	Reference top voltage of ADC	2.5	analog	Full-time use
48	CVBS1	I	CVBS input 1	2.5	analog	Open
49	ADVSS1	AVSS	Analog GND for ADC/GCA	0	analog	GND
50	CVBS2	I	CVBS input 2	2.5	analog	Open
51	ADBIAS	BIAS	Reference voltage of ADC	2.5	analog	Full-time use
52	VRM	BIAS	Reference middle voltage of ADC	2.5	analog	Full-time use
53	ADVSS2	AVSS	Analog GND for ADC/GCA	0	analog	GND
54	ADVDD2	AVDD25	Power supply for ADC&GCA: 2.5 V	2.5	analog	2.5 V
55	NotUsed	N.C.	Not connect	-	Digital	Full-time open
56	NotUsed	N.C.	Not connect	-	Digital	Full-time open
57	CVBS3	I	CVBS input 3	2.5	analog	Open
58	VRB	BIAS	Reference bottom voltage of ADC	2.5	analog	Full-time use
59	CVBS4	I	CVBS input 4	2.5	analog	Open
60	NotUsed	N.C.	Not connect	-	Digital	Full-time open
61	SDA	I/O	I²C DATA input	5	Digital	Full-time use
62	SCL	I	I²C CLOCK input	5	Digital	Full-time use
63	NotUsed	N.C.	Not connect	-	Digital	Open
64	VSS8A	DVSS	GND for Logic	0	Digital	GND

5. Function

- Multi-color decoder
- Output format is ITU-R BT.656
- The TC90107FG has many video quality improving function, such as HVD-Enhancer, dynamic-gamma, color-management and so on.
- Horizontal nonlinearly scaling (horizontal fish-eye correction, horizontal trapezoid correction and so on)
- VBI data slicer function (Closed caption, Video-ID and WSS are available.)
- Regulator circuit (3.3 V input / 2.5 V output) for ADC circuit by external connection.

5.1   Analog video signal input

5.1.1   Analog video signal input amplitude level

The TC90107FG has one 10bit ADC for 1ch CVBS input.
The dynamic range of this ADC is designed in AVDD*0.4 with the normal input dynamic range being
1 Vp-p (AVDD = 2.5 V).
Be sure to use 0.7 Vp-p with 140IRE input when using CVBS as the recommended reference input amplitude.
The TC90107FG has AGC function for CVBS input**:** however, to use the AGC cover range effectively we recommend that you use 0.7 Vp-p with 140IRE input for the input amplitude.

5.1.2   Analog video signal reference input level

1) Reference input level for Composite Video signal when 100% white (i.e. composite video input)

Composite Video signal input level   (Ex**:** 75% color bar)
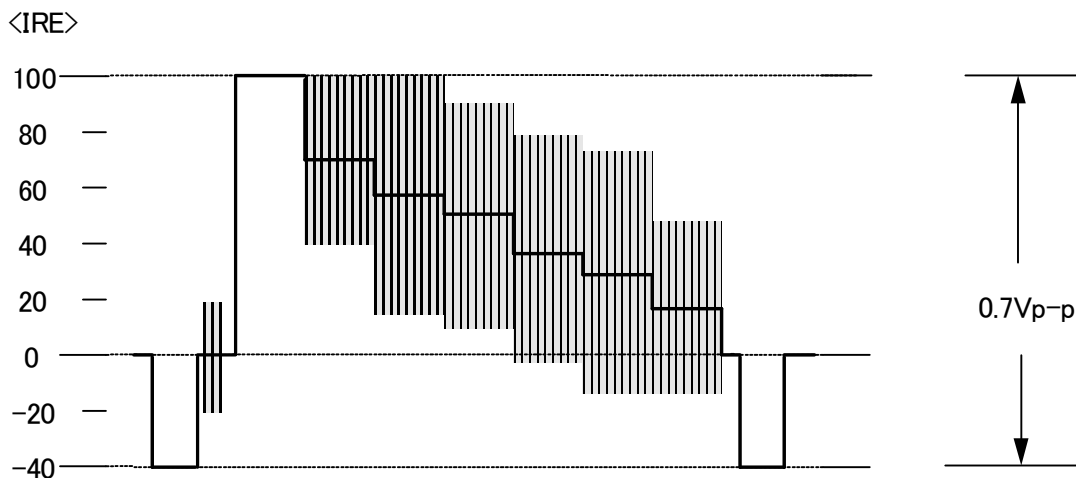
5.1.3   AGC (Auto Gain Control) function

AGC function is used for composite video signal by GCA (Gain control amp) circuit and digital AGC function.
AGC function has two mode**:** AUTO gain mode and manual gain mode.
It is possible to use 1.0 Vp-p input amplitude by GCA function.

5.1.4   LPF function

TC90107FG has LPF for anti-aliasing in front of GCA block. It is possible to select ON or through mode.
- System **:** Fourth-order Butterworth filter
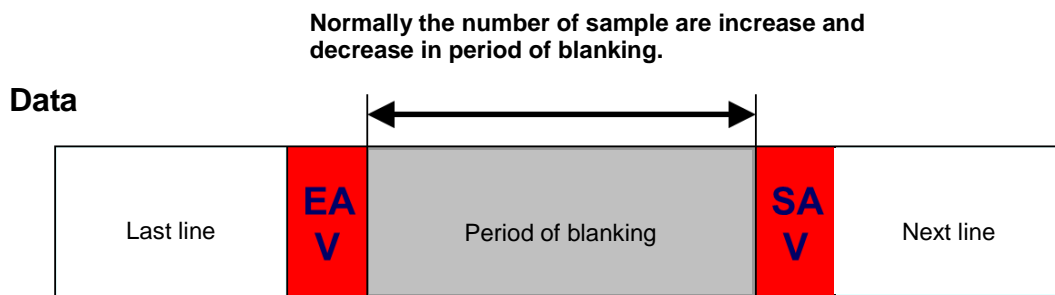- Frequency characteristic **:** -1 dB@6 MHz, -14 dB@13.5 MHz

5.2   Digital output signal (Outsel Block)

5.2.1   Output signal format

The TC90107FG output is the ITU-R BT.656.
Pedestal level for Y signal is 16 LSB.
Center level for Cb and Cr signal is 128 LSB.

∗NOTICE
TC90107FG use the free-run clock system.
Therefore, The number of sample between EAV and SAV occur the increase and decrease.
It must take the data from SAV start. If mistake , It will occur the jitter.
You must design , it is not affected by the number of sample in blanking.

Normally the number of sample are increase and decrease in period of blanking.

Data

| Last line | EAV | Period of blanking | SAV | Next line |

- The system needs not to affect in irregular EAV and SAV about ITU-R BT.656.
  The uptake start of picture must be SAV.

- When it is not suitable for ITU-R BT.656, it deeds to confirm in combination with the following signals.
 1) HD
 2) VD
 3) Data Enable
 4) Field Flag (ODD/EVEN)
 5) U/V Flag (CbCr select)

TC90107FG can output three timing signals chosen by register at timing output terminal(CON[2:0]).

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5.2.1.1.　Input of 525i/60Hz
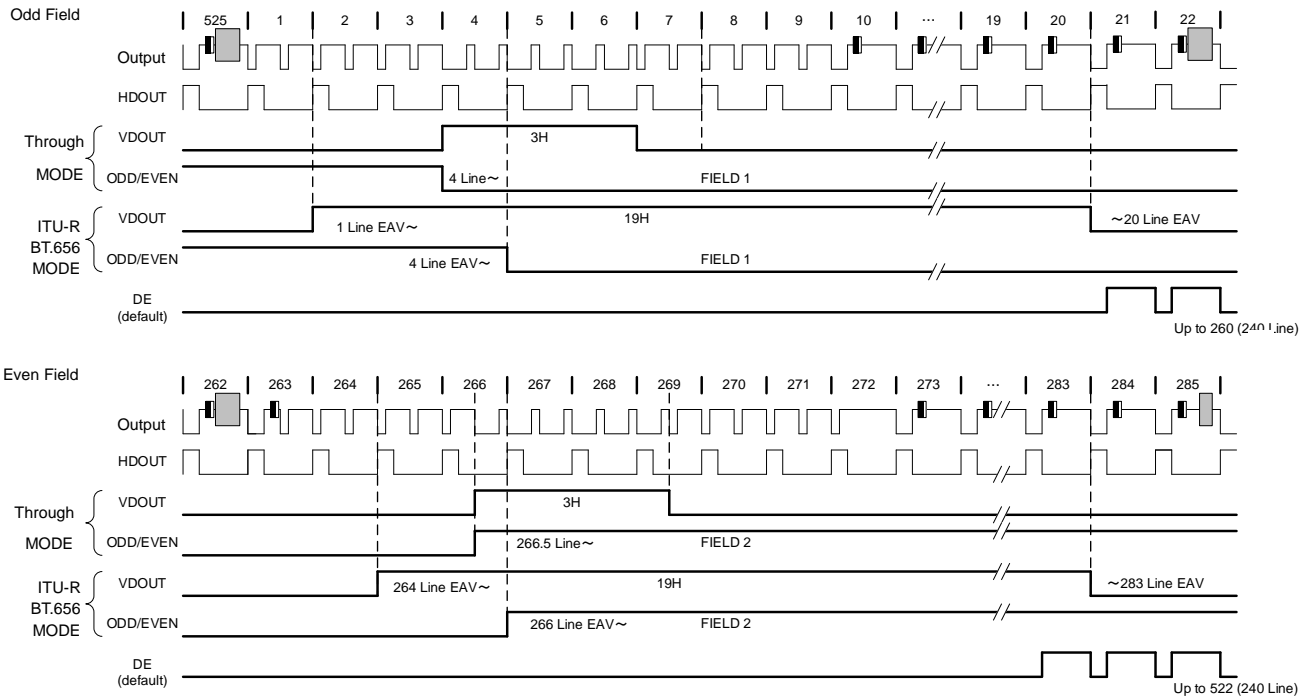
5.2.1.2.　Input of 625i/50Hz
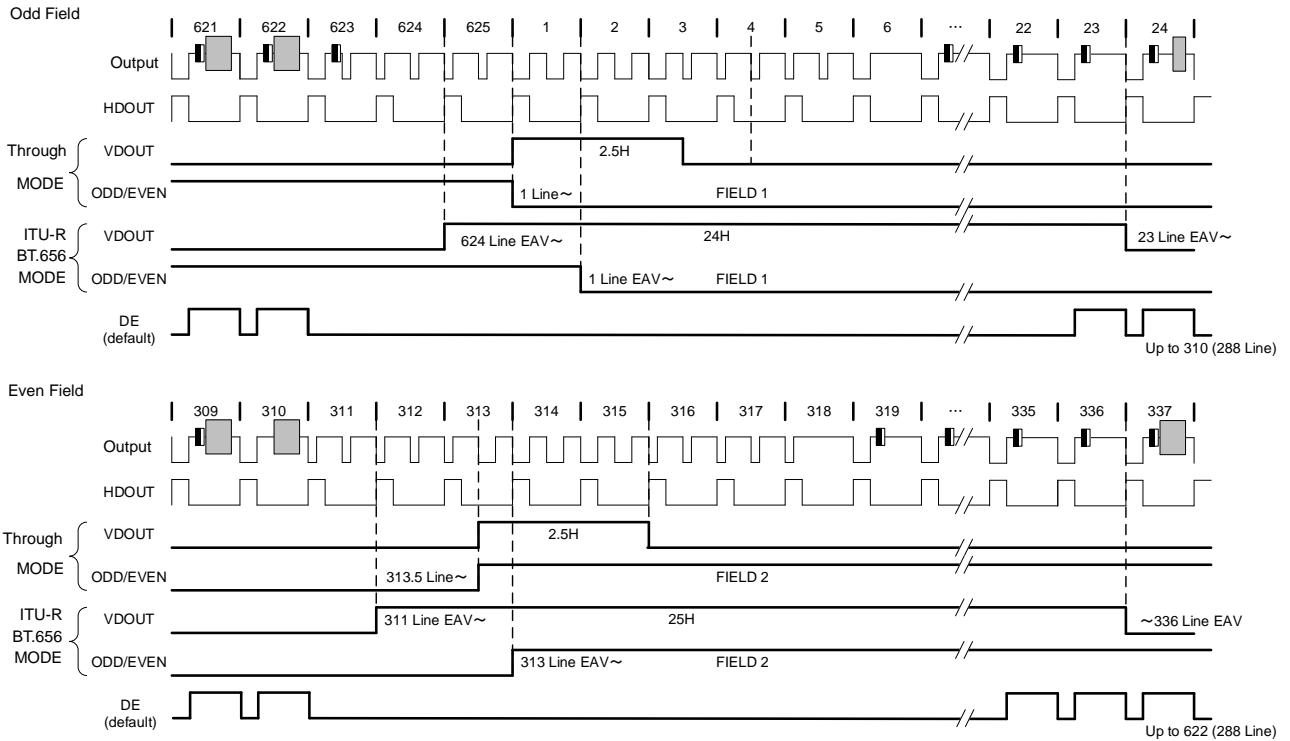
5.2.2   Timing pulse output

CON[2:0] pin(terminal No.7, 8, 9) are output terminal. Output signal can select by register.

1. DE (Data Enable) signal
   DE indicates horizontal and vertical enable picture area for output video signal.
   DE signal is the signal that is HIGH status at active video period, and LOW status at blanking period.

2. HD signal
   HD signal indicates the horizontal sync pulse synchronized with output video signal.
   Setting **:** pulse width, pulse polarity, phase delay

3. VD signal
   VD signal indicates the vertical sync pulse synchronized with output video signal.
   Setting **:** pulse width, pulse polarity, phase delay

4. FIELD signal
   FIELD signal indicates ODD/EVEN switch pulse synchronized with output video signal.
   Field signal is the signal that is HIGH status at even field, and LOW status at odd field, when default setting.
   Polarity of FIELD signal inverts by register [FLDO_POLE].

5. UVFLG signal
   UVFLG signal indicates Cb/Cr switch pulse for 4:2:2 format signal.
   Polarity of UVFLG signal inverts by register [UVREV].

5.3   Regulator circuit

The regulator circuit of 2.5 V output (3.3 V input) for ADC circuit is built in IC.

To use regulator output voltage, it is necessary to connect the output terminal of regulator circuit to the power supply input terminal of an ADC circuit in IC exterior.
In addition, please do not use the built-in regulator circuit other than the purpose of this IC operation.
When it is no use the built-in regulator, do not supply 3.3 V at 39 pin.

| Regulator circuit		The Input terminal
3.3 V Input terminal	2.5 V Output terminal	which regulator output
REGVDD33A (39 pin)	REG25OUTA (42 pin)	ADVDD1 (43 pin) ADVDD2 (54 pin)

6. Absolute maximum rating

The absolute maximum ratings are rated values which must not be exceeded during operation, even for an instant. Exceeding the absolute maximum ratings may result in destruction, degradation or other damage to the IC and other components. When designing applications for this IC, be sure that none of the absolute maximum rating values will ever be exceeded.

Characteristics	Terminal No.	Symbol	Rating	Unit
Power voltage1 (1.5 V)	3, 16, 30	VDD1	-0.3 to VSS + 2.0	V
Power voltage2 (2.5 V)	43, 54	VDD2	-0.3 to VSS + 3.5	V
Power voltage3 (3.3 V)	14, 29, 35, 39	VDD3	-0.3 to VSS + 3.9	V
Input voltage (2.5 V)	48, 50, 57, 59	VIN2	-0.3 to VDD2 + 0.3	V
Input voltage (3.3 V)	1, 33	VIN3	-0.3 to VDD3 + 0.3	V
Input voltage (3.3 V system, 5 V withstand voltage)	2, 61, 62	VIN4 (Note.1)	-0.3 to VSS + 5.5	V
Potential difference between power pins (between 1.5 V system power pins)	-	ΔVDG1 (Note.2)	0.3	V
Potential difference between power pins (between 2.5 V system power pins)	-	ΔVDG2 (Note.2)	0.3	V
Potential difference between power pins (between 3.3 V system power pins)	-	ΔVDG3 (Note.2)	0.3	V
Power dissipation	-	PD (Note.3)	1739	mW
Storage temperature	-	Tstg	-40 to 125	°C

Note1**:** The withstand voltage for pins (SDA, SCL, RESET) is 5 V.

Note2**:** For each of 1.5 V and 2.5 V and 3.3 V, system power supply terminal is made into the same voltage.
The maximum potential difference should not exceed rating for all power supply terminals then.
In addition, potential difference between all VSS terminal must be under 0.01 V in this status.

Note3**:** If you intended to use a temperature higher than Ta = 25°C, reduce by 17.39 mW per one degree (°C) increase.
The case of Ta = 85°C, power dissipation is 696 mW.
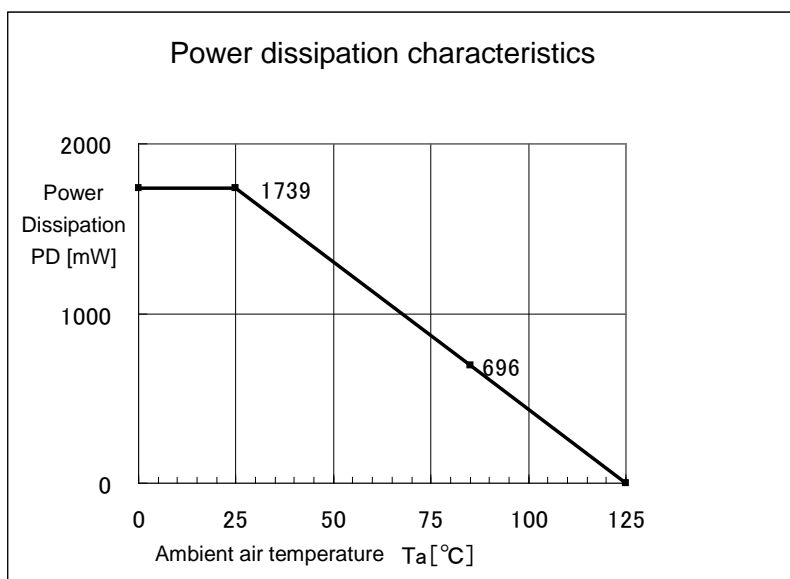
7. Operating Range

The TC90107FG is not guaranteed to function correctly if it is used outside its specified power voltage rage (1.5 V system power: 1.40 V to 1.60 V, 2.5 V system power: 2.3 V to 2.7 V, 3.3 V system power: 3.0 V to 3.6 V). Please use within the specified operating conditions.

If you temporarily leave and then return to the specified operating conditions, this IC's conditions will change, and so it is necessary to reset the IC's power to continue using it correctly within the specified operating conditions.

Characteristics	Terminal No.	Symbol	Min	Typ.	Max	Unit
Power voltage of digital block	3, 16, 30	VDD-D	1.4	1.5	1.6	V
Power voltage of I/O block (*1)	14, 29	VDD-IO	3.0	3.3	3.6	V
Power voltage of regulator block (*1)	39	VDD-REG	3.0	3.3	3.6	V
Power voltage of XO block (*2)	35	VDD-XO	2.3	3.3	3.6	V
Power voltage of analog block	43, 54	VDD-AD	2.3	2.5	2.7	V
Operating templature		Topr	-40	-	85	°C

(*1) If possible, please set I/O power supply voltage and regulator power supply voltage into the potential.
(*2) When you connect XO power supply to 2.5 V power supply, if possible, please use the potential with analog power supply voltage.
    Although connecting with 3.3 V power supply is also possible, please set I/O power supply voltage and regulator power supply voltage as the potential in that case.

8. Electrical characteristic

8.1 DC characteristic

(Ta = 25°C, VDD1 = 1.50 ± 0.1 V, VDD2 = 2.50 ± 0.2 V, VDD3 = 3.30 ± 0.3 V)

Charact erisitc	Terminal No..	Symbol	Min	Typ.	Max	Unit	Note
Power supply current (*4)	3, 16, 30	IDD1 (1.5 V)	-	-	75	mA	
	43, 54	IDD2 (2.5 V)	-	-	75	mA	When a built-in regulator was not used but 2.5 V power supply is supplied from the out side.
	14, 29, 35, 39	IDD3-1 (3.3 V)	-	-	30	mA	When a built-in regulator was not used but 2.5 V power supply is supplied from the out side.
		IDD3-2 (3.3 V)	-	-	105	mA	When a built-in regulator is used.
Input voltage	1, 33	VIH	VDD3 x 0.8	-	VDD3	V	I/O input terminal of 3.3 V system.
	2, 61, 62						I/O input terminal of 5.0 V system.
	1, 33	VIL	VSS	-	VDD3 x 0.2	V	I/O input terminal of 3.3 V system.
	2, 61, 62						I/O input terminal of 5.0 V system.
Input current	1, 33	IIH	-10	-	10	μA	I/O input terminal of 3.3 V system.
	2, 61, 62						I/O input terminal of 5.0 V system.
	1, 33	IIL	-10	-	10	μA	I/O input terminal of 3.3 V system.
	2, 61, 62						I/O input terminal of 5.0 V system.
Output voltage	7, 8, 9, 12, 17, 19, 20, 21, 23, 24, 26, 27, 34	VOH	VDD3 - 0.6	-	VDD3	V	I/O output terminal of 3.3 V system. When load current: -4 mA
		VOL	VSS	-	0.4	V	I/O output terminal of 3.3 V system. When load current: +4 mA

(*4) Power consumption (W) changes the calculation method by whether a built-in regulator is used or it is not used.
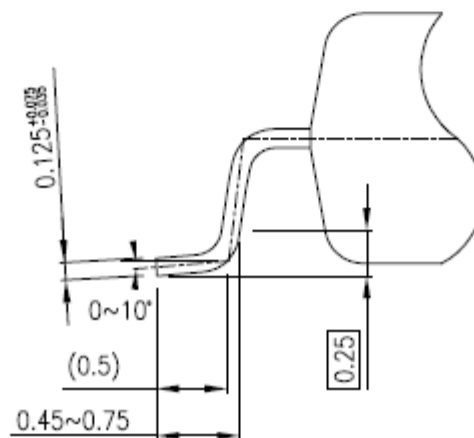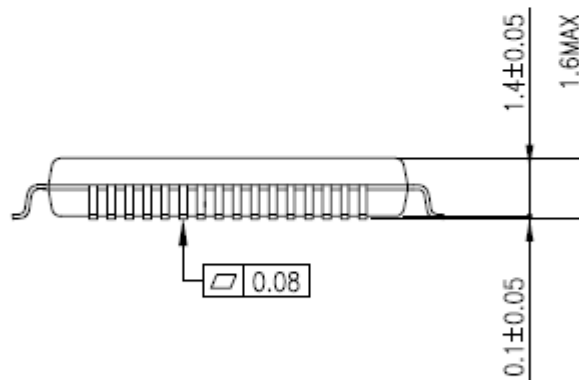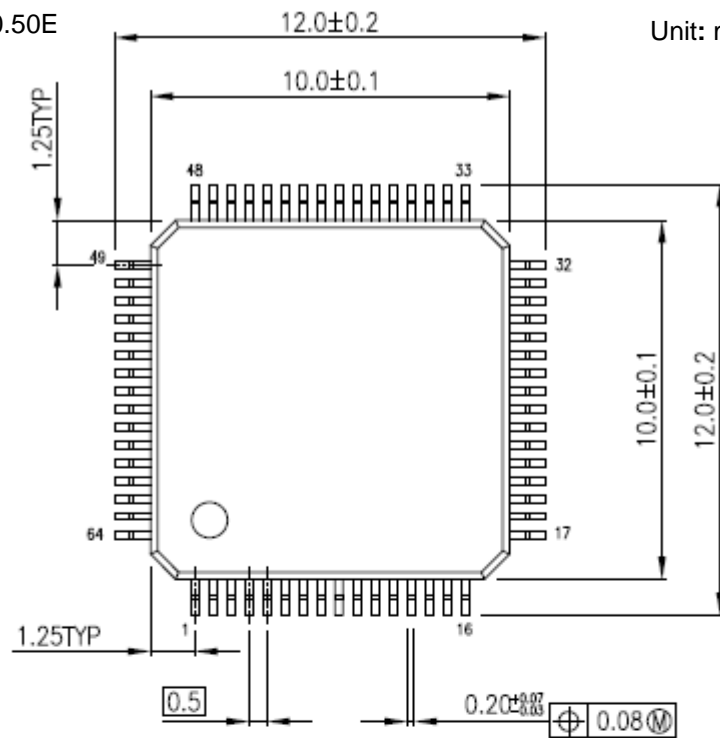　　When a built-in regulator is used : Sum total of IDD1 and IDD3-2
　　When a built-in regulator is not used : Sum total of IDD1, IDD2, and IDD3-1

9. Package

LQFP64-P-1010-0.50E

Unit: mm

Weight: 0.40 g (Typ.)

10. Revision History

Date	Revision	Contents
2015/11/24	1.00	First edition

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