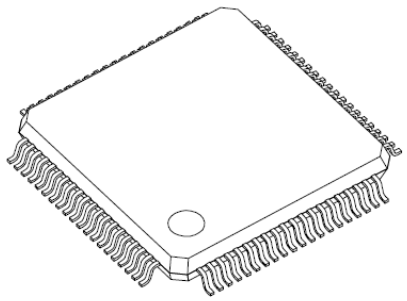
TOSHIBA C-MOS Digital Integrated Circuit Silicon Monolithic

TC90105FG

Dual channel Video Decoder

TC90105FG is a single chip IC that converts analog video signals to digital video signals (ITU-R BT.601 / ITU-R BT.656).

Additionally, the TC90105FG has a 10bit A/D converter as an analog input interface and has 3-line Y/C separation and multi-system color decoder functionality and a variegated image quality processing capability.



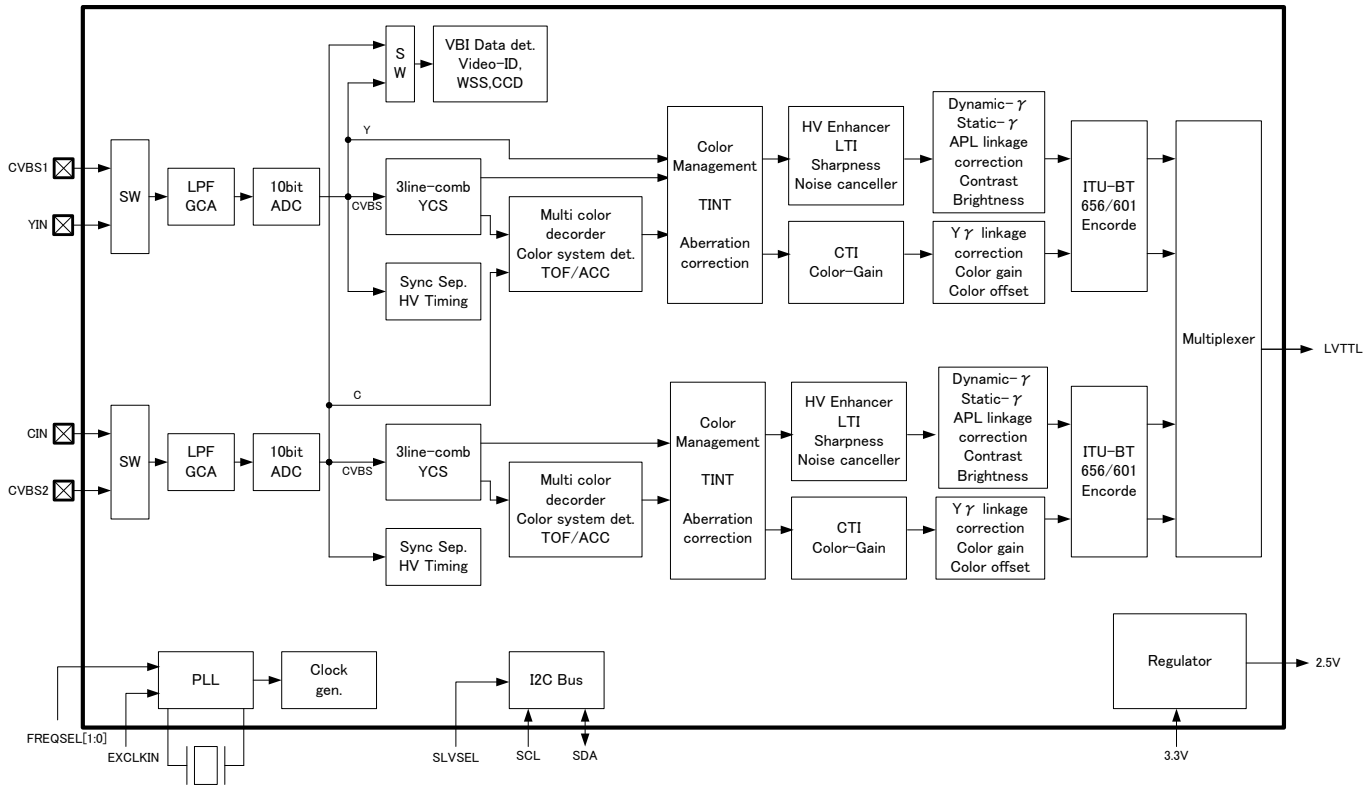
LQFP80-P-1212-0.50F

Weight: 0.50 g (typ.)

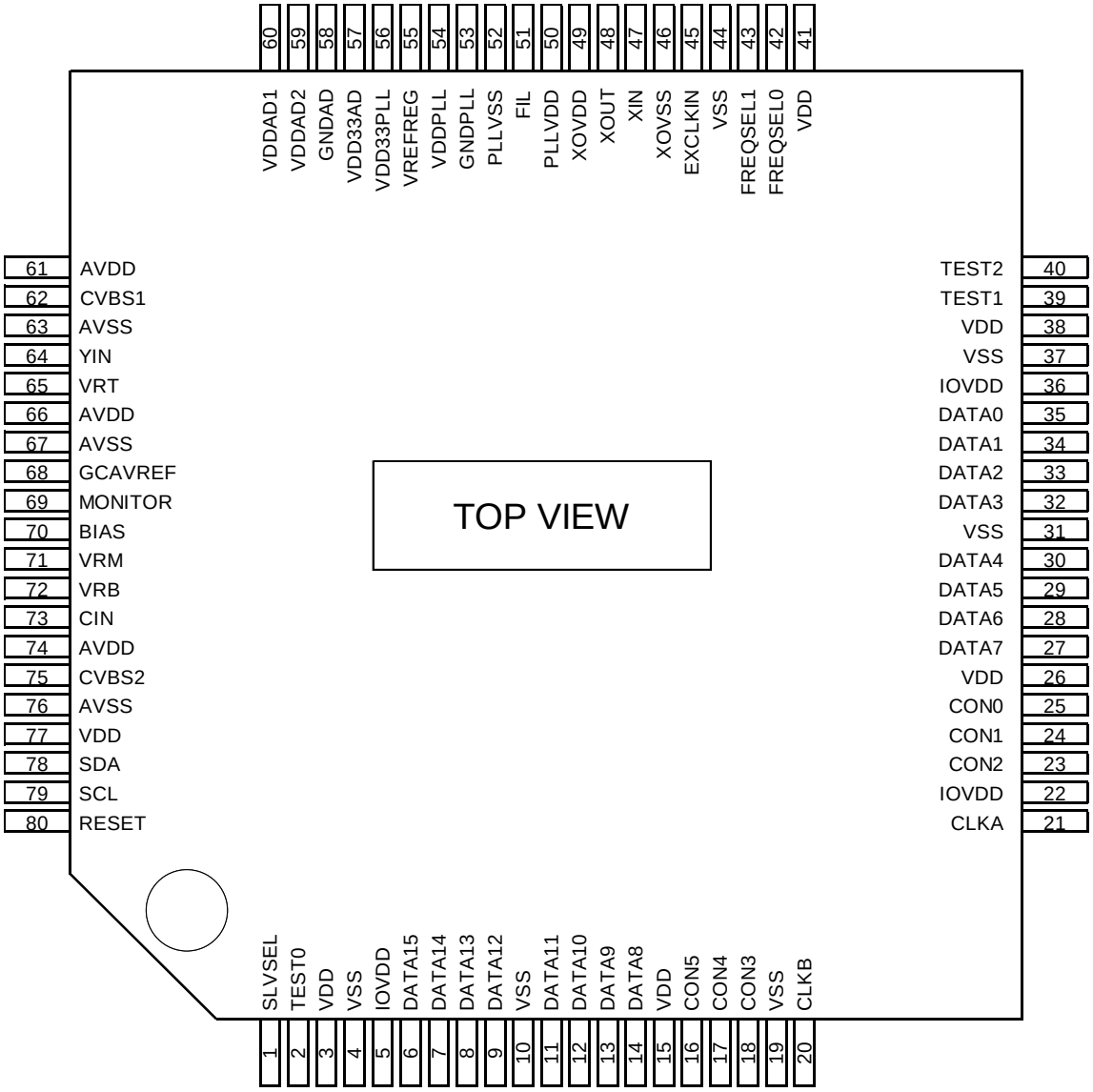
1. Features

1. Video input: CVBS, Y/C separate signal (S-Video)
2. Adaptive multi-standard detection / sync processing
3. Synchronous playback / Standard identification
4. 2ch 10bit ADC
5. Analog AGC (Sync AGC and Peak AGC) circuit built-in
6. LPF circuit for picture signal input built-in
7. Y/C separation : 3-line YCS (NTSC/PAL)
   Band Pass Filter. (SECAM)
8. Picture process Y : HVD-Enhancer, V-Enhance, LTI, Sharpness, Noise cancel, Contrast, Brightness,
   Dynamic Y-gamma correction, Static Y-gamma correction
   C : TOF, ACC, Color gain, CbCr offset, CTI, Noise cancel, Tint,
   CMC (Color Management),C gamma correction depended on Y-gamma correction
9. Feature functions : Level aberration correction
   VBI-Slicer (WSS/Video-ID/CC)
   S/N detection
10. Signal output : ITU-R BT.601 / ITU-R BT.656
11. I^2C-bus control
12. Regulator circuit (3.3 V input / 2.5 V output) built-in
13. Package : L-QFP 80 pin (0.50 mm pitch)
14. Power supply : 3.3 V, 2.5 V, 1.5 V
15. Operating templature : -40°C to 85°C

2. Block Diagram



3. Pin Layout


TOP VIEW
1 SLVSEL
2 TEST0
3 VDD
4 VSS
5 IOVDD
6 DATA15
7 DATA14
8 DATA13
9 DATA12
10 VSS
11 DATA11
12 DATA10
13 DATA9
14 DATA8
15 VDD
16 CON5
17 CON4
18 CON3
19 VSS
20 CLKB
21 CLKA
22 IOVDD
23 CON2
24 CON1
25 CON0
26 VDD
27 DATA7
28 DATA6
29 DATA5
30 DATA4
31 VSS
32 DATA3
33 DATA2
34 DATA1
35 DATA0
36 IOVDD
37 VSS
38 VDD
39 TEST1
40 TEST2
41 VDD
42 FREQSEL0
43 FREQSEL1
44 VSS
45 EXCLKIN
46 XOVSS
47 XIN
48 XOUT
49 XOVDD
50 PLLVDD
51 FIL
52 PLLVSS
53 GNDPLL
54 VDDPLL
55 VREFREG
56 VDD33PLL
57 VDD33AD
58 GNDAD
59 VDDAD2
60 VDDAD1
61 AVDD
62 CVBS1
63 AVSS
64 YIN
65 VRT
66 AVDD
67 AVSS
68 GCAVREF
69 MONITOR
70 BIAS
71 VRM
72 VRB
73 CIN
74 AVDD
75 CVBS2
76 AVSS
77 VDD
78 SDA
79 SCL
80 RESET

4. Pin Descriptions

Pin No.	Pin Name	Pin Type	Pin Function	Withstand voltage [V]	Circuit System	DC level of standard operation [V]
1	SLVSEL	IN	I^2C-BUS slave-address selector	3.3	Digital	-
2	TEST0	IN	Test terminal (Connect to GND)	3.3	Digital	3.3
3	VDD	DVDD	1.5 V power supply for Logic circuit	1.5	Digital	1.5
4	VSS	DVSS	GND for logic	0	Digital	0
5	IOVDD	IOVDD33	3.3 V power supply for I/O circuit	3.3	Digital	3.3
6	DATA15	OUT	Digital signal output 15bit	3.3	Digital	-
7	DATA14	OUT	Digital signal output 14bit	3.3	Digital	-
8	DATA13	OUT	Digital signal output 13bit	3.3	Digital	-
9	DATA12	OUT	Digital signal output 12bit	3.3	Digital	-
10	VSS	DVSS	GND for logic	0	Digital	0
11	DATA11	OUT	Digital signal output 11bit	3.3	Digital	-
12	DATA10	OUT	Digital signal output 10bit	3.3	Digital	-
13	DATA9	OUT	Digital signal output 9bit	3.3	Digital	-
14	DATA8	OUT	Digital signal output 8bit	3.3	Digital	-
15	VDD	DVDD	1.5 V power supply for Logic circuit	1.5	Digital	1.5
16	CON5	OUT	Timing pulse output 5	3.3	Digital	-
17	CON4	OUT	Timing pulse output 4	3.3	Digital	-
18	CON3	OUT	Timing pulse output 3	3.3	Digital	-
19	VSS	DVSS	GND for logic	0	Digital	0
20	CLKB	OUT	Bch Clock signal output	3.3	Digital	-
21	CLKA	OUT	Ach Clock signal output	3.3	Digital	-
22	IOVDD	IOVDD33	3.3 V power supply for I/O circuit	3.3	Digital	3.3
23	CON2	OUT	Timing pulse output 2	3.3	Digital	-
24	CON1	OUT	Timing pulse output 1	3.3	Digital	-
25	CON0	OUT	Timing pulse output 0	3.3	Digital	-
26	VDD	DVDD	1.5 V power supply for Logic circuit	1.5	Digital	1.5
27	DATA7	OUT	Digital signal output 7bit	3.3	Digital	-
28	DATA6	OUT	Digital signal output 6bit	3.3	Digital	-
29	DATA5	OUT	Digital signal output 5bit	3.3	Digital	-
30	DATA4	OUT	Digital signal output 4bit	3.3	Digital	-
31	VSS	DVSS	GND for logic	0	Digital	0
32	DATA3	OUT	Digital signal output 3bit	3.3	Digital	-
33	DATA2	OUT	Digital signal output 2bit	3.3	Digital	-
34	DATA1	OUT	Digital signal output 1bit	3.3	Digital	-
35	DATA0	OUT	Digital signal output 0bit	3.3	Digital	-
36	IOVDD	IOVDD33	3.3 V power supply for I/O circuit	3.3	Digital	3.3
37	VSS	DVSS	GND for logic	0	Digital	0
38	VDD	DVDD	1.5 V power supply for Logic circuit	1.5	Digital	1.5
39	TEST1	IN	Test terminal (Connect to GND)	3.3	Digital	3.3
40	TEST2	IN	Test terminal (Connect to GND)	3.3	Digital	3.3

Pin No.	Pin Name	Pin Type	Pin Function	Withstand voltage [V]	Circuit System	DC level of standard operation [V]
41	VDD	DVDD	1.5V power supply for Logic circuit	1.5	Digital	1.5
42	FREQSEL0	IN	Oscillator frequency change terminal 0	3.3	Digital	-
43	FREQSEL1	IN	Oscillator frequency change terminal 1	3.3	Digital	-
44	VSS	DVSS	GND for logic	0	Digital	0
45	EXCLKIN	IN	External clock input (27MHz)	3.3	Digital	-
46	XOVSS	XOVSS	GND for X'tal circuit	3.3	Digital	0
47	XIN	IN	Input for X'tal circuit	3.3	Digital	-
48	XOUT	OUT	Output for X'tal circuit	3.3	Digital	-
49	XOVDD	XOVDD	Power supply for X'tal circuit (2.5V recommendation, up to 3.3V)	3.3	Digital	2.5 or 3.3
50	PLLVDD	AVDD25	2.5V power supply for PLL circuit	2.5	Analog	2.5
51	FIL	OUT	VCO control voltage for clock	0	Analog	
52	PLLVSS	AVDD25	GND for PLL circuit	2.5	Analog	0
53	GNDPLL	AVSS	GND for regulator (PLL)	0	Analog	0
54	VDDPLL	OUT	2.5V power supply for regulator (for 2.5V PLL)	2.5	Analog	2.5
55	VREFREG	BIAS	Voltage relay for regulators	2.5	Analog	
56	VDD33PLL	AVDD33	3.3V analog power supply for regulator (for 3.3V PLL and XO)	3.3	Analog	3.3
57	VDD33AD	AVDD33	3.3V analog power supply for regulator (for 3.3V ADC)	3.3	Analog	3.3
58	GNDAD	AVSS	Analog GND for regulator (ADC)	0	Analog	0
59	VDDAD2	OUT	2.5V output for regulator (for 2.5V ADC)	2.5	Analog	2.5
60	VDDAD1	OUT	2.5V output for regulator (for 2.5V ADC)	2.5	Analog	2.5
61	AVDD	AVDD25	2.5V analog power supply for ADC / GCA circuit	2.5	Analog	2.5
62	CVBS1	IN	Composite video signal input 1	2.5	Analog	-
63	AVSS	AVSS	Analog GND for ADC / GCA circuit	0	Analog	0
64	YIN	IN	Y / Composite video signal input	2.5	Analog	-
65	VRT	BIAS	Reference top voltage for ADC	2.5	Analog	
66	AVDD	AVDD25	2.5V power supply for ADC / GCA circuit	2.5	Analog	2.5
67	AVSS	AVSS	Analog GND for ADC / GCA circuit	0	Analog	0
68	GCAVREF	BIAS	GCA output reference voltage	2.5	Analog	
69	MONITOR	OUT	Output terminal for TEST	2.5	Analog	-
70	BIAS	BIAS	Reference voltage for ADC	2.5	Analog	
71	VRM	BIAS	Reference middle voltage for ADC	2.5	Analog	
72	VRB	BIAS	Reference bottom voltage for ADC	2.5	Analog	
73	CIN	IN	C signal input	2.5	Analog	-
74	AVDD	AVDD25	2.5V analog power supply for ADC / GCA circuit	2.5	Analog	2.5
75	CVBS2	IN	Composite video signal input 2	2.5	Analog	-
76	AVSS	AVSS	Analog GND for ADC / GCA circuit	0	Analog	0
77	VDD	DVDD	1.5V power supply for Logic circuit	1.5	Digital	1.5
78	SDA	I/O	Data input / output for I^2C-BUS	5.0	Digital	-
79	SCL	IN	Clock input for I^2C-BUS	5.0	Digital	-
80	RESET	IN	System reset	5.0	Digital	3.3

5. Function

5.1 Overview

- TC90105FG is LSI in which two color decoders corresponding to a multi-system were carried.
- Carry out the color recovery of the two incoming signals simultaneously, and carry out a digital output in the format of ITU-R BT.601 or ITU-R BT.656.
  A digital output is carrying out multiplex processing, and it is possible to output two lines simultaneously.
  (8 bit of two line simultaneous outputs are possible for the time of an ITU-R BT.656 output)
- It has many image quality improvement functions, such as a HVD Enhancer, Dynamic γ correction, and Color management.
- Level scaler is built in and horizontal nonlinear extension can be performed.
- The VBI slicer function is carried and it is a Closed Caption (CC) / Video-ID / WSS is supported.
- The regulator circuit of 3.3V input 2.5V output is built in, and it can be used for power supply of ADC and PLL circuit. (When using it, terminal connection in IC exterior is required.)

5.2 Analog signal input

5.2.1 About an input signal

TC90105FG carries out a 2 line input for CVBS, and is carrying out 2ch built-in of 10bit ADC for the S-Video (Y/C) at an 1 lineinput.

The input dynamic range of ADC is designed by AVDD*0.4, and input dynamic ranges are useally 1.0 Vp-p (AVDD = 2.5 V).

Please give me the recommendation standard input amplitude as 0.7 Vp-p (0.7 time) in a 140 IRE input.

This IC carries the AGC function in the CVBS input. If an AGC function is used, it will attenuate to 0.7 Vp-p by 140 IRE, and will be inputted into ADC.

For this reason, when using an AGC function, it is possible to input amplitude by 1.0 Vp-p by 140 IRE at the time of a terminal input.

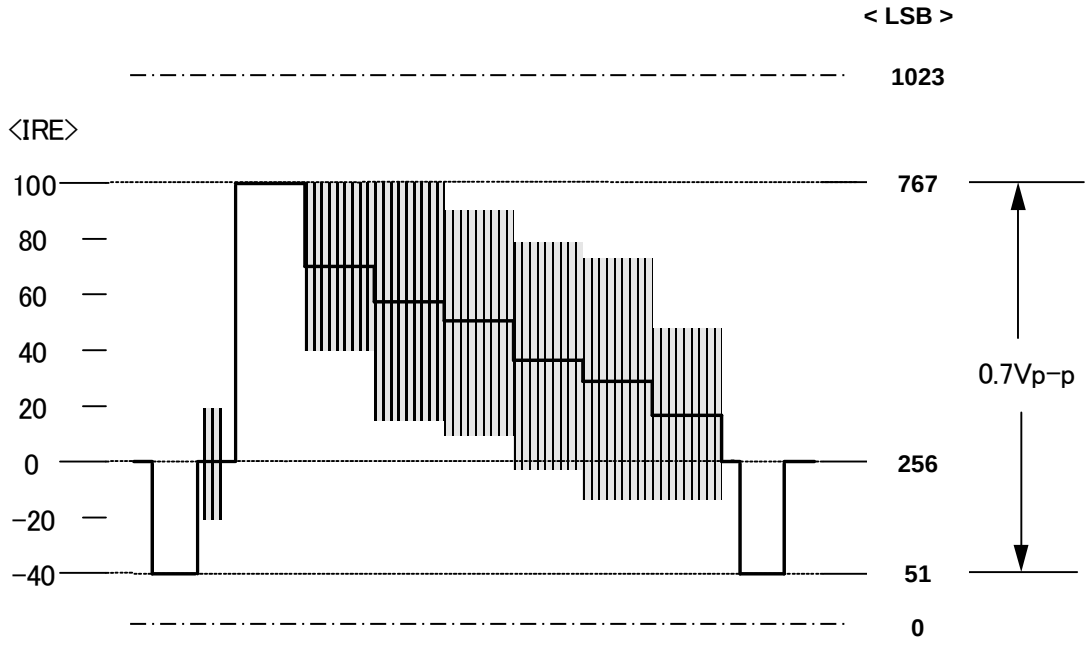
Clamp processing of the incoming signal is performing the pedestal clamp by sync feedback about the CVBS input and Y signal input of the S-Video.

C signal input of S-Video is performing bias to 128 LSB by internal bias.

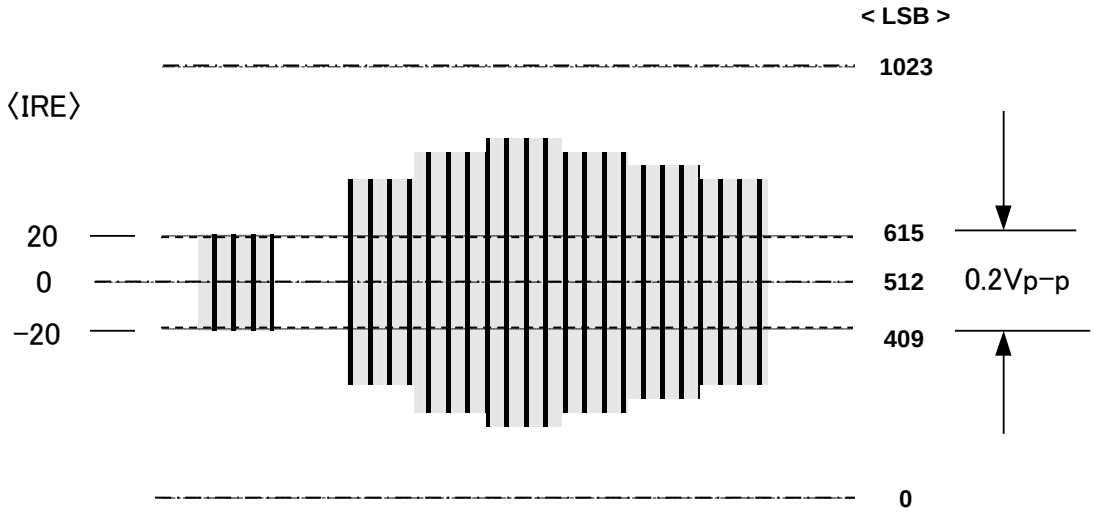
In addition, clamp processing by a digital system can be performed after an AD translation.

5.2.2 Input signal amplitude level

1) White 100% of CVBS signal or Y signal of S-Video standard input level.
(Ex. : CVBS signal input)



2) C signal of S-Video standard input level.



5.2.3 Input signal and pin list

The correspondence incoming signal format for every input terminal is indicated to the following tables.
An input terminal and corresponding core are also indicated simultaneously.

Correspondence Core	Signal format / Input terminal	CVBS	Y/C separate signal
Core-A	CVBS1	○	-
	YIN	○	○ (Y)
Core-B	CVBS2	○	-
	CIN	-	○ (C)

5.2.4 AGC (Auto Gain Control) function

GCA (Gain Control Amplifier) is built in, it is combination with a digital AGC function, and it is possible to use an AGC function to a CVBS input and Y input.
There are two kinds of AGC functions, AGC auto mode and manual gain mode.

If a GCA function is used, the 1.0 Vp-p standard input of CVBS will become possible.

5.2.5 LPF (Low Pass Filter) function

LPF for Anti-alasing is built in the preceding paragraph of GCA, and ON and through channel selection can be performed.

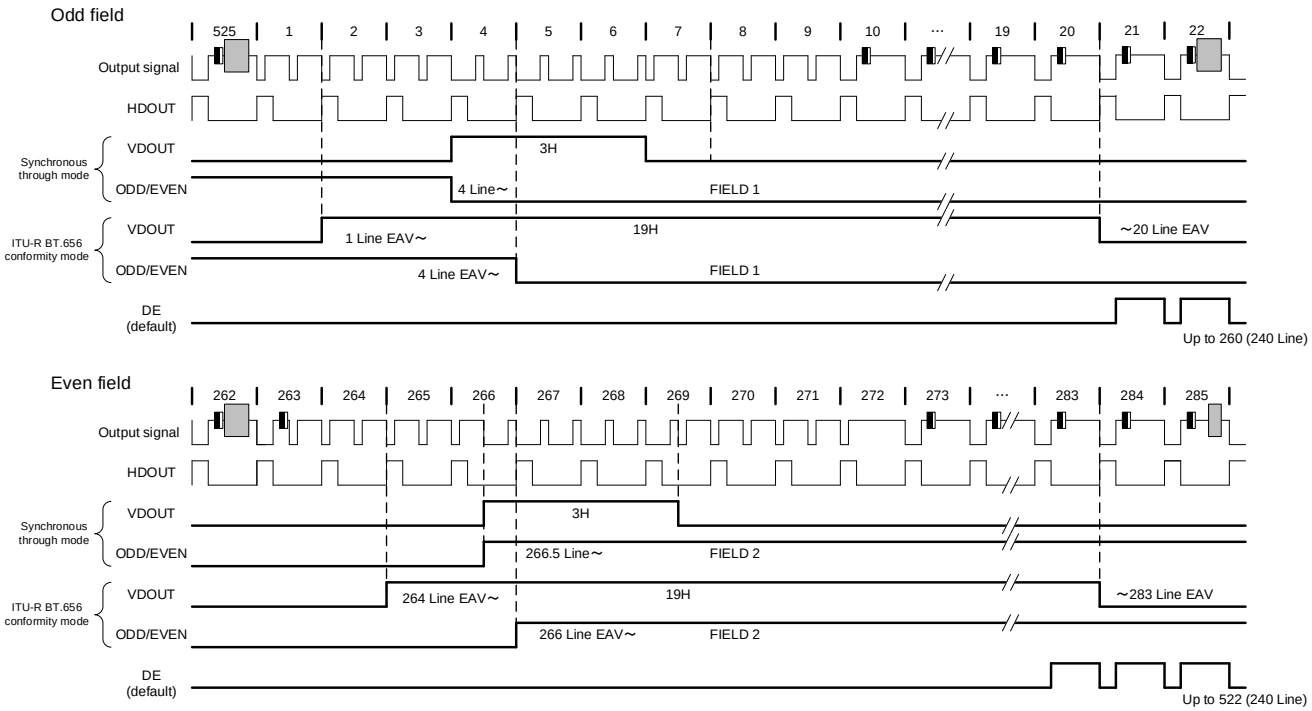
- System **:** 4th Butterworth filter
- Frequency characteristic **:** -1 dB @6 MHz, -14 dB @13.5 MHz (design value)

5.3 Digital signal output (Outsel Block)

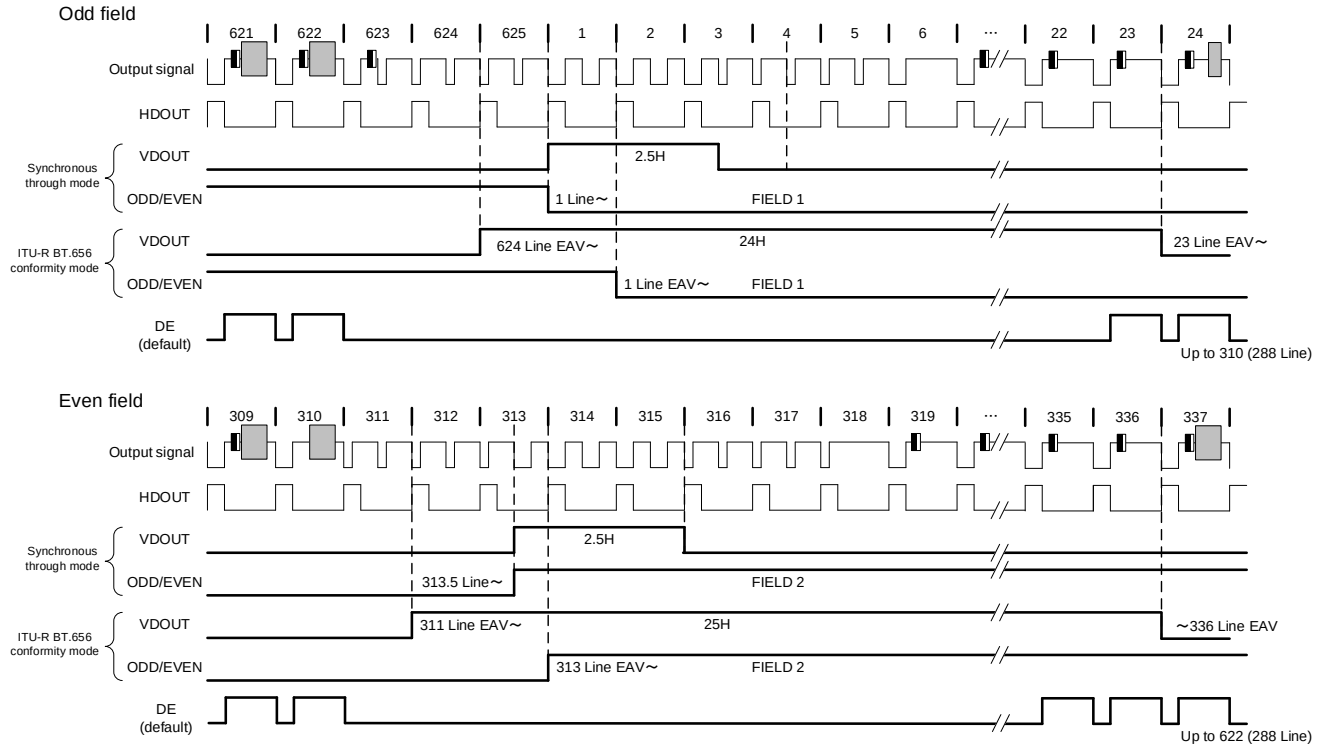
5.3.1 Output format

It outputs in the format of ITU-R BT.656 conformity or ITU-R BT.601 conformity.
The output format (ITU-R BT.656 / 601) is selected by register [601_656] (Seg0x00, Sub0x06).
Y: pedestal level = 16 LSB
C: center electric potential = 128 LSB

5.3.1.1. 525i/60Hz input



5.3.1.2. 625i/50Hz input



5.3.2 Multiplex processing output

In a two CVBS input, multiplex processing can be carried out and two outputs can be outputted.
Multiplex processing output becomes the same format from by two lines, although either of ITU-R BT.601 and ITU-R BT.656 of the formats is possible.

When multiplex processing is performed, a clock output has 6.5.2.1 Type1 and the two modes of 6.5.2.2 Type2.

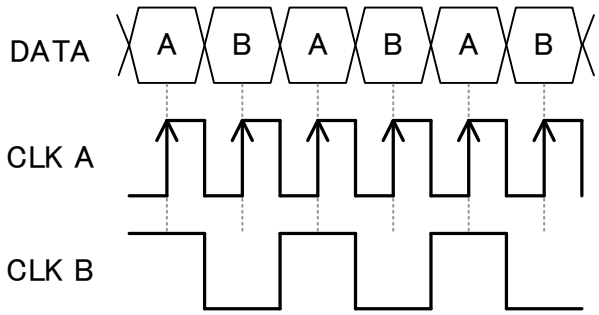
Type1 **:** The mode which outputs the flag of the output of which system in addition to the clock which carried out multiplex.

Type2 **:** The mode which outputs each clock.

5.3.2.1. Type1

It is the mode which outputs the data signal which acted as multiplex, the same clock signal of frequency, and the flag signal ofwhich system to output.

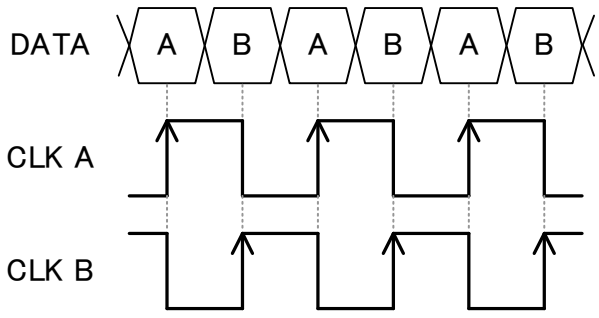
At the time of default configuration, a flag signal serves as a high output at the time of the output of CoreA (Segment 0x01), and serves as a low output at the time of the output of CoreB (Segment 0x02).



5.3.2.2. Type2

It is the mode which outputs the clock of two outputs from another terminal, respectively.

Since it acts as multiplex of the data signal, the clock signal in this mode is outputted on the frequency of the half of a data signal.



5.3.3 Timing pulse output

Following each signal of CoreA and CoreB is CON[5:0] (16 pin, 17 pin, 18 pin, 23 pin, 24 pin, 25 pin). It can choose and output to a terminal.

Output selection of each terminal is performed by [CON[5:0]] (Seg 0x00, Sub 0x08 to 0x0D).

1. DE (Data Enable) signal [CoreA / CoreB]
   The signal which shows the horizontal and vertical effective imaging range of an image display is outputted.
   A high level is an effective domain and the low level of DE signal is a blanking domain.

2. HD (Horizontal Definition) signal [CoreA / CoreB]
   The Horizontal synchronizing signal in sync with a display picture signal is outputted.
   Adjustment of width / polarity / phase can be set as arbitrary positions per pixel.

3. VD (Vertical Definition) signal [CoreA / CoreB]
   The Vertical synchronizing signal in sync with a display picture signal is outputted.
   Adjustment of width / polarity / phase can be set as arbitrary positions 1/4 unit.

4. FIELD signal [CoreA / CoreB]
   The field signal in sync with a display picture signal is outputted.
   The polarity of an output can be set up by [FLDO_POLE]. (CoreA: Seg0x01, Sub0x3C / CoreB: Seg0x01, Sub0x3C)
   At the time of default configuration, it is Even (high output) / Odd (Low output).

5. UVFLG signal [CoreA / CoreB]
   The flag signal of Cb / Cr of the output of 4:2:2 is outputted.
   The polarity of an output can be set up by [UVREV]. (CoreA : Seg0x01, Sub0x3B / CoreB : Seg0x01, Sub0x3B)
   At the time of default configuration, it is a high output at the time of Cb output.

6. NOSIG signal [CoreA / CoreB]
   The result of internal non signal detection is outputted.

7. VBI READY signal
   The VBI READY signal of the system by which input selection was mode is outputted to a VBI slicer.

5.4 Regulator circuit

Two regulator circuits of 3.3 V input 2.5 V output are built in the object for ADC circuits, and PLL circuits.

To use regulator output voltage, it is necessary to connect the output terminal of each regulator circuit to the power supply inputterminal of an ADC circuit and PLLcircuit in IC exterior.

In addition, please do not use the built-in regulator circuit other than the purpose of this IC operation.

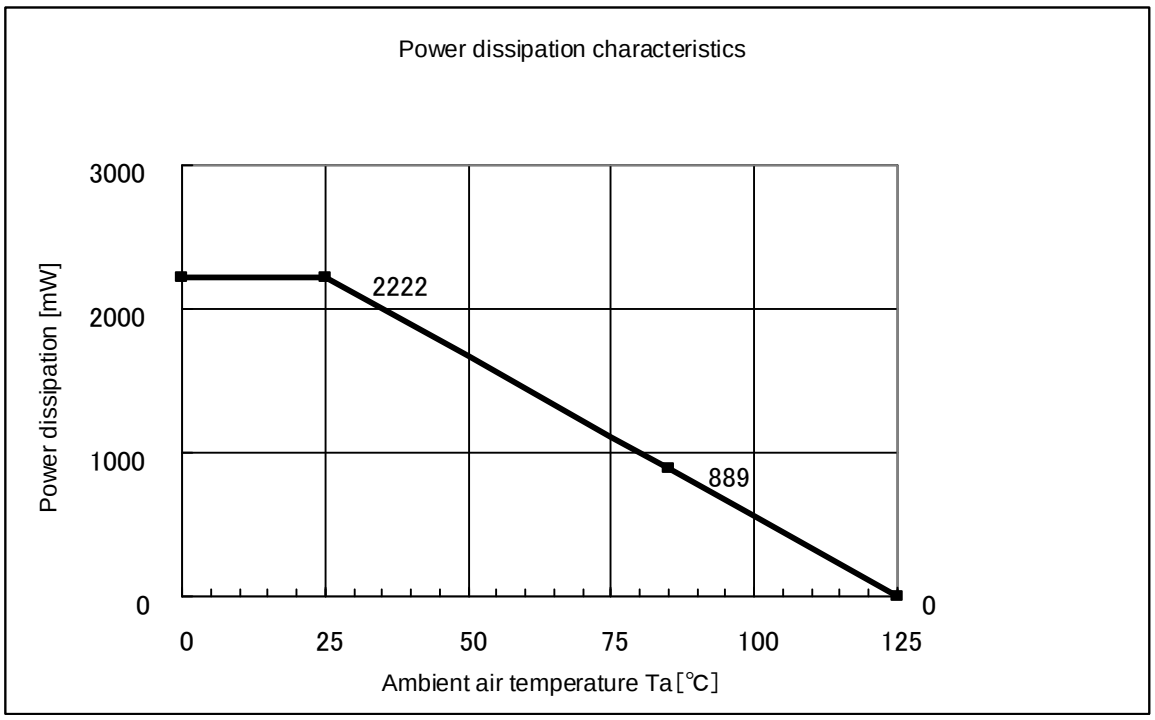
	Regulator circuit		Power supply input terminal
	Input terminal	Output terminal	
ADC circuit use	VDD33AD (57 pin)	VDDAD1 (60 pin) VDDAD2 (59 pin)	AVDD (61, 66, 74 pin)
PLL circuit use	VDD33PLL (56 pin)	VDDPLL (54 pin)	PLLVDD (50 pin) XOVDD (49 pin)

6. Absolute Maximum Ratings

The Absolute Maximum Ratings are rated values which must not be exceeded during operation, even for an instant. Exceeding the maximum rating may result in destruction, degradation or other damage to the IC and other components. When designing applications for this IC, be sure that none of the maximum rating values will ever be exceeded.

Characteristics	Terminal No.	Symbol	Rating	Unit
Power voltage1 (1.5 V system)	3, 15, 26, 38, 41, 77	VDD1	-0.3 to VSS + 2.0	V
Power voltage2 (2.5 V system)	49, 50, 61, 66, 74	VDD2	-0.3 to VSS + 3.5	V
Power voltage3 (3.3 V system)	5, 22, 36, 56, 57	VDD3	-0.3 to VSS + 3.9	V
Input voltage (2.5 V system)	47, 62, 64, 73, 75	VIN2	-0.3 to VDD2 + 0.3	V
Input voltage (3.3 V system)	1, 42, 43	VIN3	-0.3 to VDD3 + 0.3	V
Input voltage (3.3 V system, 5 V withstand voltage)	78, 79, 80	VIN4 (Note1)	-0.3 to VSS + 5.5	V
Potential difference between power pins (between 1.5 V system power pins)	-	ΔVDG1 (Note2)	0.3	V
Potential difference between power pins (between 2.5 V system power pins)	-	ΔVDG2 (Note2)	0.3	V
Potential difference between power pins (between 3.3 V system power pins)	-	ΔVDG3 (Note2)	0.3	V
Power dissipation	-	PD (Note3)	2222	mW
Storage temperature	-	Tstg	-40 to 125	°C

Note1: The withstand voltage for pins (SDA, SCL, RESET) is 5 V.
Note2: For each of 1.5 V and 2.5 V and 3.3 V, system power supply terminal is made into the same voltage.
The maximum potential difference should not exceed rating for all power supply terminals then.
In addition, potential difference between all VSS terminal must be under 0.01 V in this status. .
Note3: If you intended to use a temperature higher than Ta = 25°C, reduce by 22.22 mW per one degree (°C) increase.



7. Operating Ranges

The TC90105FG is not guaranteed to function correctly if it is used outside its specified power voltage rage (1.5 V system power**:** 1.40 V to 1.60 V, 2.5 V system power**:** 2.3 V to 2.7 V, 3.3 V system power**:** 3.0 to 3.6 V). Please use within the specified operating conditions.

If you temporarily leave and then return to the specified operating conditions, this IC's conditions will change, and so it is necessary to reset the IC's power to continue using it correctly within the specified operating conditions.

Characteristics	Terminal No.	Symbol	Min	Typ.	Max	Unit
Power voltage of digital block	3, 15, 26, 38, 41, 77	VDD-D	1.4	1.5	1.6	V
Power voltage of I/O block (*1)	5, 22, 36	VDD-IO	3.0	3.3	3.6	V
Power voltage of regulator block (*1)	56, 57	VDD-REG	3.0	3.3	3.6	V
Power voltage of XO block (*2)	49	VDD-XO	2.3	2.5	3.6	V
Power voltage of PLL block (*3)	50	VDD-PLL	2.3	2.5	2.7	V
Power voltage of analog block (*3)	61, 66, 74	VDD-AD	2.3	2.5	2.7	V
Operating temperature	-	Topr	-40	-	85	°C

(*1) If possible, please set I/O power supply voltage and regulator power supply voltage into the potential.

(*2) When you connect XO power supply to 2.5 V power supply, if possible, please use the potential with PLL power supply voltage and analog power supply voltage.
Although connecting with 3.3 V power supply is also possible, please set I/O power supply voltage and regulator power supply voltage as the potential in that case.
Recomendded input voltage is 2.5V at 49 terminal, but it is available for 3.3V input voltage.

(*3) If possible, please set PLL power supply voltage and analog power supply voltage into the potential.

8. Electrical characteristic

8.1 DC characteristic

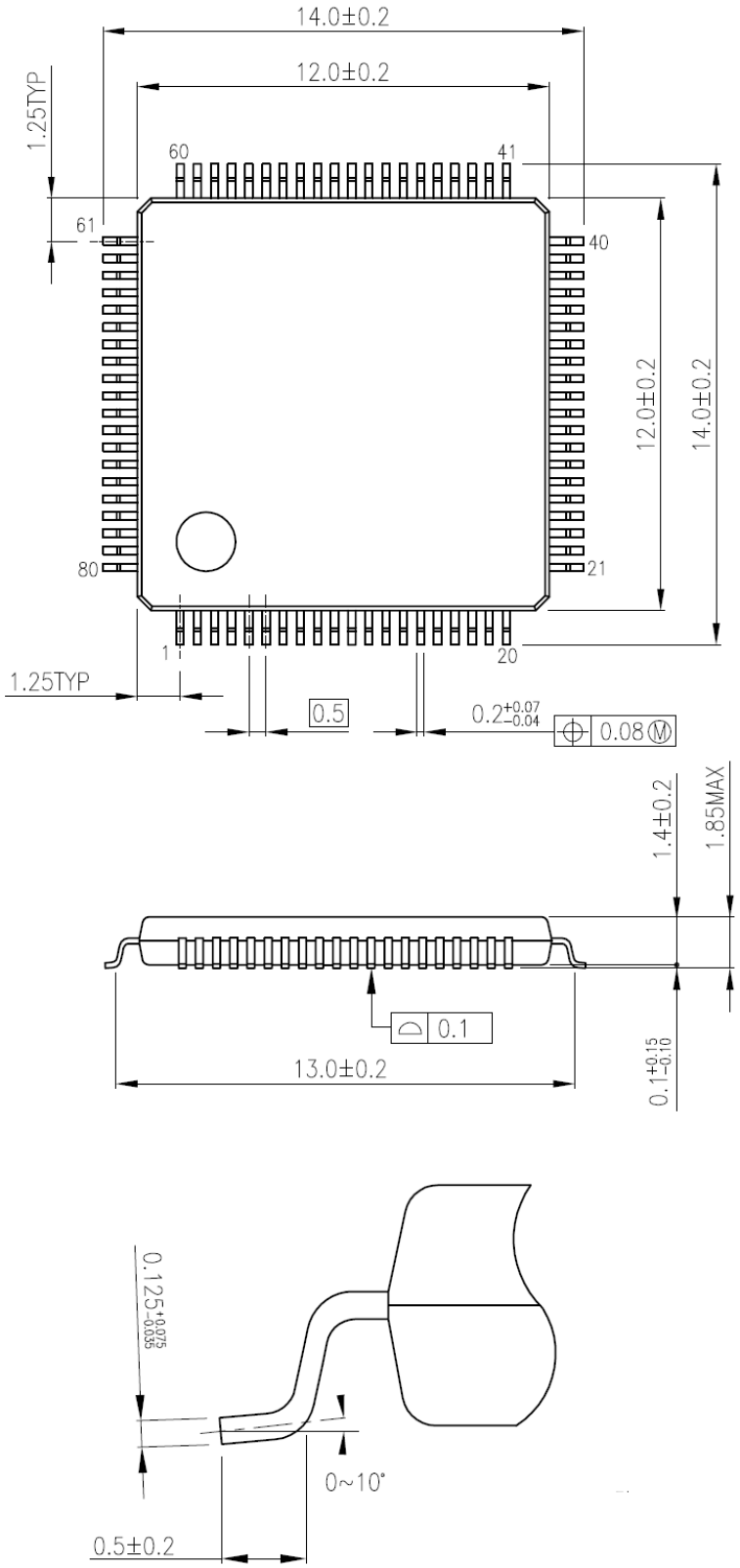
(Ta = 25°C, VDD1 = 1.50 V ± 0.1 V, VDD2 = 2.50 V ± 0.2 V, VDD3 = 3.30 V ± 0.3 V)

Characterisitc	Terminal No.	Symbol	Min	Typ.	Max	Unit	Note
Power supply current (*4)	3, 15, 26, 38, 41, 77	IDD1 (1.5 V system)	-	-	150	mA	
	49, 50, 61, 66, 74	IDD2 (2.5 V system)	-	-	150	mA	When a built-in regulator was not used but 2.5 V power supply is supplied from the out side.
	5, 22, 36, 56, 57	IDD3-1 (3.3 V system)	-	-	50	mA	When a built-in regulator was not used but 2.5 V power supply is supplied from the out side.
		IDD3-2 (3.3 V system)	-	-	170	mA	When a built-in regulator is used.
Input voltage	1, 42, 43, 45	VIH	VDD3 x 0.8	-	VDD3	V	I/O input terminal of 3.3 V system.
	78, 79, 80						I/O input terminal of 5.0 V system.
	1, 42, 43, 45	VIL	VSS	-	VDD3 x 0.2	V	I/O input terminal of 3.3 V system.
	78, 79, 80						I/O input terminal of 5.0 V system.
Input current	1, 42, 43, 45	IIH	-10	-	10	μA	I/O input terminal of 3.3 V system.
	78, 79, 80						I/O input terminal of 5.0 V system.
	1, 42, 43, 45	IIL	-10	-	10	μA	I/O input terminal of 3.3 V system.
	78, 79, 80						I/O input terminal of 5.0 V system.
Output voltage	6, 7, 8, 9, 11, 12, 13, 14, 16, 17, 18, 20, 21, 23, 24, 25, 27, 28, 29, 30, 32, 33, 34, 35	V_{OH}	VDD3 - 0.6	-	VDD3	V	I/O output terminal of 3.3 V system. When load current: -4 mA
		V_{OL}	VSS	-	0.4	V	I/O output terminal of 3.3 V system. When load current: +4 mA

(*4) Power consumption (W) changes the calculation method by whether a built-in regulator is used or it is not used.
When a built-in regulator is used : Sum total of IDD1 and IDD3-2
When a built-in regulator is not used : Sum total of IDD1, IDD2, and IDD3-1

9. Package

LQFP80-P-1212-0.50F Unit : mm



Weight: 0.50 g (Typ.)

10. Revision History

Date	Revision	Contents
2015/11/11	1.00	First edition

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