

SANYO Semiconductors DATA SHEET

An ON Semiconductor Company

LC08101CT -

Shaft Slide Actuator Driver IC

Overview

The LC08101CT is a Shaft Slide Actuator Driver IC.

Features

The shaft slide actuator can be driven simply by I²C communication.

Constant current control is exercised for the output of the supply to suppress the fluctuation in the coil current due to the temperature fluctuations.

- The drive conditions can be set externally using serial input through the I²C interface. The kick-pulse width and brake-pulse width are set using the clock count.
- ENIN input that controls the startup/stop of the IC.
- The time for which the actuator is driven is determined with the drive frequency setting based on I²C communication.
- Provides a busy signal output during periods when the actuator is being driven by OUT pin output so that applications can be aware of the actuator operating/stopped state.
- Built-in oscillator circuit (1 MHz typical). Capable of switching to an external clock.
- Separate drive waveforms can be set in steps, i.e., when the actuator is activated, stopped and subjected to braking.
- Built-in thermal protection function, reduced voltage detection/protection circuits, and register power-on reset function

Specifications

Absolute Maximum Ratings at $Ta = 25^{\circ}C$, SGND = PGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V _{CC} max		-0.5 to 4.0	V
Output current	I _O max		300	mA
Input signal voltage	V _{IN} max	SCL/SDA/CLK/WP	-0.5 to V _{CC} +0.5	V
Allowable power dissipation	Pd max	*Mounted on a specified board.	650	mW
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

*: When mounted on the specified printed circuit board (50mm ×50mm ×1.6mm), glass epoxy board

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

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LC08101CT

Allowable Operating Conditions at $Ta = 25^{\circ}C$, SGND = PGND = 0V

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VCC		2.2 to 3.6	V
Input signal voltage	VIN		-0.3 to V _{CC}	V
Corresponding CLK input frequency	Fclk		to 60	MHz
Maximum operating frequency	Ct max		Set STP count × 512	Times

Electrical Characteristics at Ta = 25° C, V_{CC} = 2.8V, SGND = PGND = 0V, unless otherwise specified.

Deremeter	Cumbal	Conditions			Unit	
Parameter	Symbol	Conditions	min	typ	max	Unit
Standby mode current drain	ICC0	CLK/SCL/SDA=0V, When ENIN=0			1.0	μA
Operating mode current drain for	I _{CC} 1	Internal oscillator movement SCL/SDA=0,		0.65	1.0	mA
driber area		When ENIN=1				
High-level input voltage	VIH	$2.2V \leq V_{CC} \leq 3.3V \text{ SCL}, \text{ SDA}$	1.4		V _{CC} +0.3	V
Low-level input voltage	VIL	$2.2V \leq V_{CC} \leq 3.3V \text{ SCL}, \text{ SDA}$	-0.3		0.3	V
CLK pin high-level input voltage	V _{IH} 2	CLK	0.45×V _{CC}		V _{CC} +0.3	V
CLK pin low-level input voltage	V _{IL} 2	CLK	-0.3		0.2×V _{CC}	V
Internal oscillator dispatch frequency	Fclk	It is calculated by an output wave pattern	0.80	0.95	1.20	MHz
Output constant current	I _O C1	I _{OUT} register D3 to D0 = 1010	95	105	115	mA
	I _O C2	I _{OUT} register D3 to D0 = 0000	190	210	230	mA
Reduced voltage protection detection voltage	Vres	V _{CC} voltage	1.8	2.0	2.2	V
Output block upper-side on resistance	RonP	I include a current current sense resistor		1.35	1.545	Ω
Output block lower-side on resistance	RonN			0.4	0.55	Ω
Turn on time	TPLH	With no load *1		0.1	0.25	μS
Turn off time	TPHL	With no load *1		0.03	0.1	μS

*1 : Rising time from 10 to 90% and falling time from 90 to 10% are specified with regard to the OUT pin voltage.

Package Dimensions

unit : mm (typ) 3423





Pin Assignment



Тор	view	
В	А	
CLK	SCL	1
SGND	SDA	2
Vcc	OUT1	3
OUT2	PGND	4

A1:CLK	B1:CLK
A2:SDA	B2:SGND
A3:OUT1	B3:VCC
A4:PGND	B4:OUT2

Block Diagram



Serial Bus Communication Specifications

I²C serial transfer timing conditions



Standard mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0	-	100	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	4.7	-	-	μs
	ts2	Setup time of SDA with respect to the rising edge of SCL	250	-	-	ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	4.0	-	-	μs
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	4.0	-	-	μs
	th2	Hold time of SDA with respect to the falling edge of SCL	0.06	-	-	μs
Pulse width	twL	SCL low period pulse width	4.7	-	-	μs
	twH	SCL high period pulse width	4.0	-	-	μs
Input waveform conditions	ton	SCL/SDA (input) rising time	-	-	1000	ns
	tof	SCL/ SDA (input) falling time	-	-	300	ns
Bus free time	tbuf	Interval between stop condition and start condition	4.7	-	-	μs

High Speed mode

Parameter	symbol	Conditions	min	typ	max	unit
SCL clock frequency	fscl	SCL clock frequency	0	-	400	kHz
Data setup time	ts1	Setup time of SCL with respect to the falling edge of SDA	0.6	-	-	μS
	ts2	Setup time of SDA with respect to the rising edge of SCL	100	-	-	ns
	ts3	Setup time of SCL with respect to the rising edge of SDA	0.6	-	-	μS
Data hold time	th1	Hold time of SCL with respect to the rising edge of SDA	0.6	-	-	μS
	th2	Hold time of SDA with respect to the falling edge of SCL	0.06	-	-	μS
Pulse width	twL	SCL low period pulse width	1.3	-	-	μS
	twH	SCL high period pulse width	0.6	-	-	μS
Input waveform conditions	ton	SCL/SDA (input) rising time	-	-	300	ns
	tof	SCL/ SDA (input) falling time	-	-	300	ns
Bus free time	tbuf	Interval between stop condition and start condition	1.3	-	-	μS

I²C bus transfer method

Start and stop conditions

The I²C bus requires that the state of SDA be preserved while SCL is high as shown in the timing diagram below during a data transfer operation.



When data is not being transferred, both SCL and SDA are in the high state. The start condition is generated and access is started when SDA is changed from high to low while SCL and SDA are high.

Conversely, the stop condition is generated and access is ended when SDA is changed from low to high while SCL is high.



Data transfer and acknowledgement response

After the start condition is generated, data is transferred one byte (8 bits) at a time. Any number of data bytes can be transferred consecutively.

An ACK signal is sent to the sending side from the receiving side every time 8 bits of data are transferred. The transmission of an ACK signal is performed by setting the receiving side SDA to low after SDA at the sending side is released immediately after the clock pulse of SCL bit 8 in the data transferred has fallen low.

After the receiving side has sent the ACK signal, if the next byte transfer operation is to receive only the byte, the receiving side releases SDA on the falling edge of the 9th clock of SCL.

There are no CE signals in the I²C bus ; instead, a 7-bit slave address is assigned to each device, and the first byte of the transfer data is allocated to the 7-bit slave address and to the command (R/W) which specifies the direction of subsequent data transfer.

The READ function of the LC08101CT Driver area provides only the functionality to test the BUSY state.

7-bit address data is transferred sequentially starting at the MSB and the second and subsequent bytes are written if the state of the 8th bit is low and read if the state is high.

In the LC08101CT Driver area, the slave address is stipulated to be "1110010."

WRITE mode timing



READ mode timing



Data transfer write format

The slave address and Write command must be allocated to the first byte and the register address in the serial map must be designated in the second byte.

For the third byte, data transfer is carried out to the address designated by the register address which is written in the second byte. Subsequently, if data continues, the register address value is automatically incremented for the fourth and subsequent bytes.

Thus, continuous data transfer starting at the designated address is made possible.

After the register address reaches 1Fh, the transfer address for the next byte is set to 00h.

Data write example



Driver area Serial Map

			R	egister	Addres	SS						Da	ata			
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	0	M/I			DF	RVPULSE[6	:0]		
0									0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	1	×	×	ENIN	CKSE	L[1:0]	INCL	K[1:0]	BRON
1									0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	0				RST	[7:0]			
2									0	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	1				GTAS	S[7:0]			
3									0	0	0	0	0	0	0	0
	0	0	0	0	0	1	0	0				STP	[7:0]			
4									0	0	0	0	0	0	0	0
	0	0	0	0	0	1	0	1	TEST	F[1:0]	SW1	SW2		IOUT	[3:0]	
5									0	0	0	0	0	0	0	0
	0	0	0	0	0	1	1	0		r		TBRA	<e[7:0]< td=""><td></td><td>r</td><td>r</td></e[7:0]<>		r	r
6									0	0	0	0	0	0	0	0
	0	0	0	0	0	1	1	1	×	×			NRPUL	SE1[5:0]		
7									0	0	0	0	0	0	0	0
	0	0	0	0	1	0	0	0	×	×		-	NRP-	A[5:0]		
8	0	0	0	0	4	0	0	4	0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0	1	×	×	0	0	NRP-	B[5:0]	0	0
9	0	0	0	0	1	0	1	0	0	0	0	0			0	0
10	0	0	0	0		0	1	0	×	×	0	0	0	0	0	0
10	0	0	0	0	1	0	1	1	×	×	0	0	NRP-	D[5:0]	0	0
11	0	Ŭ	Ũ	Ŭ		Ŭ			0	0	0	0	0	0	0	0
	0	0	0	0	1	1	0	0	×	×		Ū	NRPUL	SE2[5:0]	Ū	Ŭ
12	-		-				-		0	0	0	0	0	0	0	0
	0	0	0	0	1	1	0	1	×	×			NRP-	E[5:0]		
13									0	0	0	0	0	0	0	0
	0	0	0	0	1	1	1	0	×	×			NRP-	F[5:0]		
14									0	0	0	0	0	0	0	0
	0	0	0	0	1	1	1	1	×	×			NRP-	G[5:0]		
15									0	0	0	0	0	0	0	0
	0	0	0	1	0	0	0	0	×	×			NRP-	H[5:0]		
16									0	0	0	0	0	0	0	0
	0	0	0	1	0	0	0	1	×	×	ļ,		NRPUL	SE3[5:0]		
17									0	0	0	0	0	0	0	0
	0	0	0	1	0	0	1	0	×	×			NRP	·I[5:0]	[[
18									0	0	0	0	0	0	0	0
	0	0	0	1	0	0	1	1	×	×			NRP-	J[5:0]		
19		_							0	0	0	0	0	0	0	0
	0	0	0	1	0	1	0	0	×	×		-	NRP-	K[5:0]	-	_
20	-				6				0	0	0	0	0	0	0	0
0 4	υ	U	U	1	U	1	υ	1	×	×		0	NKP-	ւլ5:0]	0	0
∠1	0	0	0	4	0	1	1	0	0	0	U	U			U	U
22	U	U	U		U		I	U	×	×	0	0		5⊑4[5:0] ∩	0	0
22				egisto-	Addree				0	0	0		U	0	0	0
			ň	eyistel	Audies	55						Da	ud			

Upper : Register name Lower : Default value

Continued on next page.

Contin	ued fr	om pre	eceding	g page												
			R	egister	Addre	SS						Da	ata			
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	1	0	1	1	1	×	×			NRP-	M[5:0]		
23									0	0	0	0	0	0	0	0
	0	0	0	1	1	0	0	0	×	×			NRP-	N[5:0]		
24									0	0	0	0	0	0	0	0
	0	0	0	1	1	0	0	1	×	×			NRP-	O[5:0]		
25									0	0	0	0	0	0	0	0
	0	0	0	1	1	0	1	0	×	×			NRP	P[5:0]		
26									0	0	0	0	0	0	0	0
	0	0	0	1	1	0	1	1				NR1G1	AS[7:0]			
27									0	0	0	0	0	0	0	0
	0	0	0	1	1	1	0	0				NR2G1	AS[7:0]			
28									0	0	0	0	0	0	0	0
	0	0	0	1	1	1	0	1			1	NR3G1	AS[7:0]	1		
29									0	0	0	0	0	0	0	0
	0	0	0	1	1	1	1	0			1	NR4G1	AS[7:0]	1		
30									0	0	0	0	0	0	0	0
	0	0	0	1	1	1	1	1		1	1	NR5G1	AS[7:0]	1	1	1
31									0	0	0	0	0	0	0	0
			READ) mode	only re	egister			BUSY	×	×	×	×	×	×	×
32															0	
			R	egister	Addre	SS			Data							

Upper : Register name Lower : Default value

NR pulse output

Rise-time operation



If, as an example, the NRPULSE1 setting is set to 15, the NRP-A setting is set to 3, the NRP-B setting is set to 6, the NRP-C setting is set to 9 and the NRP-D setting is set to 12, then after the NR1 waveform is output for three periods, the NR2 waveform for three periods, the NR3 waveform for three periods, the NR4 waveform for three periods and the NR5 waveform for three periods, the standard waveform is output for a period equivalent to the STP x DRVPULSE period.

When the NRPULSE setting is set to 0, the same output as the normal DRVPULSE input without the NR pulses is performed.

When the same value has been set for NRP-A and NRP-B, the NR2 waveform is not output, and the NR3 waveform is output after the NR1 waveform.

Fall-time operation



During the fall-time operation, the waveforms are output in sequence from the NR5 waveform to the NR1 waveform. The method used to set the switching timing is the same as for the rise-time operation.

NR drive waveform settings

The settings are the same as for the normal drive waveform. The same parameter as for the normal waveform is used for RST, and for GTAS the drive waveform is generated using the setting values for the NR waveforms.



NR pulse output when the brake is set



When the brake output has been set, a pulse equivalent to the TBRAKE frequency is output as the brake pulse in the reverse direction after the standard waveform has been output. If the NR settings are to be established, NR pulses can be set separately for the rise and fall of the standard waveform and the rise and fall of the brake waveform. When the brake setting is not to be established (when the BRON register is set to 0), the pulse is not output in the reverse direction so it is not output even when values have been set for NRPULSE3 and NRPULSE4.

S

	0	0		0	0	0	0	0	0	D7	D6	D5	D4	D3	D2	D1	D
	D0 t	o Dé	5: DR	VP	ULSE	[6:0]									•		
	0	pera	tion c	our	nt settir	ng regis	ter. Sp	ecify a r	number	from 0	to 127.						
	Tl	he ni	ımbe	r of	cyclic	operati	ons de	termine	d by <l< td=""><td>ORVPL</td><td>USE se</td><td>tting></td><td>× <sti< td=""><td>setting</td><td>g> are p</td><td>erform</td><td>ed.</td></sti<></td></l<>	ORVPL	USE se	tting>	× <sti< td=""><td>setting</td><td>g> are p</td><td>erform</td><td>ed.</td></sti<>	setting	g> are p	erform	ed.
	A	dditi	onal	data	a can b	e input	and da	ta is ado	led up	to the e	quivale	nt of to	tal of 5	12 puls	ses.		
	H	owe	ver, i	f th	e ENIN	V regist	er is se	et to 0, 1	the DR	VPULS	E input	t is not	accept	ted beca	ause the	e DRVI	PUI
	cc	ounte	er is i	n th	e reset	state.											
	Si	nce	the o	utpi	ut oper	ation is	carrie	d out at	the tin	ne the D	DRVPU	LSE in	put is r	recogniz	zed, the	genera	atio
	th	e Ol	JT SI	gna	l is sta	rted at	the tin	he an A	CK SIE	nal 15 g	generate	d after	the ex	ecution	1 of the	instruc	ctio
	ac	lares	s 001	1 ac	cordin	g to the	value	of the v	vavetoi	m setup	o registe	er estat	lished	at that 1	time.		
	07		4/1					Oper	ation d	irection	switch	inσ					
	0/	1	vi/1					*Def	auon u Sault	nection	Switch	ing	Inf	inity di	stance	lirectio	n
	1		nacro					Der	aun				Ma	cro dire	ection	meeno	11
		ntio	n dire	oti	on antit	ohina r	agistar						IVIC		cetion		
	Uper T1		n une serati		ount s	etting r	egister	is reset	when	the reai	stor is s	witche	d To e	ton the	operati	on of t	hoi
	50	vitch	the 1	M/I	registe	er and so	of DRV		$t_0 0 f_0$	or input	5101 15 5	witche	u. 10 s	top the	operati	011 01 11	
	31	vitei	i une i	VI/ I	registe	a unu so		TOLDI	1001	n mput	•						
			-					T	1				1	-	1		1
L	0	0		0	0	0	0	0	1	0	0	D5	D4	D3	D2	D1	
	DC) [BRON					Initia	alizatio	n to be	perform	ned/not	to be p	perform	ed setti	ng	
) [BRON	<i>(</i> 0				Initia *Def	alizatio	n to be	perform	ned/not	to be p	perform	ed setti	ng	
	0		BRON No bral	ke				Initia *Def	alizatio Fault	n to be	perform	ned/not	to be p	perform	ed setti	ng	
	0 1) [BRON No bral On bral	ke ke				Initia *Def	alizatio Fault	n to be	perform	ned/not	to be p	perform	ed setti	ng	
	0 1) 	BRON No bral On bral The t	ke ke	ster wł	no sets t	frequer	Initia *Def	alizatio Fault	n to be	perform	ned/not	to be p	operate	ed setti	ng rmal os	cill
	DI, Circu) 	BRON No bral On bral The 1	ke regi	ster wł	no sets 1	frequer	Initia *Def	alizatio fault ne osci	n to be	perform	ned/not cy whe	to be p en you	oerform	ed setti an inte	ng ernal os	cill
	D1, D2	D2:	BRON No bral On bral The 1 D1	ke regi	ster wh	no sets i	frequer	Initia *Def ncy of th Num	alizatio Fault ne osci ber of	n to be llatory f	perform frequend ation se	ned/not cy whe	to be p en you e swing	operate back	an inte	ng rnal os	cill
	0 1 D1, 1 circu D2 0	D2: nit.	BRON No brai Dn brai The 1 D1 0	ke regi IN(ster wł CLK cillator si	io sets t	frequer	Initia *Def ncy of th Num *Def	alizatio Fault ne osci ber of Fault	n to be llatory f	perform frequent ation se	ned/not cy whe	to be p n you e swing	operform operate ; back	an inte	ng ernal os	cill
	0 0 1 D1, 1 circu D2 0 0	D2: uit.	BRON No bral Dn bral The r D1 0 1	ke Tegi IN(Os	ster wh CLK cillator si	no sets i	frequer	Initia *Def ncy of th Num *Def	alizatio fault ne osci ber of fault	n to be llatory f	perform frequend ation se	ned/not cy whe	to be p on you e swing	operform operate ; back	ed setti an inte	ng rnal os	cill
	D1, 1 D1, 2 Circu D2 0 0	D2: uit.	BRON No bral Dn bral The r D1 0 1 0	ke regi IN(Os 1.0	Ster wł CLK cillator si j2MHz IHz	no sets : top	frequer	Initia *Def ncy of tl Num *Def	alizatio Fault ne osci ber of Fault	n to be llatory f	perform frequent ation se	ned/not cy whe	to be p on you e swing	operform operate ; back	ed setti	ng rnal os	cill
	D1, D1, Circu D2 0 0	D2: uit.	ARON No bral Dn bral The T D1 0 1 0 1	ke regi Os 1.0 1N 0.9	Ster wł CLK cillator si p2MHz IHz p8MHz	no sets t top	frequer	Initia *Def ncy of tl Num *Def	alizatio fault ne osci ber of fault	n to be	perform frequent ation se	ned/not	to be p n you e swing	operate back	ed setti	ng rnal os	cill
	D1, 1 D1, 1 Circu D2 0 1 1) 	A brain and a brai	ke regi Os 1.0	ster wh CLK cillator s 2MHz IHz 8MHz	no sets t	frequer	Initia *Def ney of th Num *Def	alizatio fault ne osci ber of fault	n to be	perform frequent ation se	ned/not	to be p en you e e swing	operate back	ed setti	ng rnal os	cill
	D1, D1, circu D2 0 0 1 1 D3, 1	D2: iit. D2: D2: D4: 1	ARON No brai Dn brai The r D1 0 1 0 1 Regis	ke regi No 1.0 1.0 0.9 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0	ster wh CLK cillator si p2MHz IHz p8MHz (when	no sets t	frequer	Initia *Def ney of tl Num *Def al oscill	alizatio fault ne osci ber of fault ation in	n to be llatory f initializ	perform frequent ation se	ned/not cy whe equence sets the	to be p en you e swing e ratio t	operate back	an inte	ng rnal os	cill I co
	D1, D1, circu D2 0 1 1 D3, it in	D2: D2: iit. D4: 1 D4: 1 a clo	ARON No brai Dn brai Dn brai D1 0 1 0 1 Regis	ke regi INK Os 1.C 1N 0.S ter ulse	ster wł CLK cillator si p2MHz IHz 98MHz (when input	top I use an into CL	frequer intern K pin o	Initia *Def ncy of th Num *Def al oscill or the IQ	alizatio fault ne osci ber of fault ation in C inside	n to be llatory f initializ nvalidit <u>:</u> e as bas	perform frequent ation se y) who so	ned/not cy whe equence sets the	to be p on you e swing	operform operate ; back o do a s	an inte	ng rnal os o when	cill I co
	D1, D1, circu D2 0 1 1 D3, 1 it in D4	D2: iit. D2: iit. D4: 1 D4: 1 a clo	BRON No bral Dn bral The r D1 0 1 0 1 0 Regis D2	ke regi Os 1.C 1M 0.S ter ulse	Ster wh CLK cillator s 12MHz 1Hz 18MHz (when input SEL	no sets t top I use an into CL	frequer	Initia *Def ncy of tl Num *Def al oscill or the IG Inpu	alizatio fault ne osci ber of fault ation in C inside t clock	n to be llatory f initializ nvalidit e as bas division	perform frequent ation se y) who s ic time. n ratio s	ned/not cy whe equence sets the witchin	to be p on you e swing e ratio to ng	operate 3 back 0 do a s	an inte	ng rnal os o when	cill I co
	D1, D1, circu D2 0 0 1 1 D3, 1 it in D4 0	D2: D2: D2: D4: D4: D4: D4: D4: D4: D4: D4	BRON No bral Dn bral The I D1 0 1 0 1 0 1 0 1 0 1 0 0 1 0 0 0 0 0	ke regi IN(Os 1.C 1W 0.S ter ulse Ck	ster wh CLK cillator si 22MHz HZ 88MHz (when input SSEL	top I use an into CL	frequer	Initia *Def ney of th Num *Def al oscill or the IC Input *Def	alizatio fault ne osci ber of fault ation in C inside t clock fault	n to be llatory f initializ nvalidit e as bas division	perform frequent ation se ic time. n ratio s 1/4	ned/not cy whe equence sets the witchin	to be p en you e e swing e ratio to ng	operate 5 back 0 do a s	an inte	ng mal os	cill I cc
	D1, 0 1 D1, circu D2 0 0 1 1 D3, 1 it in D4 0 0) 	BRON No brai Dn brai The 1 D1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	ke regi INK Os 1.C 1N 0.s ter alse Ck 1/4 1/2	ster wh CLK cillator si p2MHz Hz b8MHz (when input SEL	top I use an into CL	frequer	Initia *Def ney of th Num *Def al oscill or the IQ Inpu *Def	alizatio fault ne osci ber of fault ation in C inside t clock fault	n to be llatory f initializ nvalidit <u>:</u> e as bas division	perform frequent ation se ic time. n ratio s 1/4 1/2	ed/not ey whe equence sets the witchin	to be p en you e swing e ratio t ng	operate g back	an inte	ng rnal os	cill:
	D1, D1, circu D2 0 0 1 1 D3, 1 it in D4 0 1	D2: 1 0 0 0 0 0 0 0 0 0 0 0 0 0	BRON No brai Dn brai Dn brai D1 0 1 0 1 0 1 0 1 0 1 0 0 1 0 0 1 0 0	ke regi IN(Os 1.0 0.9 1.0 0.9 1.1 Ck 1/4 1/2 1	ster wł CLK cillator si p2MHz Hz p8MHz (when input SEL 2	top I use an	frequer	Initia *Def ncy of th Num *Def al oscill or the IQ Input *Def	alizatio fault ne osci ber of fault ation in C inside t clock fault	n to be llatory f initializ nvalidit <u>;</u> e as bas division	y) who sic time. n ratio s 1/4 1/2 1 (n	ned/not cy whe equence sets the witchin	to be p en you e swing e ratio t ng uency d	operate back o do a s	an inte hare lap	ng rnal os	cilla I cc
	D1, D1, circu D2 0 0 1 1 D3, 1 it in D4 0 1 1	D2: D2: iit. D4: 1 D4: 1 D4: 1 D4: 1	BRON No brai Dn brai The r D1 0 1 0 1 0 1 0 0 1 0 1 0 1 0 1	ke regi IN(Os 1.C 1/ 0.s ter ulse Ck 1/4 1/2 1	ster wh CLK cillator s i2MHz iHz i8MHz (when input SEL i 2	I use an	frequer	Initia *Def ncy of th Num *Def al oscill or the IC Input *Def	alizatio fault ne osci ber of ault ation in C inside t clock ault	n to be llatory f initializ nvalidit e as bas division	perform frequent ation se ic time. n ratio s 1/4 1/2 1 (n 1 (n	ed/not cy whe quence sets the witchin o frequ o frequ	to be p en you o e swing e ratio t ng uency d uency d	operform operate back o do a s livision	an inte hare lap	ng rnal os	cill I co
	D1, D1, circu D2 0 0 1 1 1 D3, 1 it in D4 0 1 1) 	BRON No brai Dn brai The r D1 0 1 0 1 0 1 0 0 1 0 0 1 0 1 0 1	Ke Regi INC Os 1.C 1.C 1.W 0.S ter alse CK 1/4 1/2 1 1	ster wh CLK cillator si 22MHz HZ 88MHz (when input SEL 2	to sets t	frequer	Initia *Def ney of th Num *Def al oscill or the IQ Inpu *Def	alizatio fault ne osci ber of fault ation in C inside t clock fault	n to be llatory f initializ nvalidit e as bas division	y) who so the second se	ed/not ey whe equence sets the witchin o frequ o frequ	to be p en you d e swing e ratio to ng uency d uency d	operate back o do a s livision	an inter hare lap	ng mal os	cill I co
	$\begin{array}{c} D \\ 0 \\ 1 \\ 0 \\ 1 \\ 0 \\ 0 \\ 1 \\ 1 \\ 0 \\ 0$	D2: 1 1 1 1 1 1 1 1 1 1 1 1 1	BRON No brai Dn brai Dn brai D1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	Ke Regi INC 0s 1.0 0.5 1.10 0.5 1.12 <p< td=""><td>ster wh CLK cillator st 22MHz IHz 08MHz (when input SEL 2 registe</td><td>to sets the set of the</td><td>frequer intern K pin egister</td><td>Initia *Def ney of th Num *Def al oscill or the IQ Input *Def</td><td>alizatio fault ne osci ber of fault ation in C inside t clock fault</td><td>n to be llatory f initializ nvalidit<u>;</u> e as bas division</td><td>perform frequence ation se ic time. n ratio s 1/4 1/2 1 (n 1 (n 0 of the IC</td><td>ed/not ey whe equence sets the witchin o frequ C.</td><td>to be p en you d e swing e ratio t ng hency d</td><td>operate back o do a s livision</td><td>an inter hare lap</td><td>ng rnal os</td><td>cill:</td></p<>	ster wh CLK cillator st 22MHz IHz 08MHz (when input SEL 2 registe	to sets the set of the	frequer intern K pin egister	Initia *Def ney of th Num *Def al oscill or the IQ Input *Def	alizatio fault ne osci ber of fault ation in C inside t clock fault	n to be llatory f initializ nvalidit <u>;</u> e as bas division	perform frequence ation se ic time. n ratio s 1/4 1/2 1 (n 1 (n 0 of the IC	ed/not ey whe equence sets the witchin o frequ C.	to be p en you d e swing e ratio t ng hency d	operate back o do a s livision	an inter hare lap	ng rnal os	cill:
	D1, D1, circu D2 0 0 1 1 D3, 1 1 D3, 1 1 D3, 1 1 D3, 1 1 D5 :	D2: iit. D2: iit. D4: D4: D4: D4: D4: D4: D4: D4:	BRON No brai Dn brai Dn brai D1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	Ke IN4 Os 1.0 1.0 1.0 1.0 1.0 0.8 1/4 1/2 1 1 1 1 1 1 1 1	ster wh CLK cillator s 22MHz HHZ 28MHz (when input SEL 2 cregista the stat	I use an into CL	frequer intern K pin egister IIN=1,	Initia *Def ney of th Num *Def al oscill or the IC Input *Def setting the outp	alizatio fault ne osci ber of fault ation in C inside t clock fault start, th put of t	n to be llatory f initializ nvalidit <u>;</u> e as bas division he stop o he IC o	y) who sic time. n ratio s 1/4 1/2 1 (n 1 (n of the IC perates.	ed/not cy whe quence sets the witchin o frequ C. It beco	to be p en you d e swing e ratio t ng hency d hency d	operform operate back o do a s livision wait m	an inter hare lap	ng rnal os o when he time	cill I co
	D1, 0 1 D1, circu D2 0 0 1 1 D3, 1 1 D3, 1 1 D5 :	D2: itt. D2: itt. D4: D4: D4: D4: D4: D4: D4: D4:	BRON No bral Dn bral Dn bral Dn bral Dn bral D 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	Ke regi IN0 0s 1.0 1.0 1.0 1.0 0.9 ck 1/2 1 1 1 1 1 1 1 1 1	ster wh CLK cillator si 22MHz IHz 98MHz (when input SEL i SEL i sec input state i sec i he state	I use an into CL	frequer	Initia *Def ney of th Num *Def al oscill or the IG Input *Def setting the outp	Alizatio Fault ne osci ber of Tault ation in C inside t clock Tault start, th put of t	n to be llatory f initializ nvalidit e as bas division he stop o he IC o	perform frequent ation se ic time. n ratio s 1/4 1/2 1 (n 1 (n cof the IC perates.	ed/not ey whe equence sets the witchin o frequ o frequ C. It beco	to be p en you o e swing e ratio to ng hency d hency d bomes a	operform operate back o do a s livision wait m	an inter an	ng rnal os o when he time	cill I cc
	D1, 0 1 D1, circu D2 0 0 1 1 D3, 1 1 D3, 1 1 D4 0 1 D5 :	D2: iit. D2: iit. D4: D4: D4: D4: D4: D4: D4: D4:	BRON No brai Dn brai Dn brai D1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1	ке геді 1.0 0s 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0 1.0	ster wh CLK cillator si 22MHz IHz 98MHz (when input SEL cise	to sets the set of the	frequer	Initia *Def ney of th Num *Def al oscill or the IQ Input *Def setting the outp	alizatio fault ne osci ber of fault ation in C inside t clock fault start, th put of t	n to be llatory f initializ nvalidit e as bas division he stop o he IC o	perform frequent ation se ic time. n ratio s 1/4 1/2 1 (n 1 (n cof the IC perates.	ed/not ey whe equence sets the witchin o frequ C. It beco	to be p en you e swing e ratio t ng hency d omes a	operate back o do a s livision wait m	an inter hare lap	ng rnal os o when he time	cill I cc

3	0	0	0	0	0	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0
	CT				1 0 1		1	. 1	(0) 0	() D	C 1/	0				

GTAS7 to GTAS0 : Sets the GATE_A pulse set value (0 to 255). Default = 0

LC08101CT

	·			,		1	1	1	1						•		
4	0	0		0	0	0	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0
	STE	P7 to	o STP	0 : Oı	itput p	ulse st	ep num	ber for	the DR	IVE in	put (1 t	o 256).	Defaul	t = 1			
				+1	is the	quantit	y that I	did, ar	nd the s	et rang	e is trea	ted in c	lata lev	vel.			
				Wł	nen I i	nput at	8 bits (0 to 25	5), it is	treated	in STF	setting	g period	d of 1 to	o 256.		
						r	1	I	1								
5	0	0		0	0	0	1	0	1	D7	D6	D5	0	D3	D2	D1	D0
	D0	to D	03: IO	UT3	to IOL	JT0 Ou	tput co	nstant o	current	level se	etting (() to 15)	. Defau	11 = 21	0mA ty	pical	
							1				U V	,			2	1	
	D	3	D2	D1	D0		IOUT3	to IOUT)	Outpu	ut current	setting(ty	vpical)				
	()	0	0	0			0			21	10mA					
	()	0	0	1			1			19	99mA					
	()	0	1	0			2	189mA								
	()	0	1	1			3	178mA								
))	1	0	1			4 5	168mA								
	()	1	1	0			6			14	47mA					
	()	1	1	1			7			13	36mA					
	1	1	0	0	0			8			12	26mA					
	1	I	0	0	1			9			11	I5mA					
	1	1	0	1	0			10			10)5mA					
	1	1	0	1	1			11			9	4mA					
	1	1	1	0	1		12 84MA 13 73mA										
	1	1	1	1	0			14			6	3mA					
	1	1	1	1	1			15			5	2mA					
	D4,	D5:	: SW1	, SW	2												
		Iti	is a cu	irrent	value	adjusti	nent bit	t of the	consta	nt curre	nt outp	ut. Plea	ise usua	ally use	e it in 00) setting	g at the
		tin	ne or	use.													
	D6.	D7:	: TES	Т1. Т	EST0												
	,	Ιu	ise it v	with t	he test	mode	of the d	lriver I	C. Pleas	se usua	lly use	it in 00	setting	at the	time of	use.	
6	0	0		0	0	0	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0
	D0	to D	07 : TI	BRAK	KE0 to	TBRA	KE7 B	rakes p	oulse fre	equency	v setting	g (1 to 2	256). D	efault =	= 1		
					The	setting	value r	ange is	handle	d as the	e data v	alue pl	us 1.				
	I	f, wl	hen th	e BR	ON re	gister i	s set to	1, a dr	ive com	mand l	based of	n DRV	PULSE	is inpu	it, the b	rake pu	lse is
	0	utpu	it in th	he rev	verse d	irection	n after t	the nor	mal ope	ration	has end	ed. The	e revers	e-direc	tion op	eration	for the
	n	umt	ber of	perio	as set	by I B	KAKE	(the sar	ne ariv	e wave	lorm as	when	IVI/1 1S S	switche	a) is pe	riorme	1.
7	0	٥		0	0	0	1	1	1	0	0	D5	Π4	D3	ר2	D1	DU
'	ND		15 to		UT 10	(0 to 6	2) Def	$\frac{1}{1}$)	0	Ŭ	50	DŦ	50	DZ		DU
	TNN T	r UL 'he t	otal o	utnut	freque	(0 to 0 ency is	set for	aun – (the driv) ve wave	forms	from N	R1 to N	JR5 du	ring the	rise w	hen a m	ultinle
	n	umt	ber of	drive	wave	forms a	are outp	ut cont	tinuous	v durir	ig actua	tor ope	ration.	ing uit	115 C W		unipie
	I	f 0 h	as be	en set	, the N	R driv	e wave	forms a	re not c	output f	or the r	ise, and	l the no	rmal op	peration	is perf	ormed.
										-				1		-	
8	0	0		0	0	1	0	0	0	0	0	D5	D4	D3	D2	D1	D0
	NR	P-A	5 to N	RP-A	A0 (0 t	o 63). I	Default	= 0	•	•	•			-	-		
	Т	his	regist	er set	ts the	timing	of the	first sv	vitching	, for th	e rise-t	ime NF	R drive	wavef	orms. T	he nun	nber of
	р	erio	ds for	whic	h the	NR1 w	aveform	n is to	be outp	ut is se	t.						

9	0	0	0	0	1	0	0	1	0	0	D5	D4	D3	D2	D1	D0
	NRP-B5 to NRP-B0 (0 to 63). Default = 0															

This register sets the timing of the second switching for the rise-time NR drive waveforms. It outputs the

NR2 waveform for the number of periods that is the difference between NRP-A and NRP-B.

10	0	0	0	0	1	0	1	0	0	0	D5	D4	D3	D2	D1	D0
	NR	P-C5 to	NRP-	C0 (0 t	o 63). I	Default	= 0									
	This register sets the timing of the third switching for the rise-time NR drive waveforms. It outputs the NR3															
	waveform for the number of periods that is the difference between NRP-B and NRP-C.															
11	0	0	0	0	1	0	1	1	0	0	D5	D4	D3	D2	D1	D0
	NR	P-D5 to	NRP-	D0 (0 t	to 63). I	Default	= 0									
	This register sets the timing of the fourth switching for the rise-time NR drive waveforms.															
	The NR4 waveform is output for the number of periods that is the difference between NRP-C and NRP-D,															
	and the NR5 waveform is output for the number of periods that is the difference between NRP-D and															
NRPUL1.																
When setting the rise-time NR drive waveforms, set values which, in principle, satisfy the following relationship:																
NRP-A \leq NRP-B \leq NRP-C \leq NRP-D																
(If th	nis rela	tionship	is not	satisfie	ed, unin	tended	drive v	vavefor	ms ma	y be ou	tput, bu	it the IC	C will n	ot be b	roken o	r
dam	aged a	s a resul	t.)													
		1		T	r –				r	1						
12	0	0	0	0	1	1	0	0	0	0	D5	D4	D3	D2	D1	D0
	NRPUL25 to NRPUL20 (0 to 63). Default = 0															
The total output frequency is set for the drive waveforms from NR1 to NR5 during the fall when a multiple																
	number of drive waveforms are output continuously during actuator operation.															
IT U has been set, the NK drive waveforms are not output for the rise, and the stops.																
13	0	0	0	0	1	1	0	1	0	0	D5	D4	D3	D2	D1	D0
-	NR	P-E5 to	NRP-	E0 (0 to	1) efault :	= 0		-	_						
	1 (1) r	This reg	ister s	ets the	timing	of the	first sw	vitching	o for th	e fall-ti	ime NF	drive	wavefo	orms T	he nun	nber of
	1	periods f	for wh	ich the	NR5 wa	aveform	n is to l	be outp	ut is se	t.						
								1								
14	0	0	0	0	1	1	1	0	0	0	D5	D4	D3	D2	D1	D0
	NR	P-F5 to	NRP-	F0 (0 to	o 63). D	efault =	= 0									
	r	This reg	ister s	ets the	timing	of the s	second	switch	ing for	the fall	-time 1	NR driv	e wave	eforms.	It outp	uts the
]	NR4 wa	veform	n for the	e numb	er of pe	riods th	nat is th	e diffe	rence b	etween	NRP-E	and N	RP-F.		
						-										
15	0	0	0	0	1	1	1	1	0	0	D5	D4	D3	D2	D1	D0
	NR	P-G5 to	NRP-	-G0 (0 t	to 63). I	Default	= 0									
	r	This reg	ister se	ets the t	iming o	f the th	ird swi	tching	for the	fall-tim	e NR d	rive wa	veform	ns. It ou	tputs th	ie NR3
	v	wavefor	m for t	he num	ber of j	periods	that is	the diff	ference	betwee	n NRP	-F and	NRP-G	ſ.		
				1	r	r	1	1	r	1		-		-		
16	0	0	0	1	0	0	0	0	0	0	D5	D4	D3	D2	D1	D0
	NR	P-H5 to	NRP-	H0 (0 t	to 63). I	Default	= 0									
		This reg	ister se	ets the t	iming c	of the fo	ourth sv	vitching	g for th	e fall-ti	me NR	drive v	vavefor	ms.		
		The NR2	2 wave	eform is	s output	for the	numbe	er of pe	riods th	hat is th	e differ	rence be	etween	NRP-C	and N	RP-H,
	: ۱		NKI V 2	wavero	rm is o	utput 1	or the	number	r or pe	rioas tr	iat is t	ne diffe	erence	betwee	n NKP	·H and
	1	NIXI UL.	<i>-</i> .													
Whe	When setting the fall-time NR drive waveforms, set values which, in principle, satisfy the following relationship:												p:			
NRP-E < NRP-F < NRP-G < NRP-H																

(If this relationship is not satisfied, unintended drive waveforms may be output, but the IC will not be broken or damaged as a result.)

17	0	0	0	1	0	0	0	1	0	0	D5	D4	D3	D2	D1	D0
	NRPUL35 to NRPUL30 (0 to 63). Default = 0															
	The total output frequency is set for the drive waveforms from NR1 to NR5 during the rise when a multiple															
	number of drive waveforms are output continuously during actuator operation.														1	
	1	f 0 has	been se	et, the N	NR driv	e wave	forms a	are not	output	for the	rise, an	d the st	art Bra	ke outp	ut.	
18	0	0	0	1	0	0	1	0	0	0	D5	D4	D3	D2	D1	D0
	NR	P-I5 to	NRP-I	0 (0 to	63). De	fault =	0									
	-	This reg	gister so	ets the	timing	of the	first sw	vitching	g for th	e rise-t	ime NF	R drive	wavef	orms. T	he nun	iber of
	ł	periods	for whi	ich the	NR1 w	aveforr	n is to l	be outp	ut is se	t.						
		r	1	r	1	1	r	r	r	r	1	1				
19	0	0	0	1	0	0	1	1	0	0	D5	D4	D3	D2	D1	D0
	NRP-J5 to NRP-J0 (0 to 63). Default = 0															
	This register sets the timing of the second switching for the rise-time NR drive waveforms. It outputs the															
NR2 waveform for the number of periods that is the difference between NRP-I and NRP-J.																
				1			1	1	1		1	1				
20	0	0	0	1	0	1	0	0	0	0	D5	D4	D3	D2	D1	D0
	NRP-K5 to NRP-K0 (0 to 63). Default = 0															
	This register sets the timing of the third switching for the rise-time NR drive waveforms. It outputs the NR3															
waveform for the number of periods that is the difference between NRP-J and NRP-K.																
24	0	0	0	4	0	4	0	4	0	0	DE	D4	D2	D2	D1	D0
21						- C 14	0		0	0	D3	D4	03	DZ	DI	DU
	NK	P-LO IC) NKP-	LU (U to) 63). L	f the f	= ()	vitahin	- for th	a miaa ti	ma ND	drive		****		
	-	The NR	4 wave	form is		for the	numb	er of ne	g ior in riods t	e fise-ti hat is th	ne diffe	rence h	etween	NRP_k	and N	RP-I
	8	and the	NR5 v	vavefo	rm is o	utput f	for the	numbe	r of pe	riods th	hat is t	he diff	erence	betwee	n NRP	-L and
	1	NRPUL	3.			1			1							
W 71.					•	C		.1	1:1:			:-C 4	6.11.		1.	•
wne	n seun	ng the r D I < N			rive wa	velorm	is, set v	alues w	/nich, i	n princi	pie, sa	listy the		ving rei	ationsn	ip:
		1 -1 <u>-</u> 1 If this r	elation	shin is i	$x \ge 100$	1 -L sfied u	nintend	ed driv	e wave	forms n	nav he	output	but the	IC will	not he	hroken
	(n dama	ored as	a result	-)	siicu, u	mintend		c wave	1011115 11		Juipui,	out inc	IC will	not be	UIUKCII
	,	Ji dama	geu us	a resurt)											
22	0	0	0	1	0	1	1	0	0	0	D5	D4	D3	D2	D1	D0
	NR	PUL45	to NR	PUL40	(0 to 6	3) Def	ault = ()				<u> </u>	<u> </u>	<u> </u>		·
		The tota	l outpu	t frequ	ency is	set for	the driv	ve wave	eforms	from N	R1 to 1	vR5 du	ring the	e fall w	hen a m	ultiple
	1	number	of driv	e wave	forms a	re outp	out cont	inuous	ly durir	ng actua	tor ope	ration.	U			1
]	f 0 has	been se	et, the N	NR driv	e wave	forms a	are not	output	for the	rise, an	d the st	ops.			
		1	i	.	i	i						
23	0	0	0	1	0	1	1	1	0	0	D5	D4	D3	D2	D1	D0
	NR	P-M5 t	o NRP-	-M0 (0	to 63).	Defaul	t = 0									
		This reg	gister so	ets the	timing	of the	first sv	vitching	g for th	e fall-ti	ime NF	R drive	wavef	orms. T	he nun	iber of
	I	periods	for whi	ich the	NR5 w	aveforr	n is to l	be outp	ut is se	t.						
		T		1			1	1	1	r - 1	1	1				
24	0	0	0	1	1	0	0	0	0	0	D5	D4	D3	D2	D1	D0
	NR	.P-N5 to	NRP-	N0 (0 t	o 63). I	Default	= 0								_	
		This reg	gister se	ets the	timing	of the	second	switch	ing for	the fall	l-time 1	NR driv	e wave	eforms.	It outp	uts the
	1	NR4 wa	veform	n for the	e numb	er of pe	eriods tl	hat is th	e diffe	rence b	etween	NRP-N	A and N	NRP-N.		

25	0	0	0	1	1	0	0	1	0	0	D5	D4	D3	D2	D1	D0
	NR	P-05 to	NRP-	O0(0)	o 63) I	Default	= 0			I						
	This register sets the timing of the third switching for the fall-time NR drive waveforms. It outputs the NR3															
	waveform for the number of periods that is the difference between NRP-N and NRP-O.															
	•															
26	0	0	0	1	1	0	1	0	0	0	D5	D4	D3	D2	D1	D0
	NR	P-P5 to	NRP-I	P0 (0 to	63). D	efault =	= 0									
	-	This reg	ister se	ts the t	iming o	of the fo	ourth sv	vitching	g for the	e fall-ti	me NR	drive v	vavefor	ms.		
	The NR2 waveform is output for the number of periods that is the difference between NRP-O and NRP-P,														RP-P,	
	and the NR1 waveform is output for the number of periods that is the difference between NRP-P and															
	NRPUL4.															
Whe	When setting the fall-time NR drive waveforms, set values which in principle, satisfy the following relationship:															
	NRP-M < NRP-N < NRP-O < NRP-P															
	(If this relationship is not satisfied, unintended drive waveforms may be output, but the IC will not be broken															
	or damaged as a result.)															
				T												
27	0	0	0	1	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0
	NR	1GTAS	7 to N	R1GTA	.S0 (0 t	o 255).	Defaul	t = 0								
	GATE_A pulse set value for NR1 waveform															
				1						-				-		
28	0	0	0	1	1	1	0	0	D7	D6	D5	D4	D3	D2	D1	D0
	NR	2GTAS	7 to N	R2GTA	.S0 (0 t	o 255).	Defaul	t = 0								
	(GATE_A	A pulse	set val	ue for I	NR2 wa	aveform	1								
20	0	0	0	1	1	1	0	1	DZ	De	D5	D4	D2	D2	D1	DO
29	ND		7 to NI		50 (0 +	- 255)	Defaul	t = 0	Di	D0	D3	D4	D3	DZ	Ы	DU
	INK	SOTAS	\wedge 10 M	K3GIA	.50 (0 l 110 for 1	0 233). ND 2 m	Defaul	l = 0								
	,	JAIL_/	A puise	set val		NICJ W	aveloin	1								
30	0	0	0	1	1	1	1	0	D7	D6	D5	D4	D3	D2	D1	D0
	NR	4GTAS	7 to N	R4GTA	.S0 (0 t	o 255).	Defaul	t = 0								
	(GATE A	A pulse	set val	ue for l	NR4 wa	aveform	ı								
			-													
31	0	0	0	1	1	1	1	1	D7	D6	D5	D4	D3	D2	D1	D0
	NR	5GTAS	7 to N	R5GTA	.S0 (0 t	o 255).	Defaul	t = 0								
	(GATE_A	A pulse	set val	ue for l	NR5 wa	aveform	ı								
	r									-						
32			1	No registe	er address	6			D7	0	0	0	0	0	0	0
	This is a read-only register line.															

D7: BUSY register "1" is output during output operations; "0" is output when the output has stopped.

Functional Description

1 period :

One period of OUT waveform operation is equivalent to one output operation.



CLK input :

The pin for the external CLK input that provides the reference time for generating drive waveforms.

The frequency division ratio for I²C communication can be selected from 1/4, 1/2, and 1/1. Drive waveforms are generated by counting this frequency-divided clk pulses as the basic count unit. The LC08101CT supports frequency from 10MHz to 60MHz depending on the frequency division ratio and counter settings.

Register setup sequence :

(1) Apply VCC.

(2) Set register addresses 0x01 to 0x1F (set the waveform and drive conditions).

(3) Set the ENIN register to 1 (invoke initialization procedures if initialization is enabled or start up the IC).

(4) Set up M/I and DRVPULSE to start the AF operation (actuator operation instruction).

I²C communication during output operation :

I²C communication with all the registers is possible even when the IC is in operation (OUT processing or BUSY is held high).

However, if the drive waveform settings have been changed while the actuator is operating, for example, there is a possibility that unintended waveforms are output.

Actuator drive waveform settings :

Configuration of piezoelectric actuator drive waveform



The drive waveforms are set using four parameters: RST, GTAS, GTBR and GTBS.

- RST : Parameter determines the period, and sets the reference clock pulse count minus 1.
- GTAS : Parameter determines the time taken for the gate signal A to the falling edge from the reference point. Since the signal raises after two clock pulses from the reference, the Ta reference clock cycle count plus 1 is set.

[Example of settings] When setting reference clock to 10MHz, period to 13µs, Ta to 2.0µs Since the reference clock time is 0.1µs :

The period is 130 clks. \rightarrow Specify 129 (RST value of 130 -1). Ta is 20 clks. \rightarrow Specify 21 (GTAS value of 20 + 1).

Timing charts

Enlarged view of the sequence of output signals



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