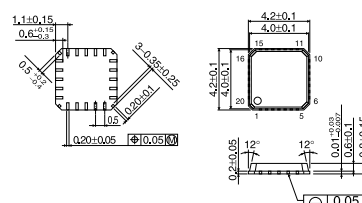# Clock generator for digital still camera
BU2385KN

● Description

BU2385KN is a clock generator IC that can generate multiple frequencies(clocks) from one oscillator. Excellent jitter characteristic is achieved through the built-in high-performance 3-channel PLL. High-quality sound and image equivalent to the oscillating module are the result of this feature. Clocks can be easily changed for other applications. The internal dividing control allows the frequency to be switched outside.

● Features

1) Multiple frequency clock signals can be generated by the built-in 3-channel PLL through connecting crystal oscillator.
2) QFN20V package
3) 3.3V single power supply
4) For crystal 14.318182MHz · 28.636363MHz

● Applications

Digital still camera

● Dimension (Unit : mm)

QFN20V

● Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Limits		Unit
Applied voltage	V_{DD}	−0.5	~ +7.0	V
Input voltage	V_{IN}	−0.3	~ V_{DD}+0.3	V
Storage temperature range	Tstg	−30	~ +125	˚C
Power dissipation	Pd	530		mW

*Derating : 5.3mW/˚C for operation above Ta=25˚C

● Recommended Operating Conditions (Ta=25˚C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3.0	–	3.6	V
Input H voltage range	V_{IH}	$0.8V_{DD}$	–	V_{DD}	V
Input L voltage range	V_{IL}	0.0	–	$0.2V_{DD}$	V
Operating temperature range	Topr	−5	–	70	˚C
Output load	C_L	–	–	15	pF

● Electrical characteristics (Unless otherwise noted: Ta=25°C, Vcc=3.3V)

When crystal is 28.636363MHz, Xtal_SEL=H. When crystal is 14.31818MHz, Xtal_SEL=L.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating circuit current	I$_{DD}$	–	40	50	mA	No load
Output frequency						
CLK1 FS2:H FS3:H	Fclk1-1	–	96.016044	–		Xtal * (228/17)/2
FS2:H FS3:L	Fclk1-2	–	71.877274	–		Xtal * (251/25)/2
FS2:L FS3:L	Fclk1-3	–	114.54546	–	MHz	Xtal * (224/14)/2
FS2:L FS3:H	Fclk1-4	–	90.314686	–	MHz	Xtal * (164/12)/2
CLK2 FS2:L FS3:L	Fclk2-1	–	96.016044	–	MHz	Xtal * (228/17)/2
FS2,3:HL LH HH	Fclk2-2	–	48.008022	–	MHz	Xtal * (228/17)/4
REFCLK FS1:H	Fref1-1	–	14.318182	–	MHz	Xtal direct
FS1:L	Fref1-2	–	17.734450	–	MHz	Xtal * (706/57)/10
Duty1 at 100MHz or less	Duty1	45	50	55	%	1/2V$_{DD}$ test
Duty2 at 100MHz or less	Duty2	–	50	–	%	1/2V$_{DD}$ test
Rise time	Tr	–	2.5	–	nsec	Time between 0.2V$_{DD}$~0.8V$_{DD}$
Fall time	Tf	–	2.5	–	nsec	Time between 0.8V$_{DD}$~0.2V$_{DD}$
Period jitter σ	P-J1 σ	–	30	–	psec	*1
Period jitter MIN-MAX	P-J MINMAX	–	180	–	psec	*2
Output lock time	Tlock	–	–	1	msec	*3

Note) Output frequency is determined by the operation expression (Frequency divide) input to Xtal IN.
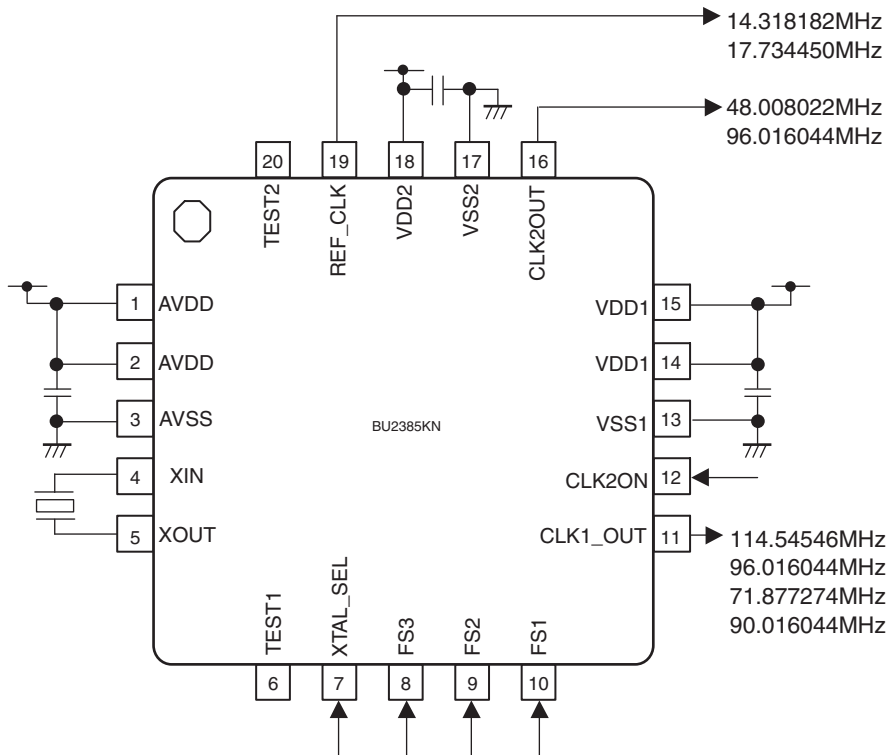Output when XIN input frequency is 14.318182MHz is shown above.
*1 Period Jitter 1 σ : Standard deviation value when using Time Interval Analyzer with 10,000 sampling of one period.
*2 Period Jitter MIN-MAX : Max width of jitter distribution when using Time Interval Analyzer with 10,000 sampling of one period.
*3 Output Lock time : Time between voltage supply leads to 3.0V and output clock gets stable.

● Application Circuit

Note) BU2385KN is basically placed on the board.
Bypass capacitor (0.1μF) needs to be placed between pin1,2 and pin3, pin13 and pin14,15, pin17 and pin18 as near to pin as possible.