

## CMOS Transimpedance Amplifier with AGC for Fiber Optic Networks up to 1.25 Gbps

Rev V4

### Applications

- GPON
- GEAPON
- Gigabit Ethernet
- Fiber Channel

### Features

- Typical  $-29\text{dBm}$  sensitivity,  $+6\text{ dBm}$  saturation at 1.25 Gbps when used with 0.9 A/W InGaAs PIN. ( $C_{pd} \leq 0.5\text{pF}$ , BER  $10^{-10}$ )
- Typical differential transimpedance:  $24\text{ k}\Omega$
- Fabricated in standard CMOS
- Differential output
- Standard  $+3.3\text{ Volt}$  supply
- Available in die form only
- Monitor output
- AGC provides dynamic range of  $35\text{ dB}$
- Internal or external bias for photodiode
- PIN or APD sensor
- Same pad layout and die size as M02011/13/14/15

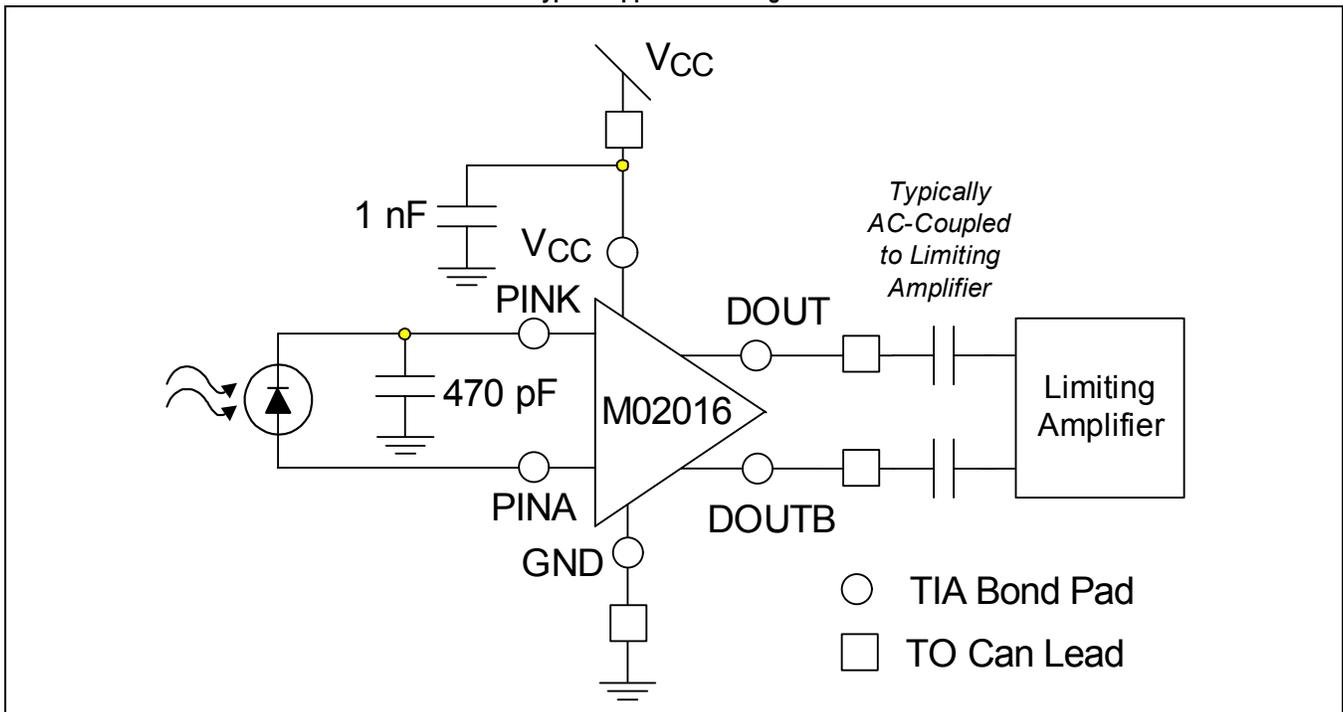
The M02016 is a CMOS transimpedance amplifier with AGC. The AGC gives a wide dynamic range of  $35\text{ dB}$ . The high transimpedance gain of  $24\text{ k}\Omega$  ensures good sensitivity.

For optimum system performance, the M02016 die should be mounted with a silicon or InGaAs PIN photo detector inside a lensed TO-Can or other optical sub-assembly.

The M02016 can either bias the PIN diode from the internal regulator or use an externally biased PIN diode.

A replica of the average photodiode current is available at the MON pad for photo-alignment.

Typical Applications Diagram



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### Ordering Information

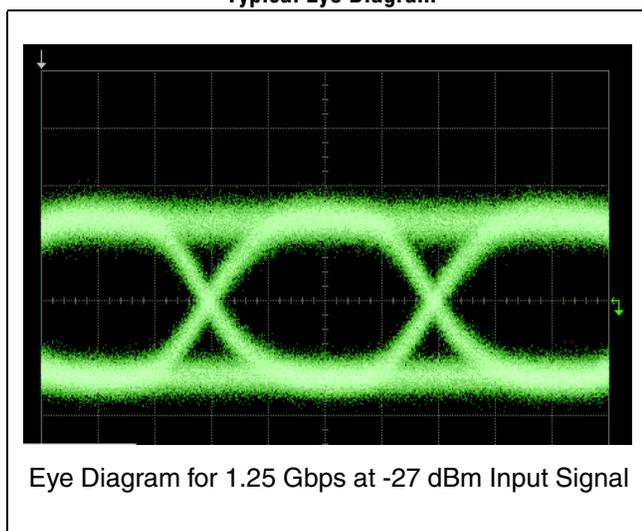
Part Number	Package	Operating Temperature
M02016-xx*	Waffle Pack	-40°C to 85°C
M02016-xx*	Expanded whole wafer on a ring	-40°C to 85°C

**NOTE:**  
\*xx represents the revision number. Please contact your local sales office for correct digits.

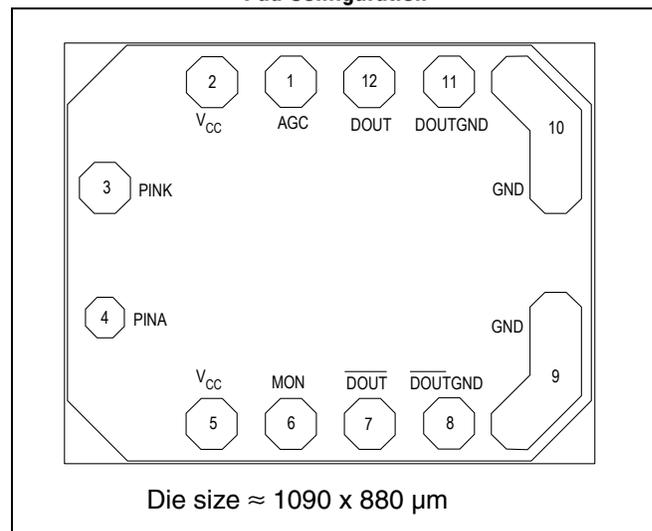
### Revision History

Revision	Level	Date	Description
V4	Release	May 2015	Updated logos and page layout. No content changes.
G (V3)	Release	August 2007	Corrected PinA, AGC, and DOUT absolute maximum voltage in Table 1-1. Removed Imon graph from the Typical Performance graphs (Chapter 1).
F (V2)	Release	June 2007	Revised Table 1-1 Separate Applications Information from Functional Description. Add notes to clarify the bonding procedure.
E (V1)	Release	November 2004	Production Release.

Typical Eye Diagram



Pad Configuration



# 1.0 Product Specification

## 1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

**Table 1-1. Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
$V_{CC}$	Power supply ( $V_{CC} - GND$ )	-0.4 to +4.0	V
$T_{STG}$	Storage temperature	-65 to +150	°C
$I_{IN}$	PINA Input current	8.0 <sup>(1, 2)</sup>	mA <sub>PP</sub>
$V_{PINA}, V_{AGC}$	Maximum input voltage at PINA and AGC	-0.4 to +2.0 <sup>(2)</sup>	V
$I_{PINK}$	Maximum average current sourced out of PINK	10.0	mA
$V_{PINK}, V_{MON}$	Maximum input voltage at PINK and MON	-0.4 to $V_{CC} + 0.4$	V
$I_{Dout}$	Maximum average current sourced out of Dout and DoutB	10.0 <sup>(3)</sup>	mA
$V_{Dout}$	Maximum input voltage at Dout and DoutB	0.0 to +2.0 <sup>(3)</sup>	V

**NOTES:**

- Equivalent to 4.9 mA average current.
- Do not exceed either the  $I_{IN}$  or  $V_{PINA}$  rating. PINA damage will result in performance degradation which is difficult to detect.
- Do not exceed either the  $I_{Dout}$  or  $V_{Dout}$  rating. Output device damage could occur.

## 1.2 Recommended Operating Conditions

**Table 1-2. Recommended Operating Conditions**

Symbol	Parameter	Rating	Units
$V_{CC}$	Power supply ( $V_{CC} - GND$ )	$3.3 \pm 10\%$	V
$C_{PD}$	Max. Photodiode capacitance ( $V_r = 1.7$ V, when using PINK), for 1.25 Gbps data rate	0.5	pF
$T_A$	Operating ambient temperature	-40 to +85	°C

## 1.3 DC Characteristics

**Table 1-3. DC Characteristics**

Symbol	Parameter	Minimum	Typical	Maximum	Units
$V_B$	Photodiode bias voltage (PINK – PINA)	1.7	2.0	2.2	V
$V_{CM}$	Common mode output voltage	0.7	1	1.3	V
$I_{CC}$	Supply current (no loads)	23	30	39	mA
$R_{LOAD}$	Recommended differential output loading	—	100 <sup>(1)</sup>	—	$\Omega$

**NOTE:**

1. 100 $\Omega$  is the load presented by the limiting amplifier.

## 1.4 AC Characteristics

**Table 1-4. AC Characteristics**

Symbol	Parameter	Minimum	Typical <sup>(1)</sup>	Maximum	Units
$R_{OUT}$	Output impedance (single ended) <sup>(2)</sup>	35	50	65	$\Omega$
LFC	Low frequency cutoff <sup>(3)</sup>	—	70	115	kHz
$V_D$	Differential output voltage	—	275	500	mV
DCD	Duty cycle distortion	—	—	40	ps
DJ	Deterministic jitter (includes DCD)	—	—	80	ps <sub>pp</sub>
In_rms	Total input RMS noise, DC to 930 MHz, Cin = 0.5 pF	—	130	185	nA
Pin	Example dynamic range of optical input <sup>(4)</sup>	-28	—	+6	dBm
PIN_mean_min	Optical Sensitivity <sup>(4)</sup>	—	-29	—	dBm

**NOTES:**

- Die designed to operate over an ambient temperature range of -40°C to +85°C,  $T_A$  and  $V_{CC}$  range from 3.0–3.6V. Typical values are tested at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 3.3\text{V}$ .
- Measured at 1 MHz.
- Input -28 dBm, Extinction Ratio = 10, Temp = 25°C.
- BER  $10^{-10}$ , PD capacitance = 0.5 pF, Responsivity 0.9 A/W, Extinction Ratio = 10.

## 1.5 Dynamic Characteristics

**Table 1-5. Dynamic Characteristics**

Symbol	Parameter	Minimum	Typical	Maximum	Units
G	Transimpedance				
	- Single ended	8	12	16	k $\Omega$
	- Differential	12	24	32	
BW	Bandwidth to -3 dB point @ -26 dBm, 0.9A/W, 0.5 pF PD	0.7	1.0	—	GHz
RC	AGC loop time constant	—	2	—	$\mu$ s
I <sub>AGC</sub>	AGC threshold	9	11	—	$\mu$ A <sub>pp</sub>
I <sub>OVL</sub>	Maximum functional input current	3.6 <sup>(1)</sup>	—	—	mA
PSRR	Power supply rejection, f < 4 MHz	20	28	—	dB

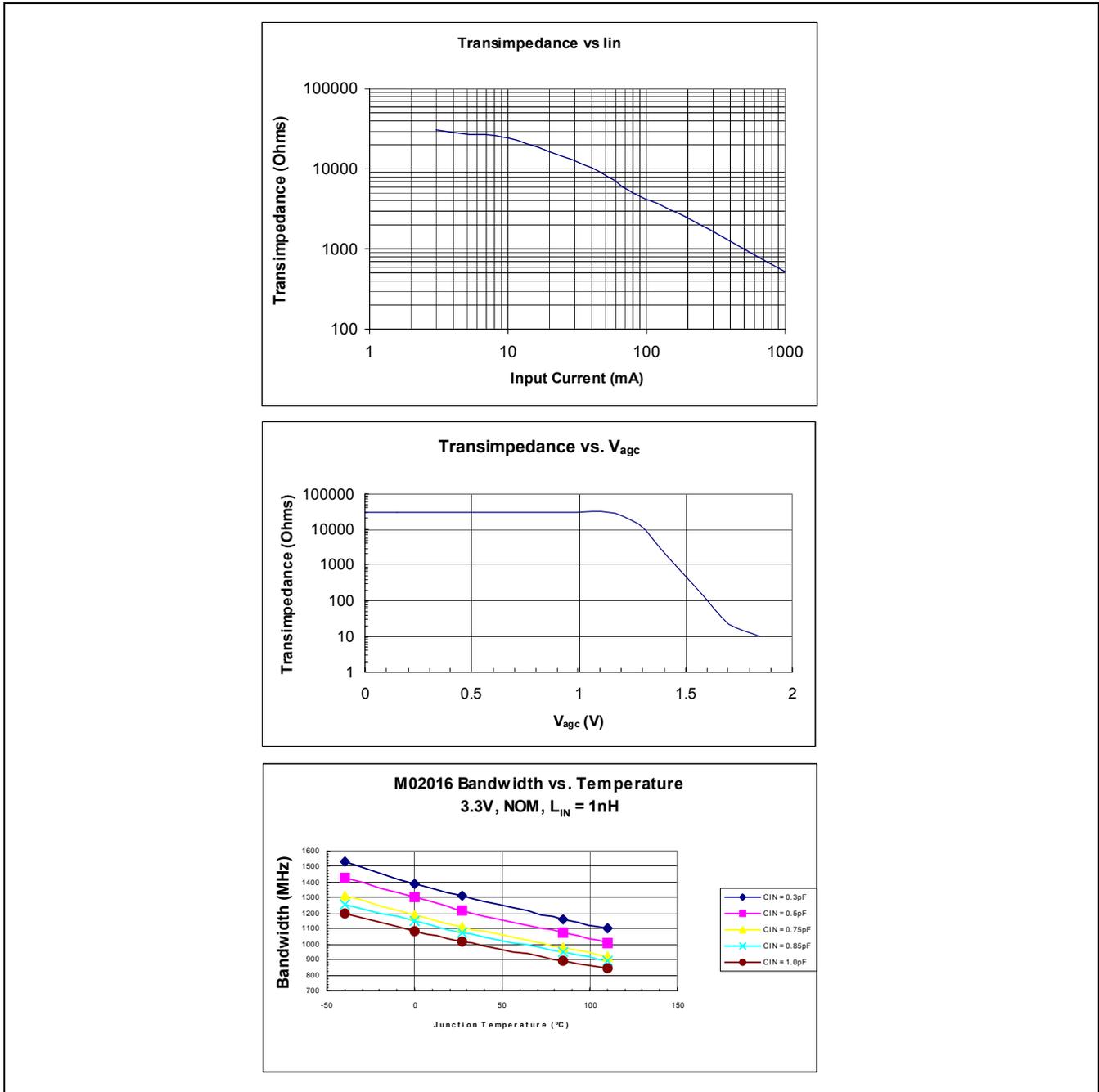
**NOTE:**

1. Equivalent to +3.4 dBm input optical power at Extinction Ratio = 10, Responsivity = 1.0 A/W.

### 1.6 Typical Performance

V<sub>cc</sub> = 3.3V, Temperature = 25 °C, L<sub>in</sub> = 1 nH, unless otherwise stated.

Figure 1-1. Typical Performance Diagrams 1 of 3

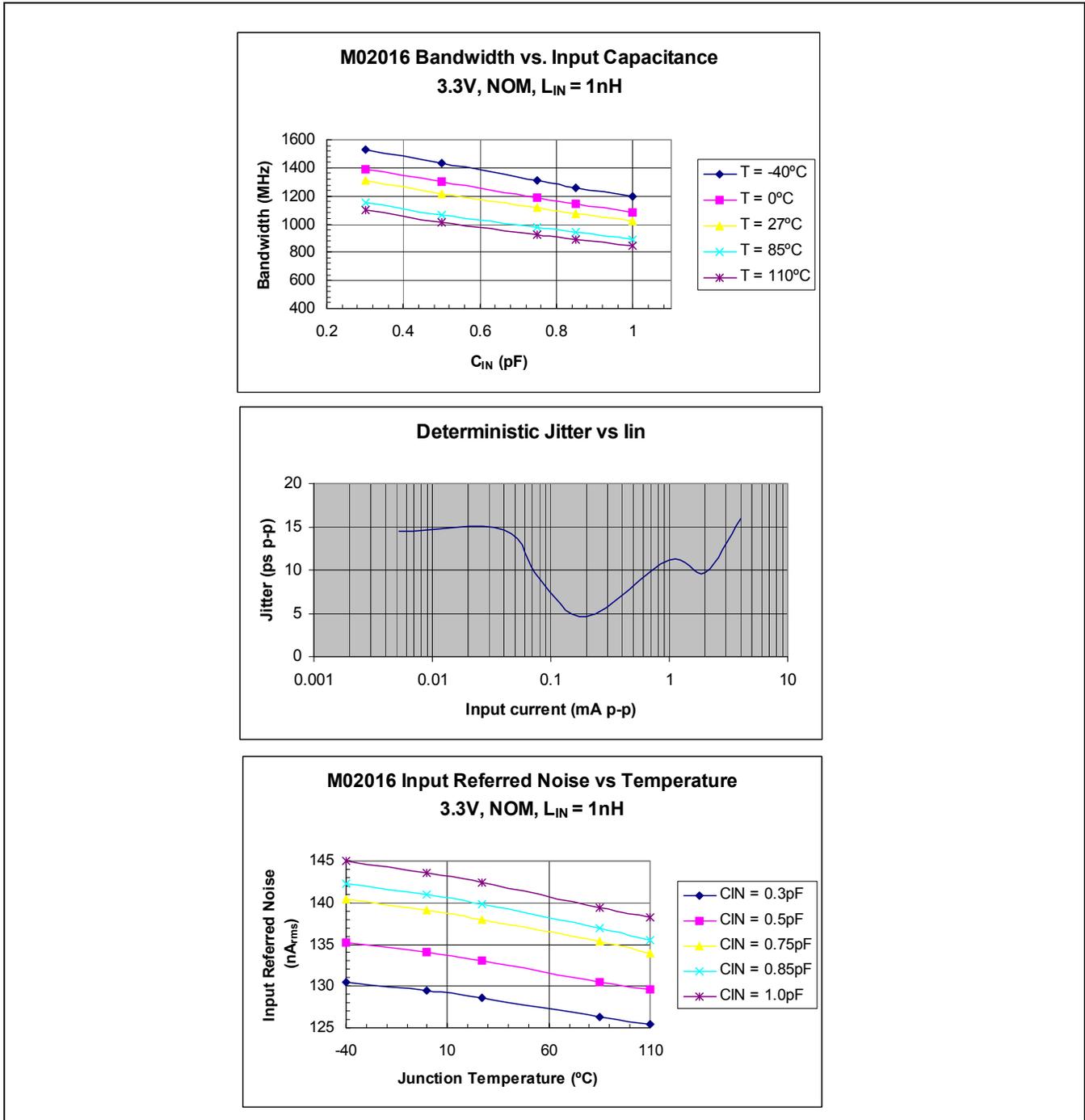


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V<sub>cc</sub> = 3.3V, Temperature = 25 °C, L<sub>in</sub> = 1 nH, unless otherwise stated.

Figure 1-2. Typical Performance Diagrams 2 of 3



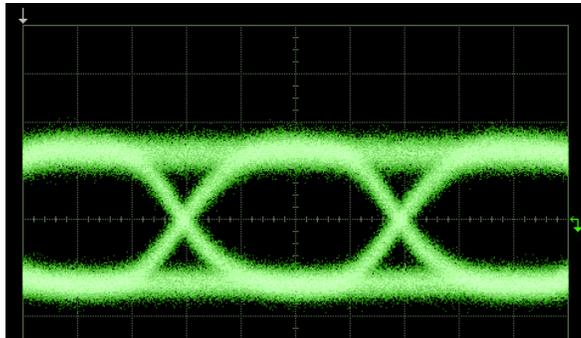
## CMOS Transimpedance Amplifier with AGC for Fiber Optic Networks up to 1.25 Gbps

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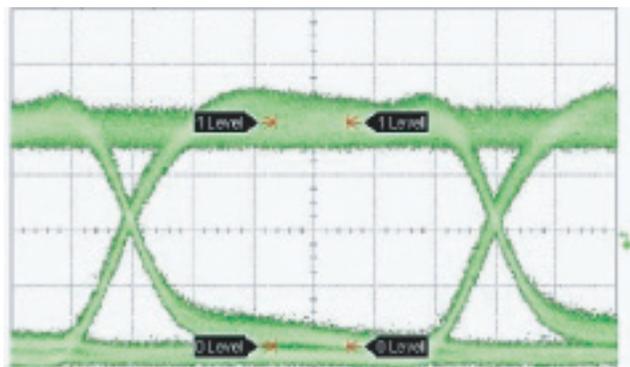
Vcc = 3.3V, Temperature = 25 °C, Lin = 1 nH, unless otherwise stated.

**Figure 1-3. Typical Performance Diagrams 3 of 3**

**Eye Diagram for 1.25 Gb/s at -27 dBm Input Signal**



**Eye Diagram for 1.25 Gb/s at +6 dBm Input Signal**



## 2.0 Pin/Pad Definitions

### 2.1 Pin/Pad Definitions

**Table 2-1. Pin/Pad Definitions**

Die Pad No	Name	Function
1	AGC	Monitor or force AGC voltage
2	V <sub>CC</sub>	Power pin. Connect to most positive supply
3	PINK	Common PIN input. Connect to photo diode cathode and a 470 pF capacitor to Gnd <sup>(1)</sup>
4	PINA	Active PIN input. Connect to photo diode anode
5	V <sub>CC</sub>	Power pin. Connect to most positive supply (only one V <sub>CC</sub> pad needs to be connected)
6	MON	Analog current sink output. Current matched to average photodiode current. Intended for photo-alignment use only.
7	$\overline{\text{DOUT}}$	Differential data output (goes low as light increases)
8	$\overline{\text{DOUTGND}}$	Ground return for $\overline{\text{DOUT}}$ pad <sup>(2)</sup>
9	GND	Ground pin. Connect to the most negative supply <sup>(2)</sup>
10	GND	Ground pin. Connect to the most negative supply <sup>(2)</sup>
11	$\overline{\text{DOUTGND}}$	Ground return for $\overline{\text{DOUT}}$ pad <sup>(2)</sup>
12	DOUT	Differential data output (goes high as light increases)
NA	Backside	Backside. Connect to the lowest potential, usually ground

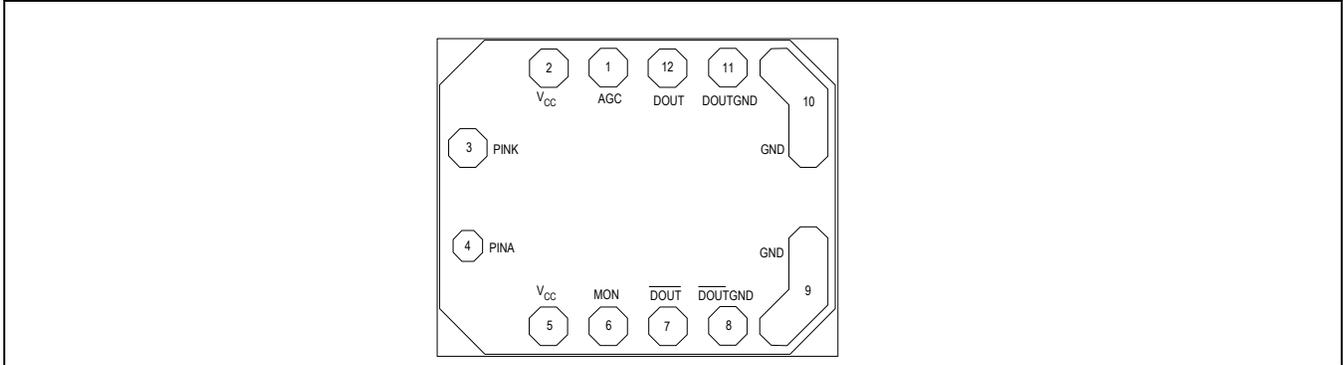
**NOTES:**

- Alternatively the photodiode cathode may be connected to a decoupled positive supply, e.g. V<sub>CC</sub>.
- All ground pads are common on the die. Only one ground pad needs to be connected to the TO-Can ground. However, connecting more than one ground pad to the TO-Can ground, particularly those across the die from each other can improve performance in noisy environments.

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Figure 2-1. Bare Die Layout



## 3.0 Functional Description

### 3.1 Overview

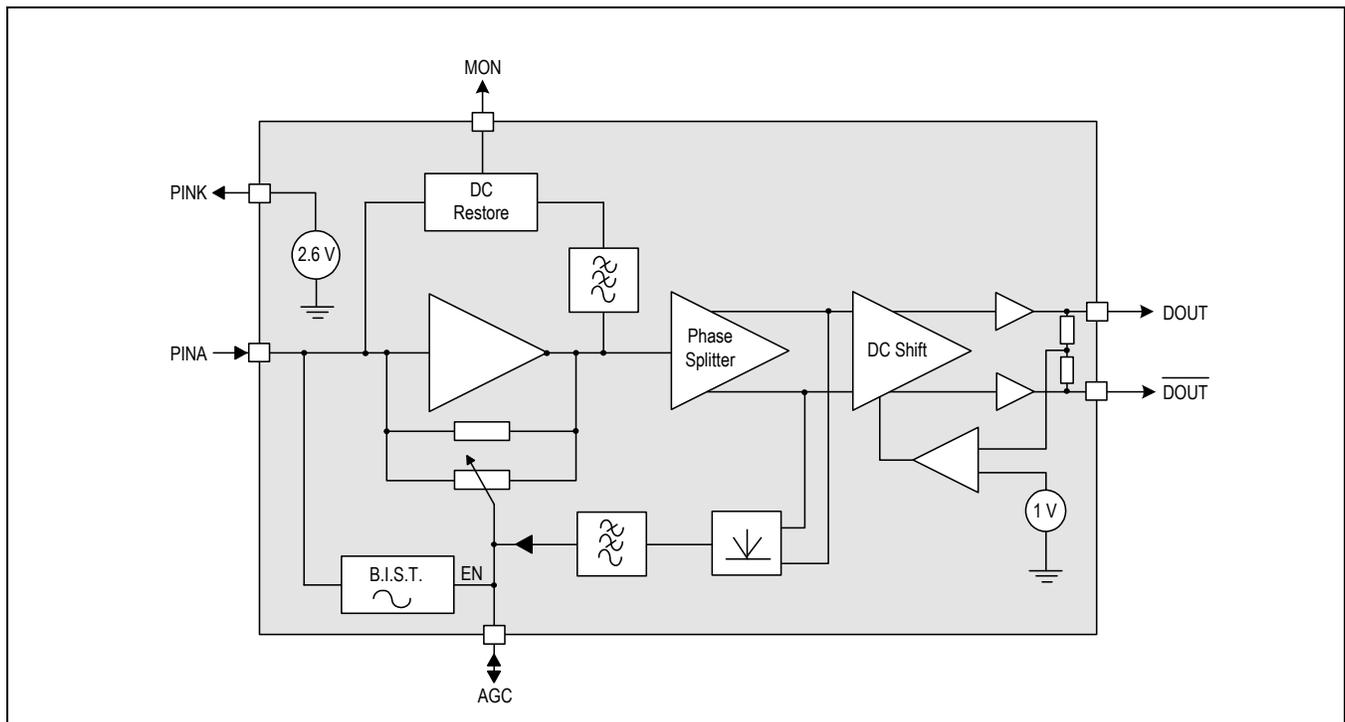
The M02016 is a CMOS transimpedance amplifier with AGC. The AGC gives a wide dynamic range of 35dB. The high transimpedance gain of 24 k $\Omega$  ensures good sensitivity.

For optimum system performance, the M02016 die should be mounted with a silicon or InGaAs PIN photo detector inside a lensed TO-Can or other optical sub-assembly.

The M02016 can either bias the PIN diode from the internal regulator or use an externally biased PIN diode.

A replica of the average photodiode current is available at the MON pad for photo-alignment.

**Figure 3-1. M02016 Block Diagram**



## 3.2 General Description

### 3.2.1 TIA (Transimpedance Amplifier)

The transimpedance amplifier consists of a high gain single-ended CMOS amplifier (TIA) with a feedback resistor. The feedback creates a virtual earth low impedance at the input and virtually all of the input current passes through the feedback resistor, defining the voltage at the output. Advanced CMOS design techniques are employed to maintain the stability of this stage across all input conditions.

An on-chip low dropout linear regulator has been incorporated into the design to give excellent noise rejection up to several MHz. Higher frequency power supply noise is removed by the external 470 pF decoupling capacitor connected to PINK.

The circuit is designed for PIN photodiodes in the “grounded cathode” configuration, with the anode connected to the input of the TIA and the cathode connected to AC ground, such as the provided PINK terminal. Reverse DC bias is applied to reduce the photodiode capacitance. Avalanche photodiodes can be connected externally to a higher voltage.

### 3.2.2 AGC

The M02016 has been designed to operate over the input range of +6 dBm to –29 dBm. This represents a ratio of 1:3000 whereas the acceptable dynamic range of the output is only 1:30 which implies a compression of 100:1 in the transimpedance. The design uses a MOS transistor operating as a “voltage controlled resistor” to achieve the transimpedance variation.

Another feature of the AGC is that it only operates on signals greater than –22 dBm (@ 0.9 A/W). This knee in the gain response is important when setting “signal detect” functions in the following post amplifier. It also aids in active photodiode alignment.

The AGC pad allows the AGC to be disabled during photodiode alignment by grounding the pad through a low impedance. The AGC control voltage can be monitored during normal operation at this pad by a high impedance (>10 M $\Omega$ ) circuit.

### 3.2.3 Output Stage

The signal from the TIA enters a phase splitter followed by a DC-shift stage and a pair of voltage follower outputs. These are designed to drive a differential (100 $\Omega$ ) load. They are stable for driving capacitive loads, such as interstage filters. Each output has its own GND pad, all four GND pads on the chip should be connected for proper operation. Since the M02016 exhibits rapid roll-off (3 pole), simple external filtering is sufficient.

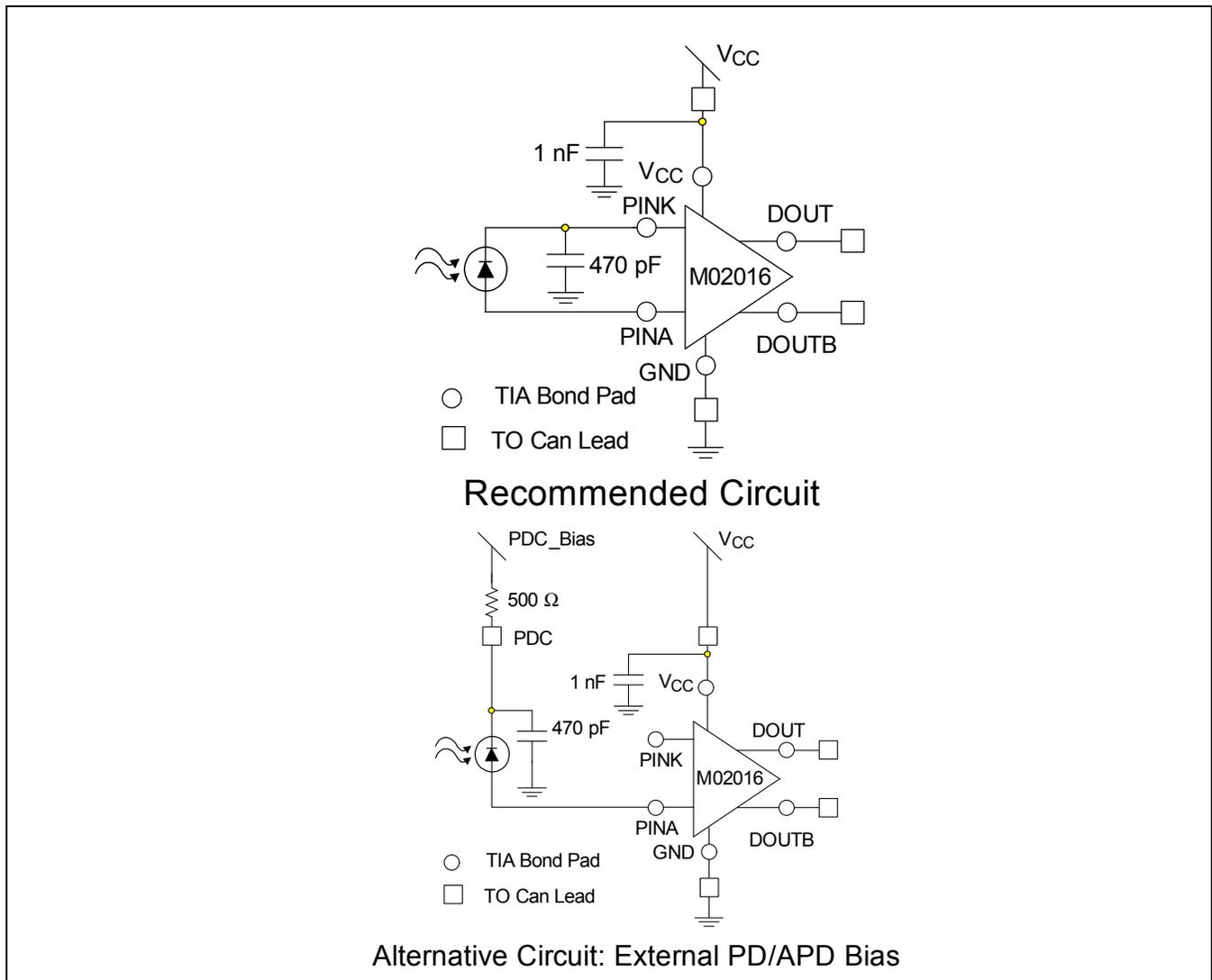
### 3.2.4 Monitor O/P

High impedance output sources a replica average photodiode current for photo-alignment use. The accuracy of this signal does not meet the DDMI Receive Power Specification (SFP-8472) and it is not intended be used as such. It is possible to use the MACOM M0204x/50 limiting amplifiers’ RxAVG<sub>IN</sub> pin to bias the photodiode cathode to provide an SFP-8472 compliant monitoring function. Ensure that the voltage on V<sub>MON</sub> is in the range of 1V to V<sub>CC</sub>.

## 4.0 Applications Information

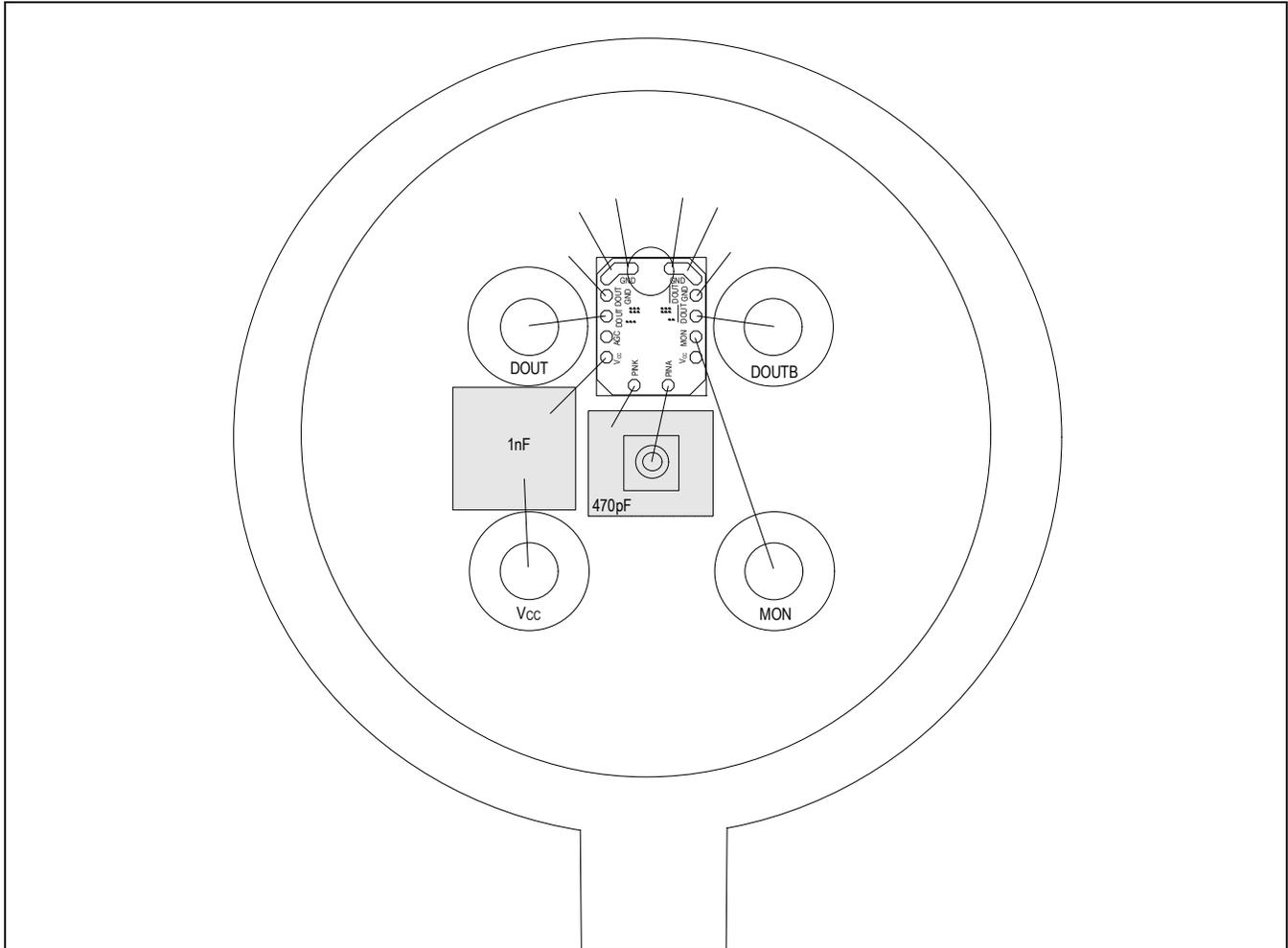
### 4.1 Recommended Pin Diode Connections

Figure 4-1. Suggested PIN Diode Connection Methods



## 4.2 TO-Can Layout

Figure 4-2. Typical Layout Diagram



**Notes:**

Typical application inside of a 5 lead TO-Can.

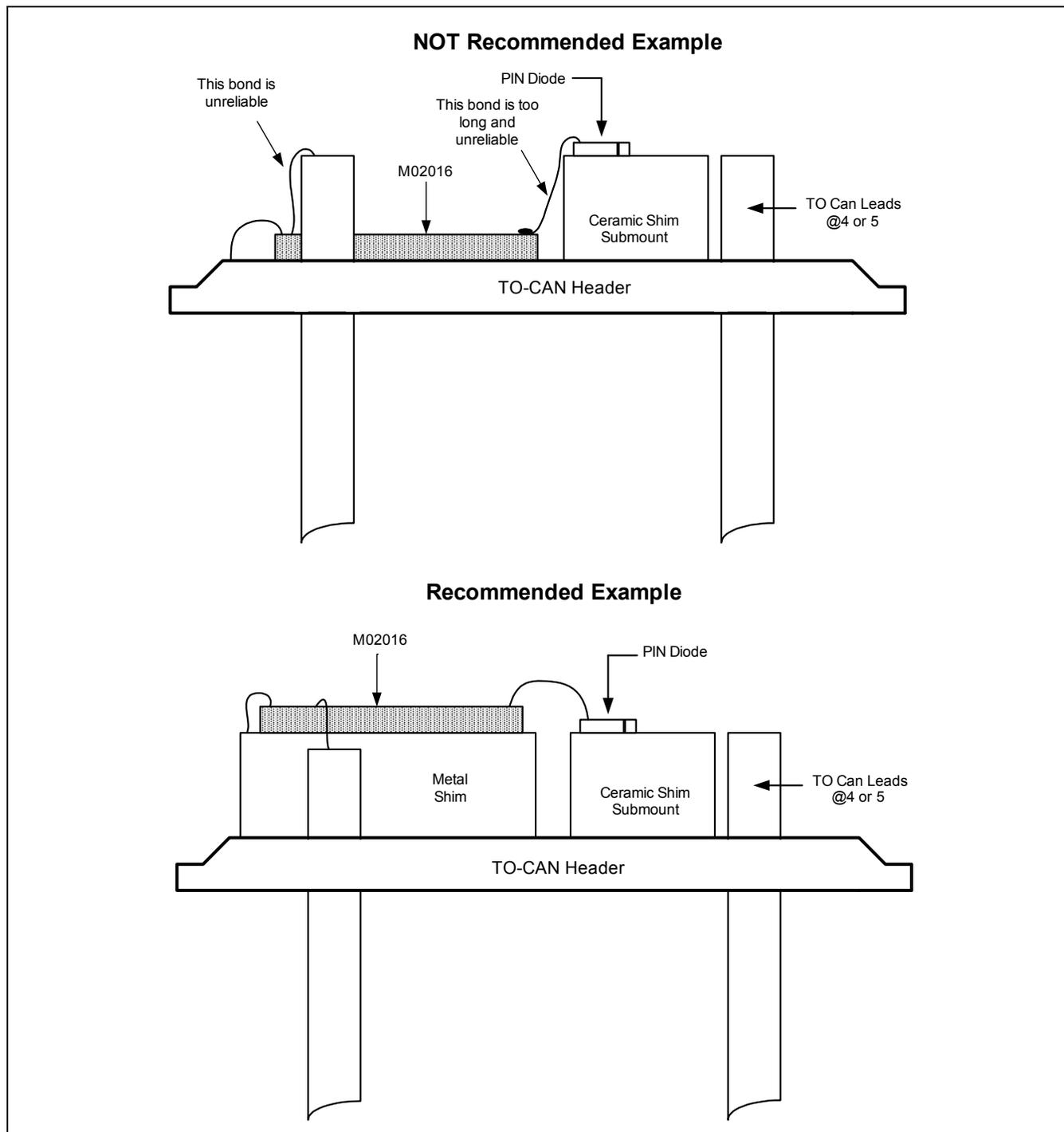
Only one of the  $V_{CC}$  pads and one of the GND pads need to be connected (though in noisy environments two or more GND pads connected may improve performance). The backside must be connected to the lowest potential, usually ground, with conductive epoxy or a similar die attach material. If a monitor output is not required then a 4 lead TO-Can may be used.

## 4.3 Treatment of PINK

PINK requires bypassing to ground with a capacitor when powering a photo diode. If PINK is not used to bias the photo diode, then it is not necessary to bypass an unused PINK.

## 4.4 TO-Can Assembly Recommendations

Figure 4-3. TO-Can Assembly Diagram



### 4.4.1 Assembly

The M02016 is designed to work with a wirebond inductance of 1 nH  $\pm$ 0.25 nH. Many existing TO-Can configurations will not allow wirebond lengths that short, since the PIN diode submount and the TIA die are more than 1 mm away in the vertical direction, due to the need to have the PIN diode in the correct focal plane. This can be remedied by raising up the TIA die with a conductive metal shim. This will effectively reduce the bond wire length. Refer to [Figure 4-3](#) for details.

MACOM recommends ball bonding with a 1 mil (25.4  $\mu$ m) gold wire. For performance reasons the PINA pad is smaller than the others and also has less via material connected to it. It therefore requires more care in setting of the bonding parameters. **For the same reason PINA has no ESD protection.**

In addition, please refer to the MACOM Product Bulletin on Recommended Assembly Procedures (document number 0201x-PBD-002-A). Care must be taken when selecting chip capacitors, since they must have good low ESR characteristics up to 1.0 GHz. It is also important that the termination materials of the capacitor be compatible with the attach method used.

For example, Tin/Lead (Pb/Sn) solder finish capacitors are incompatible with silver-filled epoxies. Palladium/Silver (Pd/Ag) terminations are compatible with silver filled epoxies. Solder can be used only if the substrate thick-film inks are compatible with Pb/Sn solders.

### 4.4.2 Recommended Assembly Procedures

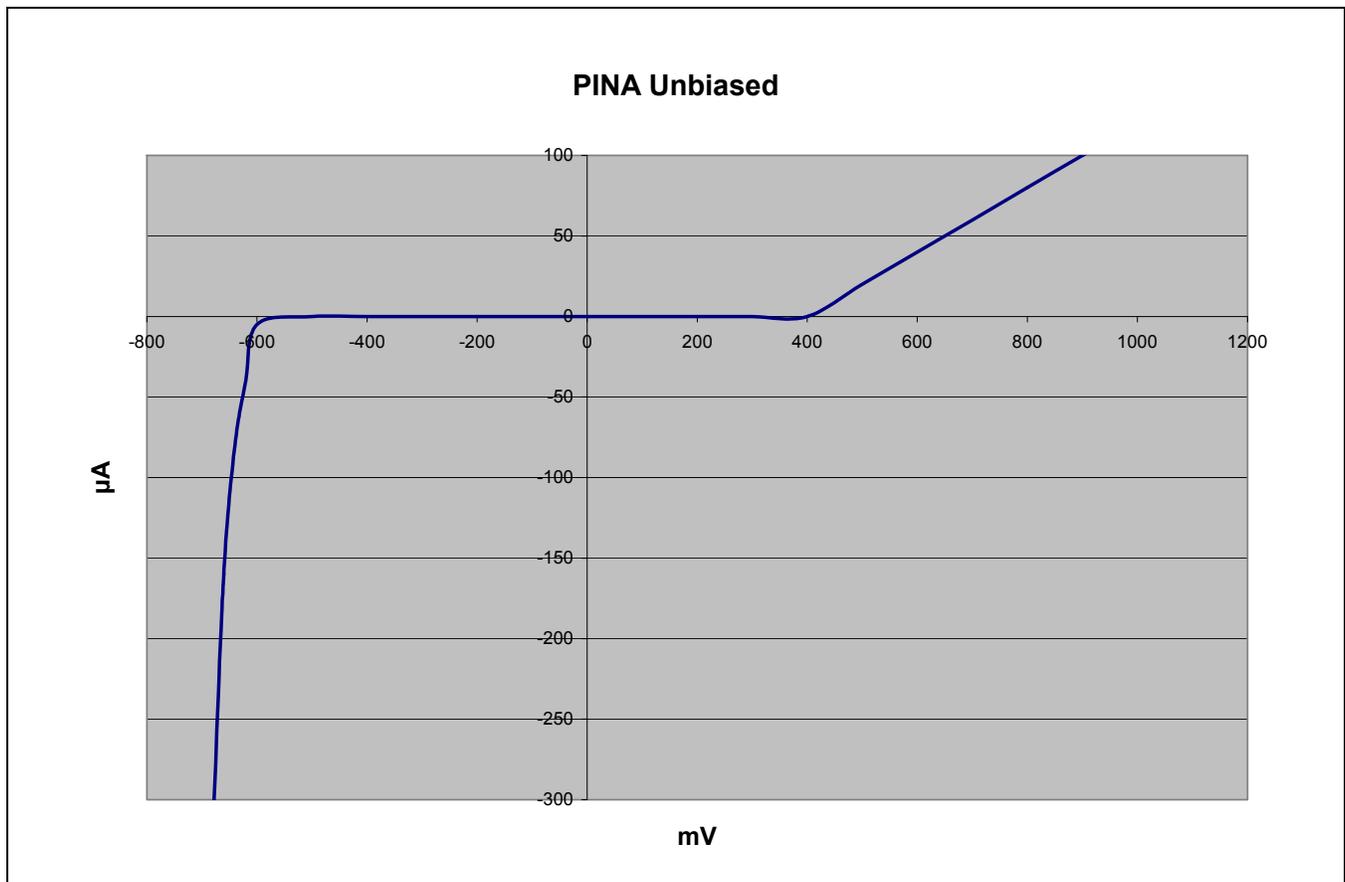
For ESD protection the following steps are recommended for TO-Can assembly:

- a. Ensure good humidity control in the environment (to help minimize ESD).
  - b. Consider using additional ionization of the air (also helps minimize ESD).
  - c. It is best to ensure that the body of the TO-can header or the ground lead of the header is grounded through the wire-bonding fixture. The best solution will ensure that the  $V_{CC}$  lead of the TO-Can is also grounded. When this is done and the procedure below is followed, the photodiode will help reduce the impact to PINA of any positive charge on the wire bonder when bonding to PINA, which is the very last bond placed. (Because the PD is already bonded to PINK and PINK has an internal ESD diode between itself and  $V_{CC}$ , if  $V_{CC}$  is grounded, this will help protect PINA.)
  - d. The most reliable protection to prevent ESD damage on the die is to assure that the wirebonder (including the spool, clamp, etc.) is properly grounded.
1. Wire bond the ground pad(s) of the die first.
  2. Then wire bond the VCC pad to the TO-Can lead.
  3. Then wire bond any other pads going to the TO-Can leads (such as DOUT, DOUT and possibly MON)
  4. Next wire bond any capacitors inside the TO-Can.
  5. Inside the TO-can, wire bond PINK.
  6. The final step is to wire bond PINA.

## 4.5 TIA Use with Externally Biased Detectors

In some applications, MACOM TIAs are used with detectors biased at a voltage greater than available from TIA PIN cathode supply. This works well if some basic cautions are observed. When turned off, the input to the TIA exhibits the following I/V characteristic:

Figure 4-4. TIA Use with Externally Biased Detectors, Powered Off



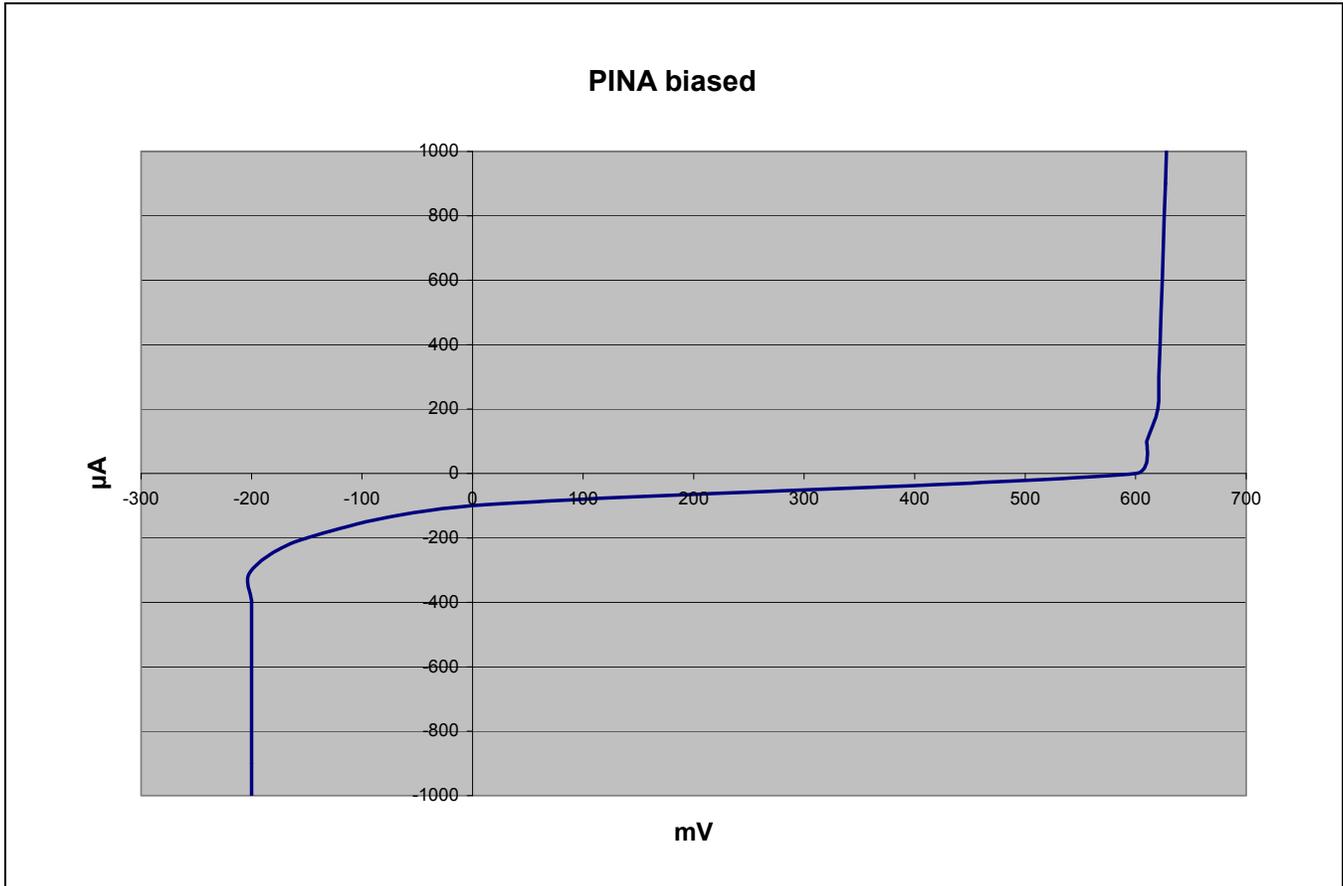
In the positive direction the impedance of the input is relatively high.

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After the TIA is turned on, the DC servo and AGC circuits attempt to null any input currents (up to the absolute maximum stated in [Table 1-1](#)) as shown by the I/V curve in [Figure 4-5](#).

**Figure 4-5. TIA Use with Externally Biased Detectors, Powered On**

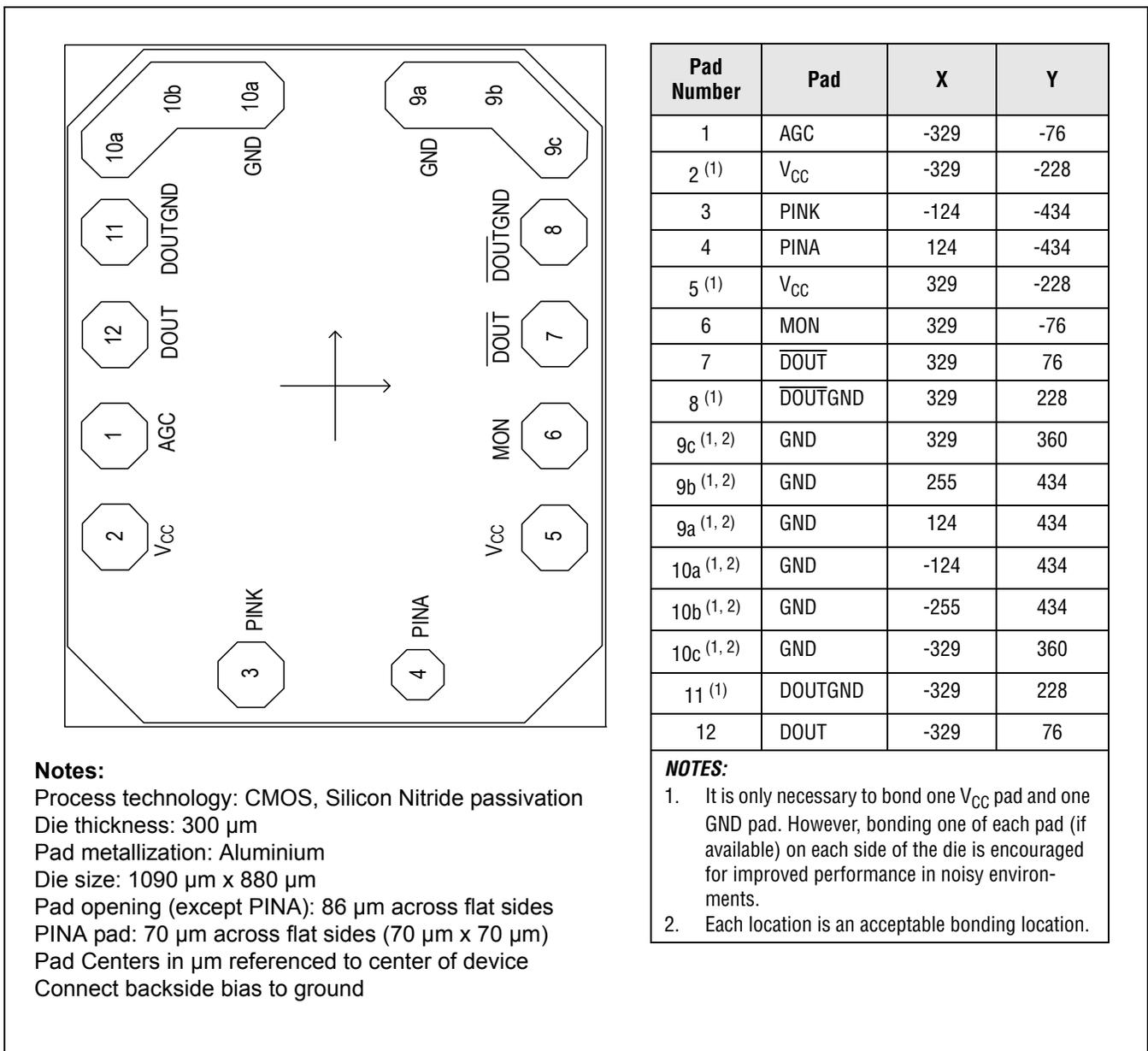


It can be seen that any negative voltage below 200 mV is nulled and that any positive going voltage above the PINA standing voltage is nulled by the DC servo. The DC servo upper bandwidth varies from part to part, but is generally at least 30 kHz.

When externally biasing a detector such as an APD where the supply voltage of the APD exceeds that for PINA [Table 1-1](#), care should be taken to power up the TIA first and to keep the TIA powered up until after the power supply voltage of the APD is removed. Failure to do this with the TIA unpowered may result in damage to the input FET gate at PINA. In some cases the damage may be very subtle, in that nearly normal operation may be experienced with the damage causing slight reductions in bandwidth and corresponding reductions in input sensitivity.

## 5.0 Die Specification

Figure 5-1. Bare Die Information



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