

ADSP-TS201S EZ-KIT Lite[®]

Evaluation System Manual

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The ADSP-TS201S EZ-KIT Lite evaluation system has been certified to comply with the essential requirements of the European EMC directive 89/336/EEC (inclusive 93/68/EEC) and, therefore, carries the “CE” mark.

The ADSP-TS201S EZ-KIT Lite evaluation system had been appended to Analog Devices Development Tools Technical Construction File referenced “DSPTOOLS1” dated December 21, 1997 and was awarded CE Certification by an appointed European Competent Body and is on file.



The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.



CONTENTS

PREFACE

Purpose of This Manual	xii
Intended Audience	xii
Manual Contents	xii
What's New in This Manual	xiii
Technical or Customer Support	xiv
Supported Processors	xiv
Product Information	xv
MyAnalog.com	xv
Processor Product Information	xv
Related Documents	xvi
Online Technical Documentation	xvii
Accessing Documentation From VisualDSP++	xviii
Accessing Documentation From Windows	xviii
Accessing Documentation From Web	xix
Printed Manuals	xix
VisualDSP++ Documentation Set	xix
Hardware Tools Manuals	xix
Processor Manuals	xx

CONTENTS

Data Sheets	xx
Notation Conventions	xxi

USING ADSP-TS201S EZ-KIT LITE

Package Contents	1-2
Default Configuration	1-3
Installation and Session Startup	1-5
Evaluation License Restrictions	1-7
Memory Map	1-7
SDRAM Interface	1-8
Flash Memory	1-9
Programmable FLAG Pins	1-10
Interrupt Pins	1-11
Audio Interface	1-12
Processor Link Ports	1-12
Example Programs	1-13
Flash Programmer Utility	1-14

ADSP-TS201S EZ-KIT LITE HARDWARE REFERENCE

System Architecture	2-2
External Port	2-3
Expansion Interface	2-3
JTAG Emulation Port	2-4
Switch Settings	2-5
Audio Amplification Selection (SW1)	2-5

Processor Mode Selections (SW2)	2-6
Processor Boot Strap Settings	2-7
SYSCON/SDRCON Mode Settings	2-7
Interrupt Enable Settings	2-8
Link Port Width Settings	2-8
FLAGS and IRQs Switch Settings (SW10)	2-9
Configuration Resistors	2-10
Processor ID Settings	2-10
Clock Mode Settings	2-12
Control Impedance Selection	2-14
Drive Strength Selection	2-15
LEDs and Push Buttons	2-16
Power LED (LED1)	2-16
Reset LED (LED8)	2-16
FLAG LEDs (LED3–6)	2-17
USB Monitor LED (ZLED3)	2-18
Programmable FLAG Push Buttons (SW6–9)	2-18
Interrupt Push Buttons (SW4 and SW5)	2-19
Reset Push Button (SW3)	2-19
Connectors	2-20
Audio (J9 and J10)	2-21
Power (J8)	2-21
JTAG (ZP4)	2-21
USB (ZJ1)	2-22

CONTENTS

Expansion Interface (J1–3)	2-22
Link Ports (J4–7)	2-23
Power Supply Specifications	2-23

ADSP-TS201 EZ-KIT LITE BILL OF MATERIALS

ADSP-TS201S EZ-KIT LITE SCHEMATIC

Title Page	B-1
Processor A	B-2
Processor B	B-3
Processor Link Ports	B-4
Processor Power	B-5
Configuration	B-6
Memory	B-7
Audio In	B-8
Audio Out	B-9
Reset/PB/LED	B-10
Expansion Interface	B-11
JTAG/CPLD For Audio	B-12
Power Page 1	B-13
Power Page 2	B-14
Processor Bypass Caps	B-15

INDEX

PREFACE

Thank you for purchasing the ADSP-TS201S EZ-KIT Lite[®], Analog Devices (ADI) evaluation system for TigerSHARC[®] floating-point embedded processors.


The TigerSHARC processor is a static super scalar (SSS) architecture targeted at software-defined radio applications. In these wireless infrastructure applications, the TigerSHARC processor is replacing field-programmable gate arrays (FPGAs) in the chip rate processing applications for third generation cellular. The performance, flexibility, multiprocessing and IO capabilities of the TigerSHARC processor makes it superior to FPGA implementations.

The evaluation board is designed to be used in conjunction with the VisualDSP++[®] development environment to test the capabilities of the ADSP-TS201S TigerSHARC processor. The VisualDSP++ development environment gives you the ability to perform advanced application code development and debug, such as:

- Create, compile, assemble, and link application programs written in C++, C, and ADSP-TS201S assembly
- Load, run, step-in, step-out, step-over, halt, and set breakpoints in application program
- Read and write data and program memory
- Read and write core and peripheral registers
- Plot memory

Access to the ADSP-TS201S processor from a personal computer (PC) is achieved through a USB port or an optional JTAG emulator. The USB interface gives unrestricted access to the ADSP-TS201S processor and the evaluation board peripherals. Analog Devices JTAG emulators offer faster communication between the host PC and target hardware. Analog Devices carries a wide range of in-circuit emulation products. To learn more about Analog Devices emulators and processor development tools, go to <http://www.analog.com/dsp/tools/>.

The ADSP-TS201S EZ-KIT Lite provides example programs to demonstrate the capabilities of the evaluation board.

 The ADSP-TS201S EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. For details about evaluation license restrictions after the 90 days, refer to “[Evaluation License Restrictions](#)” on page 1-7.

Refer to the *VisualDSP++ Installation Quick Reference Card* for details.

The board features:

- Two Analog Devices ADSP-TS201S processors
 - ✓ 500 MHz core clock speed
 - ✓ Configurable core clock mode
- Analog Devices AD1871 96 kHz analog-to-digital converter
 - ✓ Line-in 3.5 mm stereo jack
- Analog Devices AD1854 96 kHz digital-to-analog converter
 - ✓ Line-out 3.5 mm stereo jack
- SDRAM memory
 - ✓ 32 MB (4 MB x 64)

- Flash memory
 - ✓ 512K main flash memory
- USB debugging interface
- Interface connectors
 - ✓ 14-pin emulator connector for JTAG interface
 - ✓ Low Voltage Differential Signaling (LVDS) link ports via RJ-45 connectors
 - ✓ Expansion interface connectors
- General-purpose IO
 - ✓ 4 push button flags (two for each processor)
 - ✓ 2 push button interrupts (one for each processor)
 - ✓ 4 LED FLAG outputs (two for each processor)
- Analog Devices ADP3331, ADP3336, ADP1864, ADP1821, and ADP1823 voltage regulators

The EZ-KIT Lite board contains two external memories: flash memory and SDRAM. The flash memory can be used to store user-specific boot code. By configuring the boot mode switch (SW2) and programming the flash memory, the board can run as a stand-alone unit. The SDRAM is shared by both processors and can be used to store data external to the processors. For more information, see [“Memory Map” on page 1-7](#).

The EZ-KIT Lite board contains an audio interface, facilitating creation of audio signal processing applications.

Additionally, the EZ-KIT Lite board provides expansion connectors, allowing you to connect to the processor’s external port (EP).

Purpose of This Manual

The *ADSP-TS201S EZ-KIT Lite Evaluation System Manual* provides instructions for installing the product hardware (board). The text describes the operation and configuration of the board components and provides guidelines for running your own code on the ADSP-TS201S EZ-KIT Lite. Finally, a schematic and a bill of materials are provided as a reference for future designs.

The product software installation is detailed in the *VisualDSP++ Installation Quick Reference Card*.

Intended Audience

The primary audience of this manual is a programmer who is familiar with Analog Devices processors. This manual assumes that the audience has a working knowledge of the appropriate processor architecture and instruction set. Programmers who are unfamiliar with Analog Devices processors can use this manual but should supplement it with other texts (such as the *ADSP-TS201 TigerSHARC Processor Hardware Reference* and the *ADSP-TS201 TigerSHARC Processor Programming Reference*) that describe your target architecture.

Programmers who are unfamiliar with VisualDSP++ should refer to the VisualDSP++ online Help and user's or getting started guides. For the locations of these documents, see [“Related Documents”](#).

Manual Contents

The manual consists of:

- Chapter 1, “[Using ADSP-TS201S EZ-KIT Lite](#)” on [page 1-1](#)
Provides information on the EZ-KIT Lite from a programmer’s perspective and outlines the board’s memory map.
- Chapter 2, “[ADSP-TS201S EZ-KIT Lite Hardware Reference](#)” on [page 2-1](#)
Provides information on the hardware aspects of the EZ-KIT Lite.
- Appendix A, “[ADSP-TS201 EZ-KIT Lite Bill Of Materials](#)” on [page A-1](#)
Provides a list of components used to manufacture the EZ-KIT Lite board.
- Appendix B, “[ADSP-TS201S EZ-KIT Lite Schematic](#)” on [page B-1](#)
Provides the resources to allow EZ-KIT Lite board-level debugging or to use as a reference design.



Appendix B now is part of the online Help. The PDF version of the *ADSP-TS201S EZ-KIT Lite Evaluation System Manual* is located in the Docs\EZ-KIT Lite Manuals folder on the installation CD. Alternatively, the schematic can be found on the Analog Devices Web site: www.analog.com/processors.

What’s New in This Manual

This edition of the *ADSP-TS201S EZ-KIT Lite Evaluation System Manual* documents ADSP-TS201S EZ-KIT Lite compliance with the RoHS and WEEE directives.

Technical or Customer Support

You can reach Analog Devices, Inc. Customer Support in the following ways:

- Visit the Embedded Processing and DSP products Web site at <http://www.analog.com/processors/technicalSupport>
- E-mail tools questions to processor.tools.support@analog.com
- E-mail processor questions to processor.support@analog.com (World wide support)
processor.europe@analog.com (Europe support)
processor.china@analog.com (China support)
- Phone questions to **1-800-ANALOGD**
- Contact your Analog Devices, Inc. local sales office or authorized distributor
- Send questions by mail to:
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
USA

Supported Processors

The ADSP-TS201S EZ-KIT Lite evaluation system supports the Analog Devices ADSP-TS201S TigerSHARC embedded processors.

Product Information

You can obtain product information from the Analog Devices website, from the product CD-ROM, or from the printed publications (manuals).

Analog Devices is online at www.analog.com. Our Web site provides information about a broad range of products—analog integrated circuits, amplifiers, converters, and embedded processors.

MyAnalog.com

MyAnalog.com is a free feature of the Analog Devices Web site that allows customization of a Web page to display only the latest information on products you are interested in. You can also choose to receive weekly e-mail notifications containing updates to the Web pages that meet your interests. MyAnalog.com provides access to books, application notes, data sheets, code examples, and more.

Registration:

Visit www.myanalog.com to sign up. Click **Register** to use MyAnalog.com. Registration takes about five minutes and serves as means for you to select the information you want to receive.

If you are already a registered user, just log on. Your user name is your e-mail address.

Processor Product Information

For information on embedded processors and DSPs, visit our Web site at www.analog.com/processors, which provides access to technical publications, data sheets, application notes, product overviews, and product announcements.

Product Information

You may also obtain additional information about Analog Devices and its products in any of the following ways.

- E-mail questions or requests for information to
processor.support@analog.com (World wide support)
processor.europe@analog.com (Europe support)
processor.china@analog.com (China support)
- Fax questions or requests for information to
1-781-461-3010 (North America)
+49-89-76903-157 (Europe)

Related Documents

For information on product related development software, see the following publications.

Table 1. Related Processor Publications

Title	Description
<i>ADSP-TS201S Embedded Processor Data Sheet</i>	General functional description, pinout, and timing
<i>ADSP-TS201 TigerSHARC Processor Hardware Reference</i>	Description of internal processor architecture and all register functions
<i>ADSP-TS201 TigerSHARC Processor Programming Reference</i>	Description of all allowed processor assembly instructions

Table 2. Related VisualDSP++ Publications

Title	Description
<i>VisualDSP++ User's Guide</i>	Description of VisualDSP++ features and usage
<i>VisualDSP++ Assembler and Preprocessor Manual</i>	Description of the assembler function and commands
<i>VisualDSP++ C/C++ Compiler and Library Manual for TigerSHARC Processors</i>	Description of the compiler function and commands for TigerSHARC processors

Table 2. Related VisualDSP++ Publications (Cont'd)

Title	Description
<i>VisualDSP++ Linker and Utilities Manual</i>	Description of the linker function and commands
<i>VisualDSP++ Loader and Utilities Manual</i>	Description of the loader/splitter function and commands

All documentation is available online. Most documentation is available in printed form.



If you plan to use the EZ-KIT Lite board in conjunction with a JTAG emulator, also refer to the documentation that accompanies the emulator.

Visit the Technical Library Web site to access all processor and tools manuals and data sheets:

<http://www.analog.com/processors/technicalSupport/technicalLibrary/>.

Online Technical Documentation

Online documentation comprises the VisualDSP++ Help system, software tools manuals, hardware tools manuals, processor manuals, the Dinkum Abridged C++ library, and Flexible License Manager (FlexLM) network license manager software documentation. You can easily search across the entire VisualDSP++ documentation set for any topic of interest. For easy printing, supplementary .pdf files of most manuals are provided in the Docs folder on the VisualDSP++ installation CD.

Each documentation file type is described as follows.

If documentation is not installed on your system as part of the software installation, you can add it from the VisualDSP++ CD at any time by running the Tools installation. Access the online documentation from the VisualDSP++ environment, Windows[®] Explorer, or the Analog Devices Web site.

Product Information

File	Description
.chm	Help system files and manuals in Help format
.htm or .html	Dinkum Abridged C++ library and FlexLM network license manager software documentation. Viewing and printing the .html files requires a browser, such as Internet Explorer 5.01 (or higher).
.pdf	VisualDSP++ and processor manuals in Portable Documentation Format (PDF). Viewing and printing the .pdf files requires a PDF reader, such as Adobe Acrobat Reader (4.0 or higher).

Accessing Documentation From VisualDSP++

To view VisualDSP++ Help, click on the **Help** menu item or go to the Windows task bar and navigate to the VisualDSP++ documentation via the **Start** menu.

To view ADSP-TS201S EZ-KIT Lite Help, which is part of the VisualDSP++ Help system, use the **Contents** or **Search** tab of the Help window.

Accessing Documentation From Windows

In addition to any shortcuts you may have constructed, there are many ways to open VisualDSP++ online Help or the supplementary documentation from Windows.

Help system files (.chm) are located in the `Help` folder, and .pdf files are located in the `Docs` folder of your VisualDSP++ installation CD-ROM. The `Docs` folder also contains the Dinkum Abridged C++ library and the FlexLM network license manager software documentation.

Your software installation kit includes online Help as part of the Windows[®] interface. These help files provide information about VisualDSP++ and the ADSP-TS201S EZ-KIT Lite evaluation system.

Accessing Documentation From Web

Download manuals at the following Web site:

<http://www.analog.com/processors/technicalSupport/technicalLibrary/>.

Select a processor family and book title. Download archive (.zip) files, one for each manual. Use any archive management software, such as WinZip, to decompress downloaded files.

Printed Manuals

For general questions regarding literature ordering, call the Literature Center at 1-800-ANALOGD (1-800-262-5643) and follow the prompts.

VisualDSP++ Documentation Set

To purchase VisualDSP++ manuals, call 1-603-883-2430. The manuals may be purchased only as a kit.

If you do not have an account with Analog Devices, you are referred to Analog Devices distributors. For information on our distributors, log onto <http://www.analog.com/salesdir/continent.asp>.

Hardware Tools Manuals

To purchase EZ-KIT Lite and in-circuit emulator (ICE) manuals, call 1-603-883-2430. The manuals may be ordered by title or by product number located on the back cover of each manual.

Product Information

Processor Manuals

Hardware reference and instruction set reference manuals may be ordered through the Literature Center at **1-800-ANALOGD (1-800-262-5643)**, or downloaded from the Analog Devices Web site. Manuals may be ordered by title or by product number located on the back cover of each manual.




Data Sheets

All data sheets (preliminary and production) may be downloaded from the Analog Devices Web site. Only production (final) data sheets (Rev. 0, A, B, C, and so on) can be obtained from the Literature Center at **1-800-ANALOGD (1-800-262-5643)**; they also can be downloaded from the Web site.


To have a data sheet faxed to you, call the Analog Devices Faxback System at **1-800-446-6212**. Follow the prompts and a list of data sheet code numbers will be faxed to you. If the data sheet you want is not listed, check for it on the Web site.

Notation Conventions

Text conventions used in this manual are identified and described as follows.

Example	Description
Close command (File menu)	Titles in reference sections indicate the location of an item within the VisualDSP++ environment's menu system (for example, the Close command appears on the File menu).
{this that}	Alternative required items in syntax descriptions appear within curly brackets and separated by vertical bars; read the example as <i>this</i> or <i>that</i> . One or the other is required.
[this that]	Optional items in syntax descriptions appear within brackets and separated by vertical bars; read the example as an optional <i>this</i> or <i>that</i> .
[this,...]	Optional item lists in syntax descriptions appear within brackets delimited by commas and terminated with an ellipsis; read the example as an optional comma-separated list of <i>this</i> .
.SECTION	Commands, directives, keywords, and feature names are in text with letter gothic font.
<i>filename</i>	Non-keyword placeholders appear in text with italic style format.
	Note: For correct operation, ... A Note provides supplementary information on a related topic. In the online version of this book, the word Note appears instead of this symbol.
	Caution: Incorrect device operation may result if ... Caution: Device damage may result if ... A Caution identifies conditions or inappropriate usage of the product that could lead to undesirable results or product damage. In the online version of this book, the word Caution appears instead of this symbol.
	Warning: Injury to device users may result if ... A Warning identifies conditions or inappropriate usage of the product that could lead to conditions that are potentially hazardous for the devices users. In the online version of this book, the word Warning appears instead of this symbol.

Notation Conventions

 Additional conventions, which apply only to specific chapters, may appear throughout this document.

1 USING ADSP-TS201S EZ-KIT LITE

This chapter provides specific information to assist you with development of programs for the ADSP-TS201S EZ-KIT Lite evaluation system.

The information appears in the following sections.

- [“Package Contents” on page 1-2](#)
Lists the items contained in your ADSP-TS201S EZ-KIT Lite package.
- [“Default Configuration” on page 1-3](#)
Shows the default configuration of the ADSP-TS201S EZ-KIT Lite.
- [“Installation and Session Startup” on page 1-5](#)
Instructs how to start a new or open an existing ADSP-TS201SEZ-KIT Lite session using VisualDSP++.
- [“Evaluation License Restrictions” on page 1-7](#)
Describes the restrictions of the VisualDSP++ demo license shipped with the EZ-KIT Lite.
- [“Memory Map” on page 1-7](#)
Describes the ADSP-TS201S EZ-KIT Lite board’s memory map.
- [“SDRAM Interface” on page 1-8](#)
Defines the register values needed to configure the external memory for SDRAM access.
- [“Flash Memory” on page 1-9](#)
Describes how to program and use the flash memory.

Package Contents

- [“Programmable FLAG Pins” on page 1-10](#)
Describes the function and use of the programmable flag pins on the EZ-KIT Lite evaluation system.
- [“Interrupt Pins” on page 1-11](#)
Describes the function and use of the interrupt pins on the EZ-KIT Lite evaluation system.
- [“Audio Interface” on page 1-12](#)
Describes how to use and configure the audio interface.
- [“Processor Link Ports” on page 1-13](#)
Describes how to use and configure the link ports.
- [“Example Programs” on page 1-13](#)
Provides information about the example programs included in the ADSP-TS201S EZ-KIT Lite evaluation system.
- [“Flash Programmer Utility” on page 1-14](#)
Provides information on the Flash Programmer utility included with VisualDSP++.

For information on the graphical user interface, including the boot loading, target options, and other facilities of the EZ-KIT Lite system, refer to the online Help.

For detailed information about programming the ADSP-TS201S Tiger-SHARC processor, see the documents referred to as [“Related Documents”](#).

Package Contents

Your ADSP-TS201S EZ-KIT Lite package contains the following items.

- ADSP-TS201S EZ-KIT Lite board
- *VisualDSP++ Installation Quick Reference Card*

- ADSP-TS201S *EZ-KIT Lite Evaluation System Manual* (this document)
- CD containing:
 - ✓ VisualDSP++ software
 - ✓ ADSP-TS201 EZ-KIT Lite debug software
 - ✓ USB driver files
 - ✓ Example programs
- Universal 7.5V DC power supply
- USB 2.0 cable
- Registration card (please fill out and return)

If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or contact Analog Devices, Inc.

Default Configuration

The EZ-KIT Lite evaluation system contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high-energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Store unused EZ-KIT Lite boards in the protective shipping package.



The ADSP-TS201S EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to open your computer case.

Default Configuration

When removing the EZ-KIT Lite board from the package, handle the board carefully to avoid the discharge of static electricity, which may damage some components. [Figure 1-1](#) shows the default DIP switches, connector locations, and LEDs used in installation. Confirm that your board is set up in the default configuration before using the board.

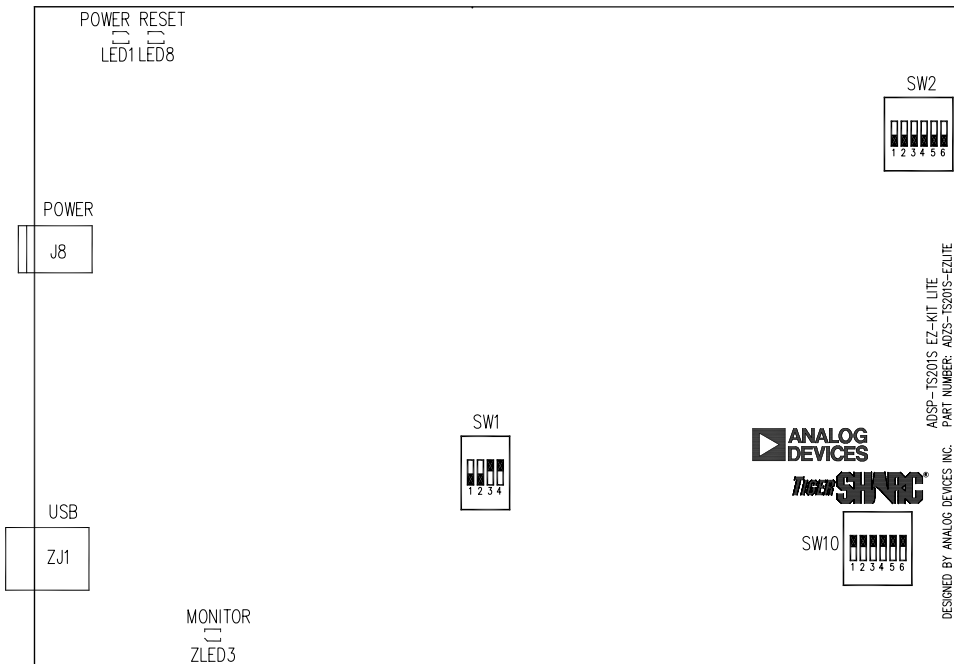



Figure 1-1. EZ-KIT Lite Hardware Setup

Installation and Session Startup

 For correct operation, install the software and hardware in the order presented in the *VisualDSP++ Installation Quick Reference Card*.

1. Verify that the yellow USB monitor LED (ZLED3, located near the USB connector) is lit. This signifies that the board is communicating properly with the host PC and is ready to run VisualDSP++.
2. If you are running VisualDSP++ for the first time, navigate to the VisualDSP++ environment via the **Start** → **Programs** menu. The main window appears. Note that VisualDSP++ does not connect to any session. Skip the rest of this step to step 3.

If you have run VisualDSP++ previously, the last opened session appears on the screen. You can override the default behavior and force VisualDSP++ to start a new session by pressing and holding down the **Ctrl** key while starting VisualDSP++. Do not release the **Ctrl** key until the **Session Wizard** appears on the screen. Go to step 4.

3. To connect to a new EZ-KIT Lite session, start **Session Wizard** by selecting one of the following.
 - From the **Session** menu, **New Session**.
 - From the **Session** menu, **Session List**. Then click **New Session** from the **Session List** dialog box.
 - From the **Session** menu, **Connect to Target**. Then click **New Session** from the **Session List** dialog box.
4. The **Select Processor** page of the wizard appears on the screen. Ensure **TigerSHARC** is selected in **Processor family**. In **Choose a target processor**, select **ADSP-TS201**. Click **Next**.

Installation and Session Startup


5. The **Select Connection Type** page of the wizard appears on the screen. Select **EZ-KIT Lite** and click **Next**.
6. The **Select Platform** page of the wizard appears on the screen. In the **Select your platform** list, select **ADSP-TS201S EZ-KIT Lite via Debug Agent**. In **Session name**, highlight or specify the session name.

The session name can be a string of any length; although, the box displays approximately 32 characters. The session name can include space characters. If you do not specify a session name, VisualDSP++ creates a session name by combining the name of the selected platform with the selected processor. The only way to change a session name later is to delete the session and to open a new session.

Click **Next**.

7. The **Finish** page of the wizard appears on the screen. The page displays your selections. If you are satisfied, click **Finish**. If not, click **Back** to make changes.



To disconnect from a session, click the disconnect button  or select **Session** → **Disconnect from Target**.

To delete a session, select **Session** → **Session List**. Select the session name from the list and click **Delete**. Click **OK**.

Evaluation License Restrictions

The ADSP-TS201S EZ-KIT Lite installation is part of the VisualDSP++ installation. The EZ-KIT Lite is a licensed product that offers an unrestricted evaluation license for the first 90 days. Once the initial unrestricted 90-day evaluation license expires:

- VisualDSP++ allows a connection to the ADSP-TS201S EZ-KIT Lite via the USB debug agent interface only. Connections to simulators and emulation products are no longer allowed.
- The linker restricts a user program to 128K words of internal memory for code space with no restrictions for data space.

Refer to the *VisualDSP++ Installation Quick Reference Card* for details.

Memory Map

The ADSP-TS201S processor has 24 Mbits of internal memory that can be used for program storage or data storage. The configuration of internal memory is detailed in the *ADSP-TS201 TigerSHARC Processor Hardware Reference*.

The ADSP-TS201S EZ-KIT Lite board contains 512K x 8-bit of external flash memory. The memory is divided into eight uniform 64 Kb sections. This memory connects to the processor's \sim BMS and \sim MS0 pins. The flash memory can be accessed in boot memory space as well as the external memory bank zero space.

The board also contains 4M x 64-bit of external SDRAM memory. The SDRAM memory connects to the processor's SDRAM interface.

SDRAM Interface

Table 1-1. EZ-KIT Lite Evaluation Board Memory Map



	Start Address	End Address	Content
Internal Memory	0x0000 0000	0x 0001 FFFF	Internal memory 0
	0x0004 0000	0x0005 FFFF	Internal memory 2
	0x0008 0000	0x0009 FFFF	Internal memory 4
	0x000C 0000	0x000D FFFF	Internal memory 6
	0x0010 0000	0x0011 FFFF	Internal memory 8
	0x0014 0000	0x0015 FFFF	Internal memory 10
	0x001E 0000	0x001E 03FF	Internal registers
	0x001F 0000	0x001F 03FF	SOC registers
	0x0C00 0000	0x0FFF FFFF	Broadcast
	0x1000 0000	0x13FF FFFF	Processor ID 0
	0x1400 0000	0x17FF FFFF	Processor ID 1
	External Memory	0x3000 0000	0x37FF FFFF
0x3800 0000		0x39FF FFFF	External memory space bank 1
0x4000 0000		0x43FF FFFF	External memory space (MSSD0); MSSD0 includes SDRAM which ends at 0x407F FFFF.
0x8000 0000		0xFFFF FFFF	Host

SDRAM Interface

The SDRAM on the EZ-KIT Lite evaluation board is 32 MB. To access SDRAM, the `SYSCON` and `SDRCON` registers must be configured properly. The SDRAM default values are:

- `SYSCON` = 0x00189067
- `SDRCON` = 0x00005983

For the supplied memory, the `SDRCON` register should be configured as follows:

- SDRAM enable, CAS latency of two cycles
 - Pipe depth of zero, page boundary of 256 words
 - Refresh rate of every 3700 cycles, precharge to RAS of two cycles
 - RAS to precharge of five cycles
 - Init sequence is MRS cycle follows refresh
-  The `SYSCON` and `SDRCON` registers define bus control configuration. They can be written only once after reset and cannot be changed during system operation.
-  In emulation space, the `SYSCON` and the `SDRCON` registers can be written to as many times as needed. The USB debug monitor operates in emulation space and allows “always writable” mode for these registers.

Flash Memory

The AT49BV040 chip provides a total of 512K x 8-bits of external flash memory, arranged into eight uniform 64 Kb memory blocks. The block addresses are shown in [Table 1-2](#).

Table 1-2. Flash Memory Map

Start Address	End Address	Content
0x3000 0000	0x3000 FFFF	Uniform block 0
0x3001 0000	0x3001 FFFF	Uniform block 1
0x3002 0000	0x3002 FFFF	Uniform block 2
0x3003 0000	0x3003 FFFF	Uniform block 3

Programmable FLAG Pins

Table 1-2. Flash Memory Map (Cont'd)

Start Address	End Address	Content
0x3004 0000	0x3004 FFFF	Uniform block 4
0x3005 0000	0x3005 FFFF	Uniform block 5
0x3006 0000	0x3006 FFFF	Uniform block 6
0x3007 0000	0x3007 FFFF	Uniform block 7

To program the flash memory with your boot code, first create a loader file from your processor code. You set up the loader in VisualDSP++ depending on how you plan to boot the flash. For information on creating a loader file, refer to VisualDSP++ online help and the *VisualDSP++ Loader and Utilities Manual*.

Next, the loader file must be programmed into the flash memory. This can be done using the VisualDSP++ Flash Programmer utility (see online Help).

Programmable FLAG Pins

Each ADSP-TS201S processor has four programmable flag pins. Two flag pins from each processor (FLAG0 and FLAG1) allow interaction with the running program through the use of a switch (SW6-9). The FLAG2 and FLAG3 pins from each processor are connected to LEDs (LED3-6).

After the processor is reset, the programmable flags are configured as inputs. The direction of each programmable FLAG is configured in the FLAGREG register. If the flag is configured for output, the value of the flag pin is set in the FLAGREG register. If the flag is configured for input, the value on the flag pin is read from the SQSTAT register. Programmable flags are summarized in [Table 1-3](#). For more information on how to configure the programmable flag pins, see the *ADSP-TS201S TigerSHARC Processor Hardware Reference*.

Table 1-3. Programmable FLAG Pin Summary

FLAG	Connection	Description
FLAG0_A	SW9	The FLAG0 and FLAG1 pins connect to the push buttons to supply feedback for program execution. For instance, you can write user input to trigger a routine when the push button is pressed.
FLAG1_A	SW8	
FLAG0_B	SW6	
FLAG1_B	SW7	
FLAG2_A	LED4	The FLAG2 and FLAG3 pins connect to the LEDs to supply feedback during program execution.
FLAG3_A	LED6	
FLAG2_B	LED5	
FLAG3_B	LED3	

Interrupt Pins

The ADSP-TS201S processor includes four interrupt pins (IRQ3-0) for interaction with the running program. One external interrupt from each processor is directly accessible through push buttons SW4 and SW5 on the EZ-KIT Lite board. Interrupts are summarized in [Table 1-4](#). For more information on configuring the interrupt pins, see the *ADSP-TS201S TigerSHARC Processor Hardware Reference*.

Table 1-4. Interrupt Pin Summary

Interrupt	Connection	Description
IRQ0_A	SW4	The IRQ0 interrupt connects to push buttons to supply feedback for program execution. For instance, you can write your code to perform a different function when an interrupt is detected.
IRQ0_B	SW5	

Audio Interface

The audio interface of the EZ-KIT Lite board allows you to interface with the board's analog-to-digital converter (ADC) and digital-to-analog converter (DAC). The audio interface consists of two main ICs: AD1871 and AD1854.

The AD1871 is a stereo audio ADC intended for digital audio applications requiring high-performance analog-to-digital conversion. The AD1871 provides 97 dB THD+N and 107 dB dynamic range.

The AD1854 is a high-performance, single-chip stereo, audio DAC delivering 113 dB dynamic range and 112 dB SNR at a 48 kHz sample rate.

Because the ADSP-TS201S processor does not have any SPORTs, a Xilinx complex programmable logic device (CPLD) generates the audio interface control signals between the processor and the audio circuit. Setting the FLAG3 signal of processor A high enables the audio interface inside of the CPLD. Once the audio interface has been enabled, the audio data can be transferred to and from the processor by generating a DMAR0 cycle. The audio data interfaces with the processor via the lowest 24 bits of the data bus (D23-0).

A CPLD IO connector (P6) has been added to allow a user to connect to the CPLD and the external port of the ADSP-TS201S (DSP A) processor. Refer to the schematic for information on how the connector is wired to the CPLD. Refer to the audio example program included in the EZ-KIT Lite's installation directory for more information on how to use the audio interface. Refer to [“Audio \(J9 and J10\)” on page 2-21](#) for information about the audio connectors.

Processor Link Ports

The link ports on the ADSP-TS201S processor uses Low Voltage Differential Signaling (LVDS) to communicate with each other. Each processor has a TX (transmit) port and RX (receive) port for each of its link ports. The RJ-45 connectors, J4-5, are the TX and RX ports for processor A. Similarly, J6-7 are TX and RX for processor B. The TX and RX of one processor's link ports should be respectively connected to RX and TX of another processor's link ports. In this manner, the TX of one processor connects to the RX of the other processor.

Connect the link ports with a standard CAT 5E networking cable. The length of the cable may affect the maximum frequency at which the data can be transferred. Refer to the ADSP-TS201S embedded processor data sheet at http://www.analog.com/Uploaded-Files/Data_Sheets/ADSP_TS201S.pdf for more information.

There are four link ports on each of the processors on the EZ-KIT Lite. For each processor, the Link Port 0 transmit signals are connected to the receive of the same Link Port 0 signals. Link ports 2 and 3 connect the transmit of one processor to the receive of the other processor.

Example Programs

Example programs are provided with the ADSP-TS201S EZ-KIT Lite to demonstrate various capabilities of the evaluation board. These programs are installed with the EZ-KIT Lite software and can be found in the ...\\TS\\Examples\\ADSP-TS201 EZ-KIT Lite subdirectory of the VisualDSP++ installation directory. Please refer to the readme file provided with each example program for more information.



When running the examples, do not change the BGEN or NMOD (8 or 9) bits in the SQCTL register. The change can disable communications with the host.

Flash Programmer Utility

The ADSP-TS201S EZ-KIT Lite evaluation system includes a Flash Programmer utility. The utility allows you to program the flash memory on the EZ-KIT Lite. The Flash Programmer is installed with VisualDSP++. Once the utility is installed, it is accessible from the **Tools** pull-down menu.

For more information on the Flash Programmer utility, refer to the online Help.

2 ADSP-TS201S EZ-KIT LITE HARDWARE REFERENCE

This chapter describes the hardware design of the ADSP-TS201S EZ-KIT Lite board. The following topics are covered.

- [“System Architecture” on page 2-2](#)
Describes the configuration of the ADSP-TS201S processor and explains how the board components interface with the EZ-KIT Lite.
- [“Switch Settings” on page 2-5](#)
Shows the location and describes the function of each configuration DIP switch.
- [“Configuration Resistors” on page 2-10](#)
Shows the location and describes the function of each configuration resistor.
- [“LEDs and Push Buttons” on page 2-16](#)
Shows the location and describes the function of the LEDs and push buttons.
- [“Connectors” on page 2-20](#)
Shows the location of and gives the part number for all of the connectors on the board. In addition, provides the manufacturer and part number information for the mating parts.
- [“Power Supply Specifications” on page 2-23](#)
Describes the power connector.

System Architecture

This section describes the processor's configuration on the EZ-KIT Lite board.

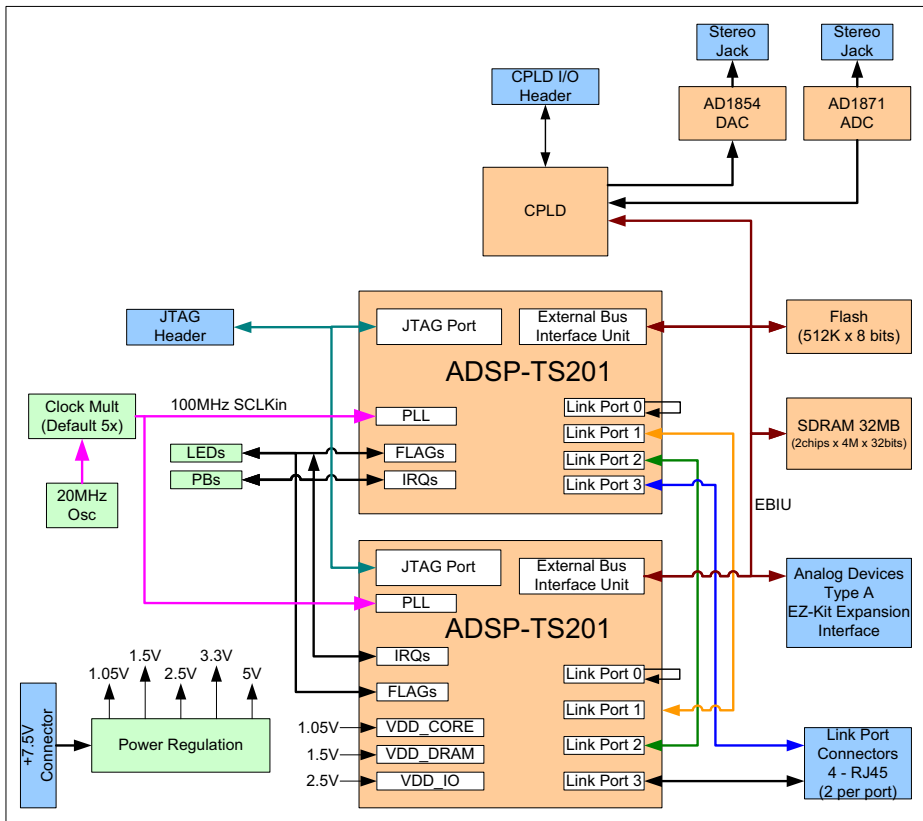


Figure 2-1. System Architecture

This EZ-KIT Lite has been designed to demonstrate the capabilities of the ADSP-TS201S TigerSHARC processor. The processor is powered by three separate regulators for the core, internal DRAM, and IO. The pro-

cessor core voltage is set to 1.05V. The internal DRAM is powered by an external 1.5V regulator. Finally, the external interface (IO) operates at 2.5V but can accept up to 3.3V levels.

A 20 MHz SMT oscillator, in conjunction with a clock generator set to 5x, supply the input clock to the processors. The speed at which the core operates is determined by pull-up and pull-down resistors on both the clock generator (U1) and the SCLKRAT2-0 bit of each of the processors. For more information, see [“Clock Mode Settings” on page 2-12](#). By default, the processor core runs at 500 MHz (20 MHz x 5 (U1) x 5 (SCLKRAT) =500 MHz).

External Port

The external port (EP) connects to a 512K x 8-bit flash memory. The flash memory connects to the boot memory select (~BMS) and memory bank 0 (~MS0) pins. The flash can be used to boot the processor as well as to store information during normal operation. Refer to [“Flash Memory” on page 1-9](#) for more information.

The EP also connects to a 4MB x 64-bit SDRAM. Refer to [“SDRAM Interface” on page 1-8](#) for more information.

Expansion Interface

The expansion interface consists of three connectors. The following table shows the interfaces each connector provides. For the exact pinout of the connectors, refer to [“Expansion Interface” on page B-11](#).


Table 2-1. Expansion Interface Connectors

Connector	Interfaces
J1	5V, GND, address, data

Table 2-1. Expansion Interface Connectors (Cont'd)

Connector	Interfaces
J2	2.5V, GND, SDRAM control signals, flags, IRQs, timers, data
J3	GND, reset, DMA, memory control, CLKOUT, Link Ports signals

When you use the expansion interface, limits to the current and to the interface speed must be taken into consideration. The maximum current limit depends on the regulator capabilities. Additional circuitry can also add extra loading to signals, decreasing their maximum effective speed.

 Analog Devices does not support and is not responsible for the effects of additional circuitry.

JTAG Emulation Port

The JTAG emulation port allows an emulator to access the processor's internal and external memory, as well as the special function registers through a 14-pin header. See [“JTAG \(ZP4\)” on page 2-21](#) for more information about the JTAG connector. To learn more about available emulators, contact Analog Devices as described in [“Product Information”](#).

For more information about the JTAG interface and JTAG custom board design, refer to *EE-68* found at the Analog Devices Web site.

Switch Settings

This section describes the function of the DIP switches SW1, SW2, and SW10. The locations and default settings of the switches are shown in [Figure 2-2](#).

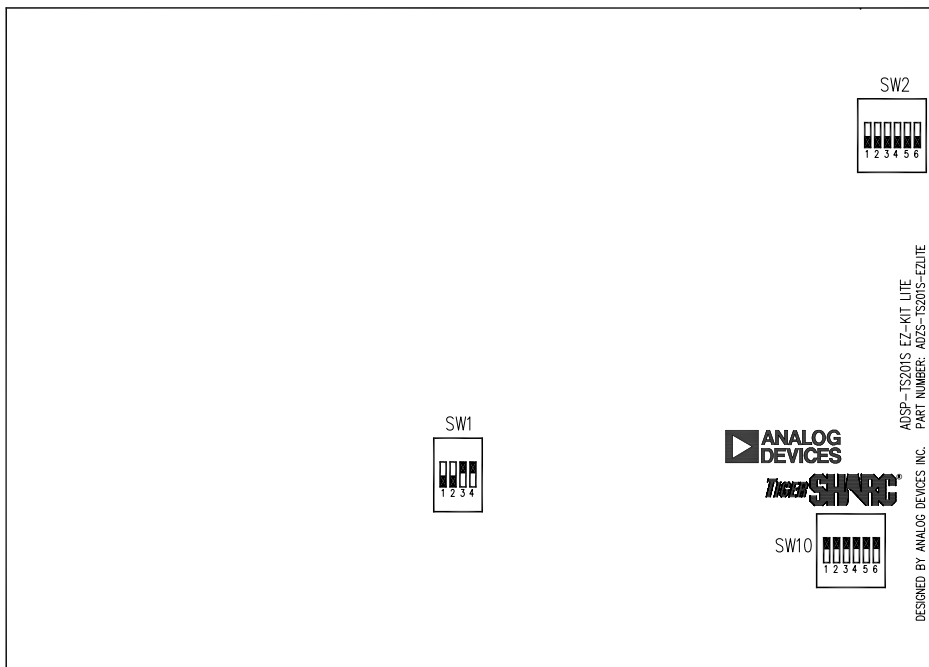


Figure 2-2. Switch Locations

Audio Amplification Selection (SW1)

The SW1 switch determines the amplification of right and left signals connected to the LINE IN connector J9. A non-powered electret microphone can be used by simply varying the switch setting to the values shown in [Table 2-2](#). An amplification gain of a factor of 10 can be achieved by setting the switch into electret microphone use.

Switch Settings

Table 2-2. Audio Amplification Selection (SW1)

Position 1	Position 2	Position 3	Position 4	Audio Amplification Mode
OFF	OFF	ON	ON	No amplification (default)
ON	ON	OFF	OFF	For electret microphone use

Processor Mode Selections (SW2)

The SW2 switch configures several processor strap pins, which in turn, set the processor's operating modes after power up or hard reset:

- “Processor Boot Strap Settings”
- “SYSCON/SDRCON Mode Settings”
- “Interrupt Enable Settings”
- “Link Port Width Settings”

Do not change the switch settings while power is being applied to the board. Many of the strap pin settings can be re-configured in software after the processor is powered up. Refer to the ADSP-TS201S processor data sheet at http://www.analog.com/Uploaded-Files/Data_Sheets/ADSP_TS201S.pdf for more information.

Processor Boot Strap Settings

Position 1 of the SW2 switch determines how the processor boots.

Table 2-3 shows the available boot mode settings. Refer to the ADSP-TS201S processor data sheet at http://www.analog.com/UploadedFiles/Data_Sheets/ADSP_TS201S.pdf for more information.

Table 2-3. Processor Boot Strap Settings (SW2 Position 1)

SW2 Position 1	Boot Mode
OFF	EPROM boot (default)
ON	External boot or link port boot

SYSCON/SDRCON Mode Settings

Position 2 of the SW2 switch determines how the processor handles writes to the SYSCON and SDRCON registers. Table 2-4 shows the available settings for each write type. Refer to the ADSP-TS201S processor data sheet at http://www.analog.com/UploadedFiles/Data_Sheets/ADSP_TS201S.pdf for more information.

Table 2-4. SYSCON/SDRCON Mode Settings (SW2 Position 2)

Position 2	SYSCON/SDRCON Mode
OFF	SYSCON/SDRCON one-time writable (default)
ON	SYSCON/SDRCON always writable



In emulation space, the SYSCON and SDRCON registers can be written to as many times as needed. The USB debug monitor operates in emulation space and allows “always writable” mode for these registers.

Switch Settings

Interrupt Enable Settings

Positions 3 and 5 of the SW2 switch determine how each of the processors handles interrupts. [Table 2-5](#) and [Table 2-6](#) show the available interrupt settings. Refer to the ADSP-TS201S processor data sheet at http://www.analog.com/UploadedFiles/Data_Sheets/ADSP_TS201S.pdf for more information.

Table 2-5. Interrupt Enable Settings (SW2 Position 3)

SW2 Position 3	Interrupt Enable Mode for Processor A (U11)
OFF	Disable interrupts, level-sensitive mode (default)
ON	Enable interrupts, edge-sensitive mode

Table 2-6. Interrupt Enable Settings (SW2 Position 5)

SW2 Position 5	Interrupt Enable Mode for Processor B (U12)
OFF	Disable interrupts, level-sensitive mode (default)
ON	Enable interrupts, edge-sensitive mode

Link Port Width Settings

Positions 4 and 6 of the SW2 switch determine the link port data width. [Table 2-7](#) and [Table 2-8](#) show the available settings for the two types of link port data widths. Refer to the ADSP-TS201S processor data sheet at http://www.analog.com/UploadedFiles/Data_Sheets/ADSP_TS201S.pdf for more information.

Table 2-7. Link Port Width Settings (SW2 Position 4)

SW2 Position 4	Link Port Data Width for Processor A (U11)
OFF	1-bit link port data width (default)
ON	4-bit link port data width

Table 2-8. Link Port Width Settings (SW2 Position 6)

SW2 Position 6	Link Port Data Width for Processor B (U12)
OFF	1-bit link port data width (default)
ON	4-bit link port data width

FLAGS and IRQs Switch Settings (SW10)

The SW10 switch determines the source of the flag and IRQ signals connected to each of the prospective processors. The source can be modified to drive the nets by either a push button switch or an external source via the expansion header. Refer to “[Programmable FLAG Push Buttons \(SW6–9\)](#)” and “[Interrupt Push Buttons \(SW4 and SW5\)](#)” on page 2-19 for information on the flags, IRQs, and associated push buttons. [Table 2-9](#) shows the available flag and interrupt source settings.

Table 2-9. FLAGS and IRQs Switch Settings (SW10)

DSP A		DSP B		DSP A	DSP B	Use With
Position 1 (FLAG0)	Position 2 (FLAG1)	Position 3 (FLAG0)	Position 4 (FLAG1)	Position 5 (IRQ0)	Position 6 (IRQ0)	
OFF	OFF	OFF	OFF	OFF	OFF	External source
ON ¹	ON	ON	ON	ON	ON	On-board push button switch

1 Default settings

Configuration Resistors

This section describes the configuration resistors of the two TigerSHARC processors. The locations of the configuration resistors and their respective default settings are shown in [Figure 2-3](#).

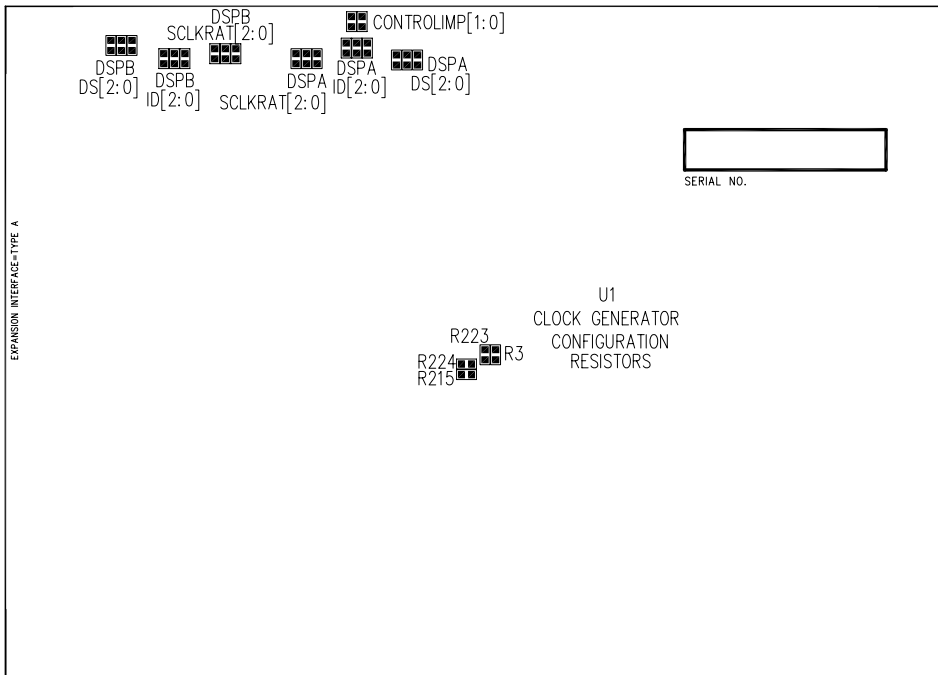


Figure 2-3. Resistor Locations (Bottom View of the Board)

Processor ID Settings

The two ADSP-TS201S processors on the EZ-KIT Lite are factory-configured to set the processor A to an ID value of zero and processor B to an ID value of one. This means that in the cluster, processor A is the master.

ADSP-TS201S EZ-KIT Lite Hardware Reference

Although it is not recommended, the ID value of each processor can be varied by placing 500 Ohm resistors in the appropriate position.

Table 2-10 and Table 2-11 show the available ID settings.



The EZ-KIT Lite must have a processor with the processor ID set to zero (0) on the board. ID0 must be present in order to allow initialization of SDRAM external memory. Internal pull-up or pull-downs on certain pins, such as memory interface and bus arbitration, are enabled only when the ID=(000). Refer to the *ADSP-TS201S TigerSHARC Processor Hardware Reference* for more information.

Table 2-10. Processor A ID Pins Configuration

R115 (Net: ID2_A)	R117 (Net: ID1_A)	R120 (Net: ID0_A)	ID[2:0] Value
Not populated ¹	Not populated	Not populated	0
Not populated	Not populated	Populated	1
Not populated	Populated	Not populated	2
Not populated	Populated	Populated	3
Populated	Not populated	Not populated	4
Populated	Not populated	Populated	5
Populated	Populated	Not populated	6
Populated	Populated	Populated	7

¹ Default settings

Table 2-11. Processor B ID Pins Configuration

R122 (Net: ID2_B)	R123 (Net: ID1_B)	R124 (Net: ID0_B)	ID[2:0] Value
Not populated	Not populated	Not populated	0
Not populated ¹	Not populated	Populated	1
Not populated	Populated	Not populated	2

Configuration Resistors

Table 2-11. Processor B ID Pins Configuration (Cont'd)

R122 (Net: ID2_B)	R123 (Net: ID1_B)	R124 (Net: ID0_B)	ID[2:0] Value
Not populated	Populated	Populated	3
Populated	Not populated	Not populated	4
Populated	Not populated	Populated	5
Populated	Populated	Not populated	6
Populated	Populated	Populated	7

1 Default settings

Clock Mode Settings

The resistors on the clock generator (U1) and the resistors on the SCLKRAT2-0 pins of each of the processors determine the frequency at which the two processors operate. The frequency supplied to CLKIN of the processor also can be changed by replacing the 20 MHz oscillator (U18) shipped with the board with a different oscillator. Ensure that the selected clock mode and frequency do not exceed the minimum and maximum specifications of the ADSP-TS201S processor as noted in the product data sheet.

The final frequency at which the processors operate is determined by the following equation:

$$(\text{Freq of U18}) * (\text{Mult Factor of U1}) * (\text{Mult Factor of SCLKRAT pins}) = \text{Final Oper Freq}$$

The default frequency factory setting is $20 \text{ MHz} * 5 * 5 = 500 \text{ MHz}$.

Table 2-12 through Table 2-14 show the resistor settings for the clock generator and the SCLKRAT pins. For more information on the clock modes, see the ADSP-TS201S processor data sheet at http://www.analog.com/UploadedFiles/Data_Sheets/ADSP_TS201S.pdf.

Table 2-12. Clock Generator (U1) Settings

R215	R224	R3	R223	Multiplication Factor
Not populated	Populated	Not populated	Populated	2
Not populated	Populated	Populated	Populated	3
Not populated	Populated	Populated	Not populated	4
Populated	Populated	Not populated	Populated	4.25
Populated¹	Populated	Populated	Populated	5
Populated	Populated	Populated	Not populated	6
Populated	Not populated	Not populated	Populated	6.25
Populated	Not populated	Populated	Populated	8
Populated	Not populated	Populated	Not populated	Reserved (test mode)

¹ Default settings

Table 2-13. SCLK Ratio Settings for Processor A

R128 (SCLKRAT2)	R127 (SCLKRAT1)	R133 (SCLKRAT0)	Multiplication Factor
Not populated	Not populated	Not populated	4
Not populated¹	Not populated	Populated	5
Not populated	Populated	Not populated	6
Not populated	Populated	Populated	7
Populated	Not populated	Not populated	8
Populated	Not populated	Populated	10

Configuration Resistors

Table 2-13. SCLK Ratio Settings for Processor A

R128 (SCLKRAT2)	R127 (SCLKRAT1)	R133 (SCLKRAT0)	Multiplication Factor
Populated	Populated	Not populated	12
Populated	Populated	Populated	Reserved

1 Default settings

Table 2-14. SCLK Ratio Settings for Processor B

R126 (SCLKRAT2)	R125 (SCLKRAT1)	R45 (SCLKRAT0)	Multiplication Factor
Not populated	Not populated	Not populated	4
Not populated¹	Not populated	Populated	5
Not populated	Populated	Not populated	6
Not populated	Populated	Populated	7
Populated	Not populated	Not populated	8
Populated	Not populated	Populated	10
Populated	Populated	Not populated	12
Populated	Populated	Populated	Reserved

1 Default settings



The processor A and processor B SCLK ratios must be of the same value.

Control Impedance Selection

The CONTROLIMP1 and CONTROLIMP0 resistors set the impedance and driver mode of the processors, as described in [Table 2-15](#). The resistors are used together with the drive strength pins to determine the actual impedance and drive strength. Refer to the ADSP-TS201S processor data sheet at http://www.analog.com/UploadedFiles/Data_Sheets/ADSP_TS201S.pdf for more information.

Table 2-15. Control Impedance Selection

R143 (CONTROLIMP1)	R131 (CONTROLIMP0)	Driver Mode
Populated ¹	Not populated	Normal
Populated	Populated	Pulse mode
Not populated	Not populated	A/D mode
Not populated	Populated	Pulse mode, A/D mode

¹ Default settings

Drive Strength Selection

The DS2-0 pins of each processor determine the digital drive strength as described in [Table 2-16](#) and [Table 2-17](#). Refer to the ADSP-TS201S processor data sheet at

http://www.analog.com/UploadedFiles/Data_Sheets/ADSP_TS201S.pdf for more information.

Table 2-16. Drive Strength Setting for Processor A

R136 (DS2)	R132 (DS1)	R135 (DS0)	Drive Strength	Output Impedance
Populated	Not populated	Populated	11.1%	26 Ohm
Populated	Not populated	Not populated	23.8%	32 Ohm
Populated	Populated	Populated	36.5%	40 Ohm
Populated	Populated	Not populated	49.2%	50 Ohm
Not populated	Not populated	Populated	61.9%	62 Ohm
Not populated¹	Not populated	Not populated	74.6%	70 Ohm
Not populated	Populated	Populated	87.3%	96 Ohm
Not populated	Populated	Not populated	100%	120 Ohm

¹ Default settings

LEDs and Push Buttons

Table 2-17. Drive Strength Setting for Processor B

R138 (DS2)	R139 (DS1)	R137 (DS0)	Drive Strength	Output Impedance
Populated	Not populated	Populated	11.1%	26 Ohm
Populated	Not populated	Not populated	23.8%	32 Ohm
Populated	Populated	Populated	36.5%	40 Ohm
Populated	Populated	Not populated	49.2%	52 Ohm
Not populated	Not populated	Populated	61.9%	62 Ohm
Not populated¹	Not populated	Not populated	74.6%	70 Ohm
Not populated	Populated	Populated	87.3%	96 Ohm
Not populated	Populated	Not populated	100%	120 Ohm

¹ Default settings

LEDs and Push Buttons

This section describes the function of the LEDs and push buttons.

[Figure 2-4](#) shows the locations of the LEDs and push buttons.

Power LED (LED1)

The green LED, LED1, indicates that power is being supplied properly to the board.

Reset LED (LED8)

When LED8 is lit, it indicates that the master reset of all the major ICs is active.

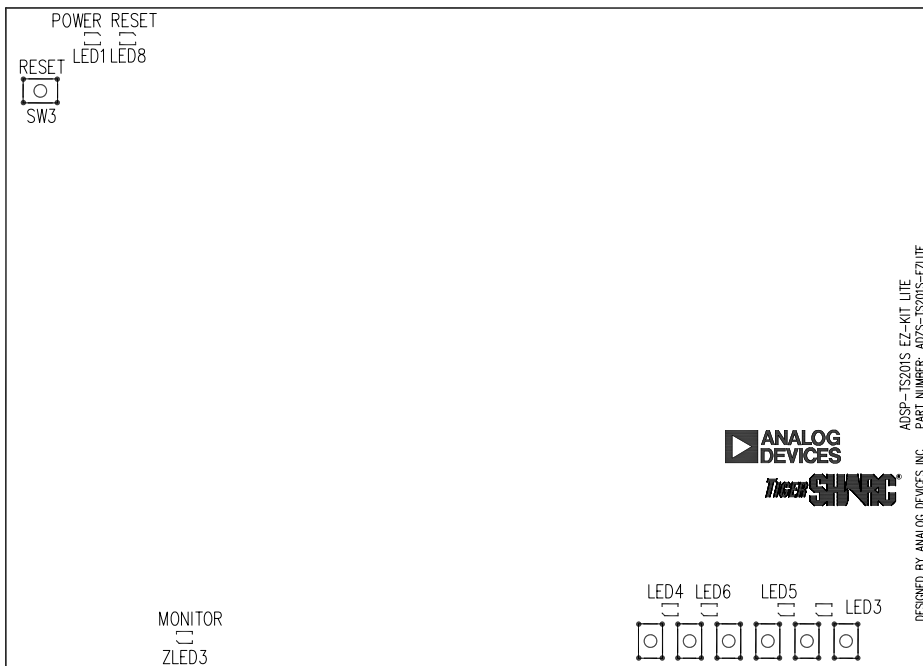


Figure 2-4. LED and Push Button Locations

FLAG LEDs (LED3–6)

The flag LEDs connect to the processor’s programmable FLAG pins (FLAG2 and FLAG3). The LEDs are active high and are lit by an output of “1” from the processor. Refer to [“Programmable FLAG Pins” on page 1-10](#) for information on how to utilize the flags when programming the processor. [Table 2-18](#) shows the FLAG signals and corresponding LEDs.


LEDs and Push Buttons

Table 2-18. FLAG LEDs

FLAG Pin	LED Reference Designator	FLAG Pin	LED Reference Designator
FLAG2_A	LED4	FLAG2_B	LED5
FLAG3_A	LED6	FLAG3_B	LED3

USB Monitor LED (ZLED3)

The USB monitor LED indicates that USB communication has been initialized successfully, allowing you to connect to the processor using VisualDSP++. If ZLED3 is not lit, try resetting the board and/or reinstalling the USB driver.

 When VisualDSP++ is communicating with the EZ-KIT Lite target board, the LED can flicker, indicating communications handshake.

Programmable FLAG Push Buttons (SW6–9)

Four push buttons are provided for general-purpose user input. The SW6–9 push buttons connect to the processor’s programmable FLAG pins. The push buttons are active high and when pressed, send a high (1) to the processor. Refer to [“Programmable FLAG Pins” on page 1-10](#) for more information on how to use the flags. [Table 2-19](#) shows the FLAG signals and corresponding switches.

Table 2-19. FLAG Push Buttons

FLAG Pin	Push Button Reference Designator
FLAG0_A	SW9
FLAG1_A	SW8
FLAG0_B	SW6
FLAG1_B	SW7

Interrupt Push Buttons (SW4 and SW5)

Two push buttons, SW4 and SW5, are provided for user interrupts. The push buttons connect to the processor's interrupt pins. The push buttons are active low and, when pressed, send a low (0) to the processor. Refer to “[Interrupt Pins](#)” on page 1-11 for more information on how to use the interrupts. [Table 2-20](#) shows the interrupt signals and corresponding switches.

Table 2-20. Interrupt Push Buttons

Interrupt Pin	Push Button Reference Designator
IRQ0_A	SW4
IRQ0_B	SW5

Reset Push Button (SW3)

The RESET push button, SW3, resets all ICs on the board, except the USB interface after it has been configured.

Connectors

This section describes the connector functionality and provides information about mating connectors. The connector locations are shown in [Figure 2-5](#).

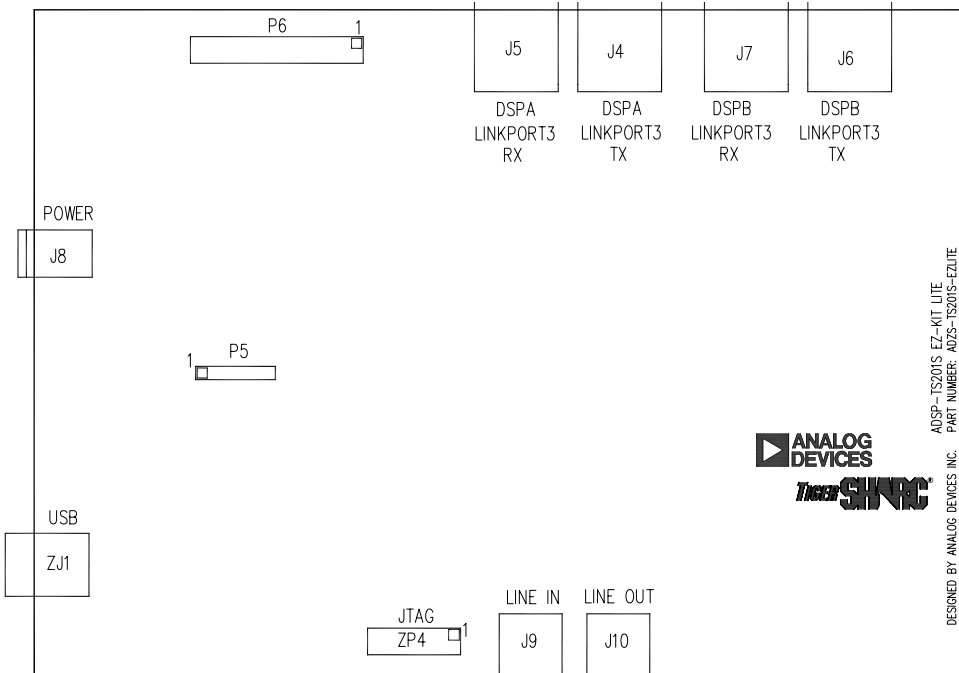


Figure 2-5. Connector Locations

Audio (J9 and J10)

There are two 3.5 mm stereo audio jacks.

Part Description	Manufacturer	Part Number
3.5 mm stereo jack	A/D ELECTRONICS	ST-323-5
Mating Connector		
3.5 mm stereo plug to 3.5 mm stereo cable	RADIO SHACK	L12-2397A



Power (J8)

The power connector provides all the power necessary to operate the EZ-KIT Lite board.

Part Description	Manufacturer	Part Number
2.5 mm power jack	SWITCHCRAFT	RAPC712X
	DIGI-KEY	RAPC712X-ND
Mating Power Supply (shipped with the EZ-KIT Lite)		
7.5V power supply	CUI	DTS075400UDC-P6P-DB

JTAG (ZP4)

The JTAG header is the connecting point for a JTAG in-circuit emulator pod. For more information about a JTAG custom board design or interface, please refer to *EE-68* found at Analog Devices Web site.

-  Pin 3 is missing to provide keying. Pin 3 in the mating connector should have a plug. When an emulator is connected to the JTAG header, the USB debug interface is disabled.
-  When using an emulator with the EZ-KIT Lite board, follow the connection instructions provided with the emulator.

Connectors

USB (ZJ1)

The USB connector is a standard type B USB receptacle.

Part Description	Manufacturer	Part Number
Type B USB receptacle	MILL-MAX	897-43-004-90-000000
	DIGI-KEY	ED90064-ND
Mating Connector		
USB cable (provided with the kit)	ASSMAN	AK672/2-3
	RANDOM	USB-AB-1004A

Expansion Interface (J1–3)

Three board-to-board connectors provide signals for most of the processor's peripheral interfaces. The connectors are located at the bottom of the board. For more information about the expansion interface, see [“Expansion Interface” on page 2-3](#).

Part Description	Manufacturer	Part Number
90-position 0.05” spacing	SAMTEC	SFC-145-T2-F-D-A
Mating Connectors		
90-position 0.05” spacing (through hole)	SAMTEC	TFM-145-x1 series
90-position 0.05” spacing (surface mount)	SAMTEC	TFM-145-x2 series
90-position 0.05” spacing (low cost)	SAMTEC	TFC-145 series

Link Ports (J4–7)

There are four RJ-45 connectors on the EZ-KIT Lite. Two connectors are used for link port 3 of processor A, and two connectors are used for link port 3 of processor B.

Part Description	Manufacturer	Part Number
8-pin RJ-45 connector	TYCO	1-16609214-1
Mating Cables		
BLK CAT 5E cable (1 foot)	E-FILLIATE	119-5136
Gray CAT 5E cable (1 meter)	DIGI-KEY	AE1233-ND

Power Supply Specifications

The power connector supplies DC power to the EZ-KIT Lite board. [Table 2-21](#) shows the power connector pinout.

Table 2-21. Power Connector

Terminal	Connection
Center pin	+7.5 VDC@4 amps
Outer ring	GND

Power Supply Specifications

A ADSP-TS201 EZ-KIT LITE BILL OF MATERIALS

The bill of materials corresponds to “[ADSP-TS201S EZ-KIT Lite Schematic](#)” on page B-1. Please check the latest schematic on the Analog Devices Web site:

<http://www.analog.com/processors/tigersharc/technicalLibrary/manuals/index.html#Evaluation%20Kit%20Manuals>.

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
1	2	74LVC14ASOIC14	U14,U30	TI	74LVC14AD
2	1	IDT74FCT3244-APY SSOP20	U13	IDT	IDT74FCT3244APYG
3	2	SN74AHC1G00 SOT23-5	U31,U38	TI	SN74AHC1G00DBVR
4	1	12.288MHZ OSC003	U2	DIGI-KEY	SG-8002CA-PCC-ND (12.288M)
5	1	MMBT3904SOT23	Q1	MOUSER	512-MMBT3904
6	2	MT48LC4M32B2 TSOP86	U24-25	DIGI-KEY	557-1196-1-ND
7	1	IDT5V928PGI TSSOP24	U1	IDT	IDT5V928PGGI
8	1	TS201S AT49BV040 "U10"	U10	ATMEL	AT49BV040B-70JU
9	4	LMV722MSOIC8	U6-8,U26	NATIONAL SEMI	LMV722MNOPB
10	1	TS201S XC2C384 "U4"	U4	XILINX	XC2C384-10TQG144C

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
11	1	FDC658PSOT23-6	U15	FAIRCHILD	FDC658P
12	2	FDS9926ASOIC8	U16-17	MOUSER	512-FDS9926A
13	2	IRF7832 SOIC8	U20-21	INTERNAT. RECT	IRF7832PBF
14	1	IRF7821 SOIC8	U19	INTERNAT. RECT.	IRF7821PBF
15	1	20MHz OSC003	U18	DIGI-KEY	SG-8002CA-PCC-ND (20.000M)
16	1	ADM708SARZ SOIC8	U5	ANALOG DEVICES	ADM708SARZ
17	1	ADP3331ARTZ SOT23-6	VR4	ANALOG DEVICES	ADP3331ARTZ-REEL7
18	1	AD1854JRSZ SSOP28	U3	ANALOG DEVICES	AD1854JRSZ
19	1	AD1871YRSZ SSOP28	U9	ANALOG DEVICES	AD1871YRSZ
20	1	ADP3336ARMZ MSOP8	VR6	ANALOG DEVICES	ADP3336ARMZ-REEL
21	2	ADSP-TS201SA BP576	U11-12	ANALOG DEVICES	AD91032Z
22	1	ADP1864SOT23-6	VR1	ANALOG DEVICES	ADP1864AUJZ-R7
23	1	ADP1823LFCSP32	VR3	ANALOG DEVICES	ADP1823ACPZ-R7
24	1	ADP1821QSOP16	VR2	ANALOG DEVICES	ADP1821ARQZ-R7
25	5	RUBBERFOOT	M1-5	MOUSER	517-SJ-5018BK
26	1	PWR 2.5MM_JACK CON005	J8	SWITCH- CRAFT	RAPC712X

ADSP-TS201 EZ-KIT Lite Bill Of Materials

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
27	7	MOMENTARY SWT013	SW3-9	PANASONIC	EVQ-PAD04M
28	3	.0545X2 CON019	J1-3	SAMTEC	SFC-145-T2-F-D-A
29	2	DIP6 SWT017	SW2,SW10	CTS	218-6LPST
30	4	RJ45 8PIN CON_RJ45	J4-7	TYCO	1-16609214-1
31	1	DIP4 SWT018	SW1	ITT	TDA04HOSB1
32	1	IDC6X1 IDC6X1	P5	FCI	90726-406HLF
33	1	IDC7X2 IDC7X2	ZP4	FCI	68737-414HLF
34	2	3.5MM STEREO_JACK CON001	J9-10	A/D ELEC- TRONICS	ST-323-5
35	1	IDC13x2 IDC13x2	P6	BERG	54102-T08-13LF
36	1	5A RESETABLE FUS005	F1	MOUSER	650-RGEF500
37	15	0 1/4W 5% 1206	R76,R91,R104, R107,R109-110, R113,R118, R161-164, R178-179,R202	KOA	0.0ECTrk7372BTTED
38	4	YELLOWLED001	LED3-6	PANASONIC	LN1461C
39	1	22PF 50V 5% 0805	C63	AVX	08055A220JAT
40	2	330PF 50V 5% 0805	C25,C30	AVX	08055A331JAT
41	4	0.01UF 100V 10% 0805	C1-2,C7-8	AVX	08051C103KAT2A
42	10	0.1UF 50V 10% 0805	C4,C142-143, C145-149, C153,C249	AVX	08055C104KAT

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
43	4	1000PF 50V 5% 0805	C10-11,C13-14	AVX	08055A102JAT2A
44	27	10K 1/10W 5% 0805	R3,R26,R39-42, R77,R86-87, R89,R94,R100, R102,R108, R112,R116, R153,R158-160, R203,R215, R223-224, R235-236,R238	VISHAY	CRCW080510K0JNEA
45	3	4.7K 1/10W 5% 0805	R5,R93,R188	VISHAY	CRCW08054K70JNEA
46	2	2.0K 1/8W 1% 1206	R156-157	VISHAY	CRCW12062K00FKEA
47	2	49.9K 1/8W 1% 1206	R60,R63	VISHAY	CRCW120649K9FKEA
48	10	100PF 100V 5% 1206	C3,C6,C9,C12, C15,C20-21, C23,C27,C31	AVX	12061A101JAT2A
49	1	2.2UF 35V 10% B	CT15	AVX	TAJB225K035R
50	3	10UF 16V 10% B	CT1-3	AVX	TAJB106K016R
51	6	100 1/10W 5% 0805	R78,R85,R95, R99,R101,R103	VISHAY	CRCW0805100RJNEA
52	2	220PF 50V 10% 1206	C28,C32	AVX	12061A221JAT2A
53	5	600 100MHZ 500MA 1206	FER1-3,FER6-7	STEWARD	HZ1206B601R-10
54	4	237.0 1/8W 1% 1206	R46,R48,R50, R52	VISHAY	CRCW1206237RFKEA
55	2	750.0K 1/8W 1% 1206	R47,R49	VISHAY	CRCW1206750KFKEA

ADSP-TS201 EZ-KIT Lite Bill Of Materials

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
56	8	5.76K 1/8W 1% 1206	R44,R53-57, R150,R152	VISHAY	CRCW12065K76FKEA
57	2	11.0K 1/8W 1% 1206	R61-62	VISHAY	CRCW120611K0FKEA
58	4	120PF 50V 5% 1206	C16-19	AVX	12065A121JAT2A
60	3	1UF 16V 10% 0805	C54,C71-72	PANASONIC	ECJ2FB1E105K
61	1	47PF 100V 10% 1206	C96	KOA	NPO1206HTTD470J
62	1	340.0K 1/8W 1% 0805	R192	VISHAY	CRCW0805-3403FRT1E3
63	1	698.0K 1/8W 1% 0805	R201	VISHAY	CRCW0805698KFKEA
64	2	680PF 50V 1% 0805	C26,C29	AVX	08055A681FAT2A
65	2	2.74K 1/8W 1% 1206	R68,R73	VISHAY	CRCW12062K74FKEA
66	4	5.49K 1/8W 1% 1206	R64-65,R69-70	VISHAY	CRCW12065K49FKEA
67	2	3.32K 1/8W 1% 1206	R66,R71	VISHAY	CRCW12063K32FKEA
68	2	1.65K 1/8W 1% 1206	R67,R72	VISHAY	CRCW12061K65FKEA
69	2	10UF 16V 20% CAP002	CT4-5	PANASONIC	EEE1CA100SR
70	2	68UF 25V 20% CAP003	CT6-7	PANASONIC	EEE-FC1E680P
71	1	332.0K 1/10W 1% 0805	R234	VISHAY	CRCW0805332KFKEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
72	9	0 1/10W 5% 0805	R1,R7,R9-10, R130,R155, R166,R208-209	VISHAY	CRCW08050000Z0EA
73	1	190 100MHZ 5A FER002	FER5	MURATA	DLW5BSN191SQ2
74	2	10UH 10% 1008	L1-2	PANASONIC	ELJ-FC100KF
75	12	22 1/10W 5% 0805	R4,R6,R11,R24, R32,R34-35, R129,R205-207, R219	VISHAY	CRCW080522R0JNEA
76	1	0.47UF 16V 10% 0805	C73	AVX	0805YC474KAT2A
77	7	10UF 6.3V 10% 0805	C33,C57-58, C90-92,C99	AVX	080560106KAT2A
78	6	1000PF 10V 20% 0805	C38-40,C42-43, C45	DIGI-KEY	311-1136-1-ND
79	2	4.7UF 6.3V 10% 0805	C70,C74	AVX	08056D475KAT2A
80	37	0.1UF 10V 10% 0402	C66,C69,C75, C108,C111- 115,C118,C120, C141,C144, C165-166, C182,C184- 185,C187, C197-201, C221-225, C228-231, C237-239,C241	AVX	0402ZD104KAT2A

ADSP-TS201 EZ-KIT Life Bill Of Materials

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
81	43	0.01UF 16V 10% 0402	C49-50,C68, C77-85,C103-104,C107,C109, C129-140, C167,C181, C183,C202-205,C216, C218-220, C227,C232, C240,C242	AVX	0402YC103KAT2A
82	3	10K 1/16W 5% 0402	R184,R189, R197	VISHAY	CRCW040210K0FKED
83	6	0 1/16W 5% 0402	R170-173, R199-200	PANASONIC	ERJ-2GE0R00X
84	1	1.2K 1/16W 5% 0402	R196	PANASONIC	ERJ-2GEJ122X
85	2	4.7K 31MW 5% RNET8	RN3-4	CTS	746X101472JP
86	14	499.0 1/10W 1% 0805	R23,R25,R45, R111,R124, R124,R133, R140-146, R154	VISHAY	CRCW0805499RFKEA
87	2	100UF 10V 10% C	CT20-21	AVX	TPSC107K010R0075
88	44	1000PF 50V 5% 0402	C67,C168-180, C186,C188-196,C206-215, C217,C226, C233-236, C243-246	AVX	04025C102JAT2A
89	1	64.9K 1/10W 1% 0805	R191	VISHAY	CRCW080564K9FKEA
90	2	57.6K 1/4W 1% 1206	R147-148	VISHAY	CRCW120657K6FKEA

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
91	1	210.0K 1/4W 1% 0805	R190	VISHAY	CRCW0805210KFKEA
92	14	1UF16V10%0603	C37,C41,C44, C46,C60-62, C86,C93-95, C101,C105-106	PANASONIC	ECJ-1VB1C105K
93	1	68PF 50V 5% 0603	C53	AVX	06035A680JAT2A
94	1	470PF 50V 5% 0603	C52	AVX	06033A471JAT2A
95	2	100K 1/10W 5% 0603	R169,R183	VISHAY	CRCW0603100KJNEA
96	1	0 1/10W 5% 0603	R105	PHYCOMP	232270296001L
97	1	10 1/10W 5% 0603	R198	VISHAY	CRCW060310R0JNEA
98	2	4700PF 16V 10% 0603	C88,C97	DIGI-KEY	311-1083-2-ND
99	1	10.0K 1/10W 1% 0603	R211	DIGI-KEY	311-10.0KHRTR-ND
100	1	680PF 50V 5% 0603	C65	PANASONIC	ECJ-1VC1H681J
101	1	2200PF 50V 5% 0603	C98	PANASONIC	ECJ-1VB1H222K
102	4	470UF 2V 20% E	CT16,CT19, CT22-23	PANASONIC	EEF-SE0D471R
103	2	15.0K 1/16W 1% 0603	R193,R195	DIGI-KEY	311-15.0KHRTR-ND
104	1	24.9K 1/10W 1% 0603	R92	DIGI-KEY	311-24.9KHTR-ND
105	1	47UF 6.3V 10% B	CT14	NIC COMPO- NENTS	NTC-T476K6.3TRBF

ADSP-TS201 EZ-KIT Life Bill Of Materials

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
106	9	2.0K 1/16W 1% 0603	R37-38,R88, R121,R212, R214,R216-218	PANASONIC	ERJ-3EKF2001V
107	1	0.05 1/2W 1% 1206	R165	SUSUMA	RL16326-R050-F-N
108	3	10UF 16V 10% 1210	C36,C55,C110	AVX	1210YD106KAT2A
109	1	GREENLED001	LED1	PANASONIC	LN1361CTR
110	1	RED LED001	LED8	PANASONIC	LN1261CTR
111	2	1000PF 50V 5% 1206	C47-48	AVX	12065A102JAT2A
112	2	2200PF 50V 5% 1206	C22,C24	AVX	12065A222JAT050
113	1	0.1UF 50V 20% 1206	C5	AVX	12065E104MAT2A
114	2	100K 1/8W 5% 1206	R58-59	VISHAY	CRCW1206100KFKEA
115	6	270 1/8W 5% 1206	R79-82,R90, R151	VISHAY	CRCW1206270RJNEA
116	2	604.0 1/8W 1% 1206	R74-75	PANASONIC	ERJ-8ENF6040V
117	6	1UF 20V 20% A	CT8-13	AVX	TAJA105K020R
118	1	255.0K 1/10W 1% 0603	R168	VISHAY	CRCW06032553FK
119	1	80.6K 1/10W 1% 0603	R167	DIGI-KEY	311-80.6KHRCT-ND
120	1	6.8UH 25% IND009	L3	DIGI-KEY	308-1328-1-ND
121	1	4A SSB43L DO-214AA	D7	VISHAY	SSB43L

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
122	1	250MA BZX84C5V6 SOT23D	D8	MOUSER	512-BZX84C5V6
123	1	200MA BAT54A SOT23D	D6	MOUSER	512-BAT54A
124	3	200MA BAT54 SOT23D	D3-5	MOUSER	512-BAT54
125	1	8.2UH 20% IND012	L5	COILCRAFT	MSS6132-822ML
126	1	10UH 20% IND012	L4	COILCRAFT	MSS6132-103ML
127	1	0.7UH 20% IND010	L6	COILCRAFT	MLC1265-701ML
128	2	1.1K 1/16W 1% 0402	R174-175	PANASONIC	ERJ-2RKF1101X
129	1	18K 1/16W 5% 0402	R176	DIGIKEY	311-18KJRCT-ND
130	1	12.1K 1/16W 1% 0402	R177	DIGIKEY	311-12.1KLRCT-ND
131	1	38.3K 1/10W 1% 0603	R181	DIGIKEY	311-38.3KHRCT-ND
132	1	820 1/16W 5% 0402	R182	DIGIKEY	311-820JRCT-ND
133	1	430 1/16W 1% 0402	R194	DIGIKEY	311-430LRCT-ND
134	1	2.2PF 50V 10% 0402	C100	DIGIKEY	490-1267-1-ND
135	1	1200PF 50V 10% 0402	C89	DIGIKEY	490-1304-1-ND
136	2	330UF 10V 20% D	CT17-18	SANYO	10TPB330M
137	1	82PF 50V 5% 0402	C87	DIGIKEY	490-1290-1-ND

ADSP-TS201 EZ-KIT Lite Bill Of Materials

Ref.	Qty.	Description	Reference Designator	Manufacturer	Part Number
138	3	22000PF 25V 10% 0402	C59,C76,C102	DIGIKEY	490-3252-1-ND
139	1	1500PF 50V 10% 0402	C64	DIGIKEY	490-3245-1-ND
140	1	1UH20%IND011	L7	DIGIKEY	495-1985-1-ND
141	2	5A MBRS540T3G SMC	D1-2	ON SEMI	MBRS540T3G
142	1	8.20K 1/10W 1% 0603	R210	DIGIKEY	541-8.20KHCT-ND
143	1	10.0K 1/16W 1% 0402	R185	DIGIKEY	P10.0KLCT-ND
144	1	1.50K 1/16W 1% 0402	R204	DIGIKEY	P1.50KLCT-ND

A

B

C

D

1

1

2

2

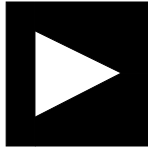
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3

4

4

ADSP-TS201S EZ-KIT Lite

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Title		ADSP-TS201S EZ-KIT LITE TITLE	
Size	Board No.	Rev	
C	A0178-2002	2.1C	
Date	4-9-2007_15:02	Sheet	1 of 15

A

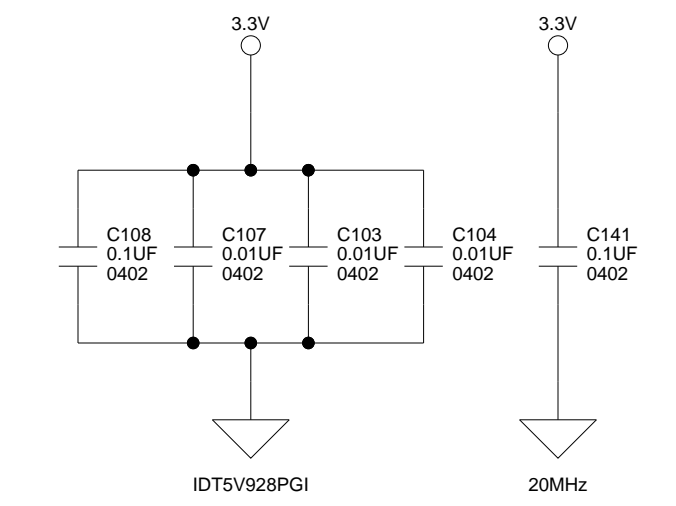
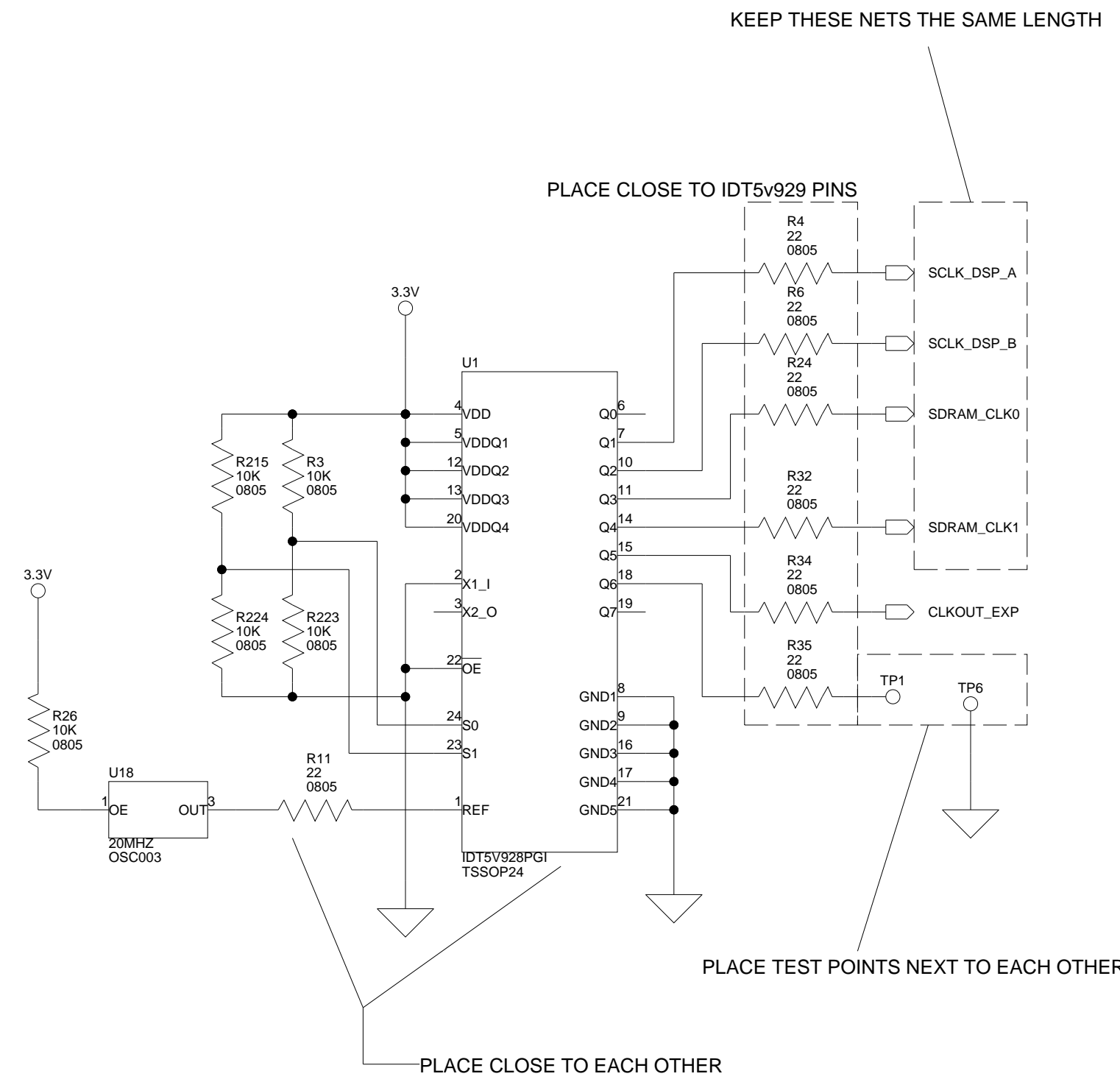
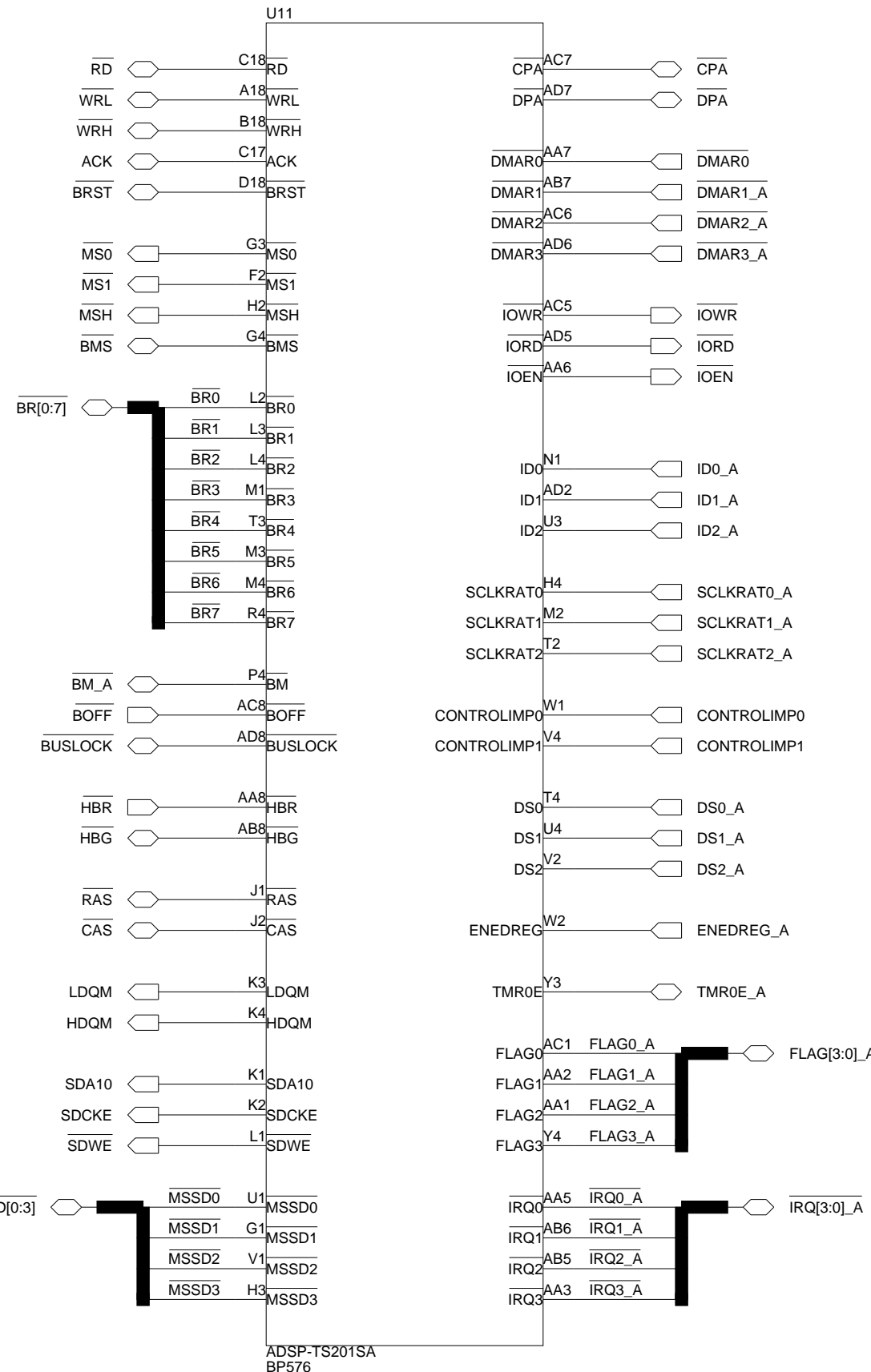
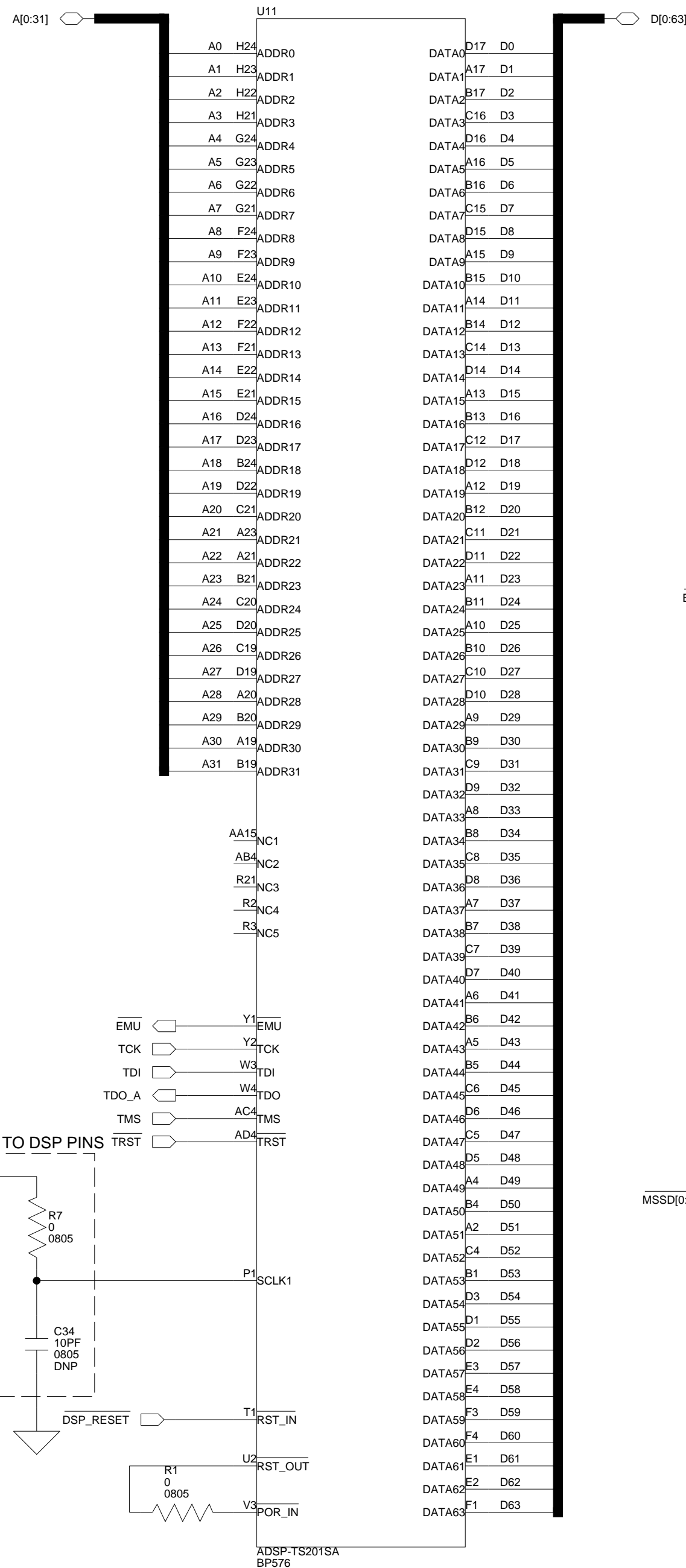
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C

D

DSP A

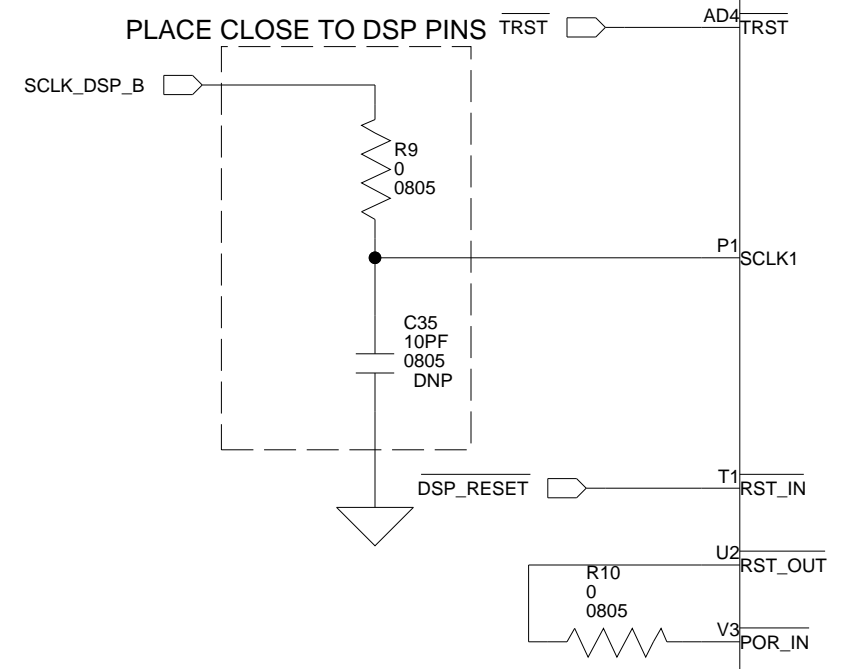
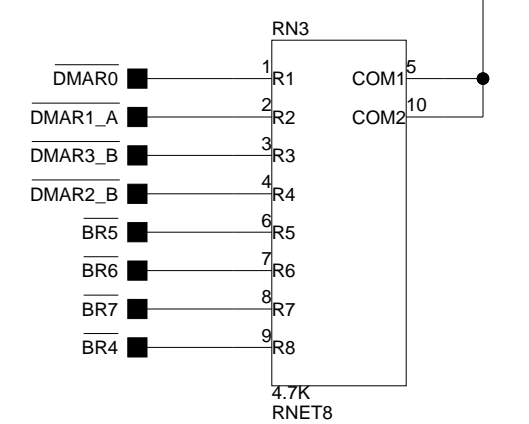
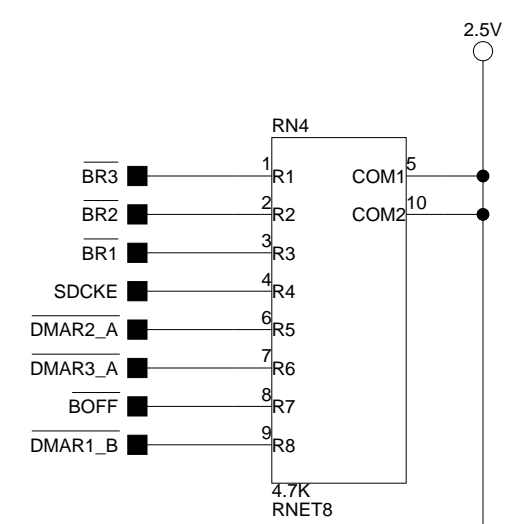
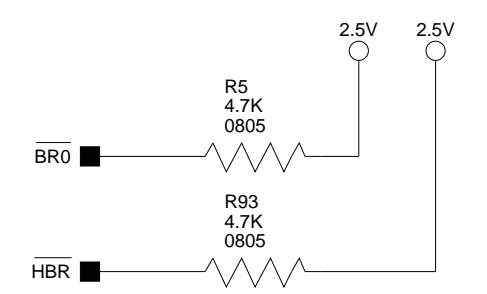
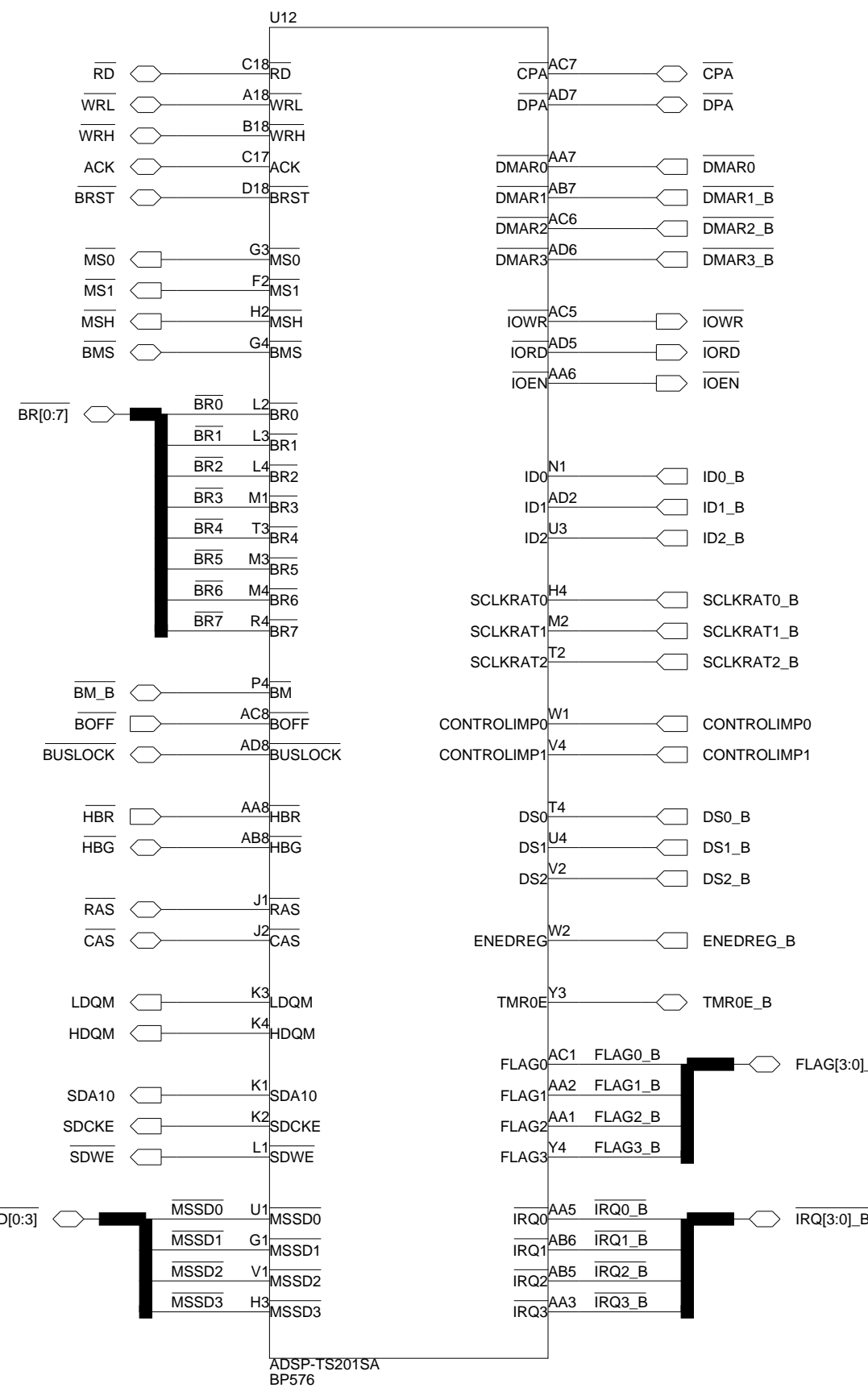
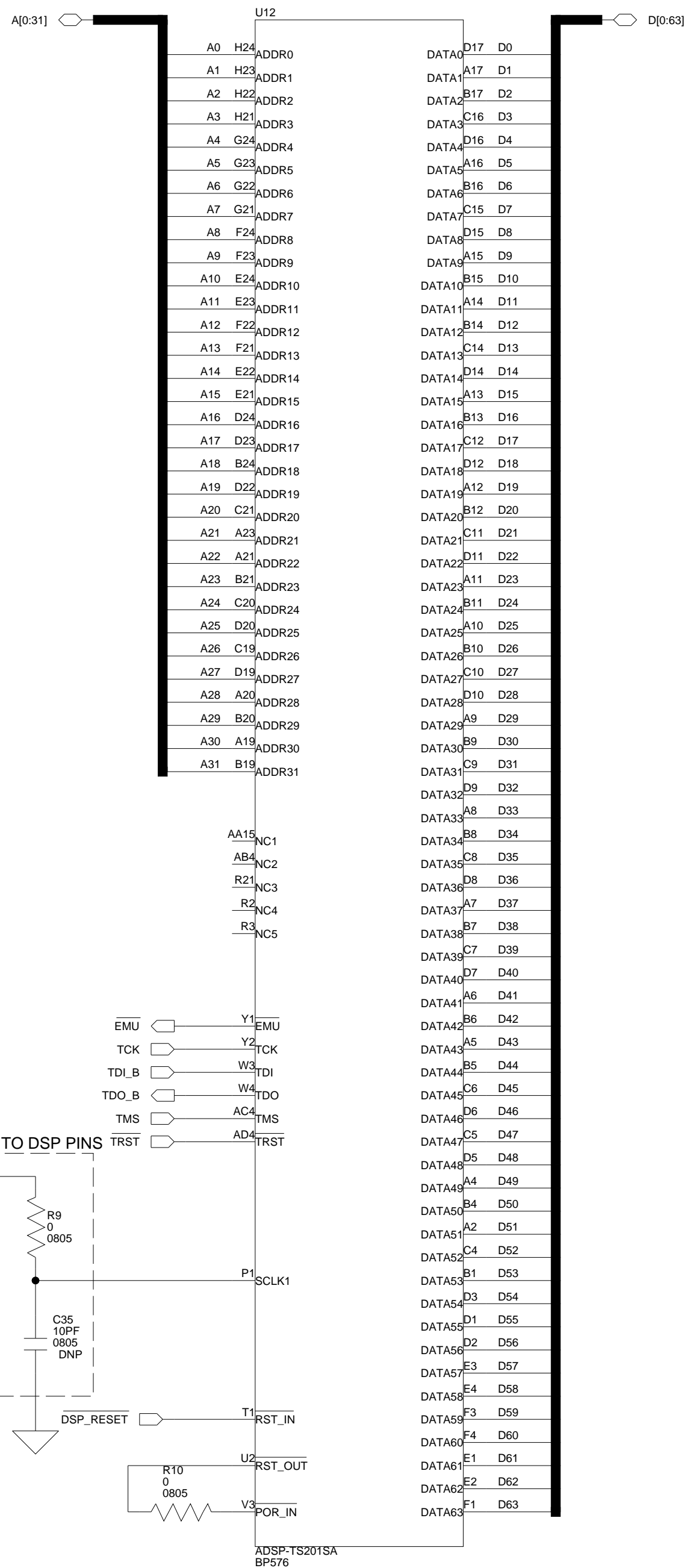
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		Title ADSP-TS201S EZ-KIT LITE DSP A	
Size C	Board No. A0178-2002	Rev 2.1C	
Date 1-10-2007_10:57	Sheet 2 of 15		

DSP B

LABEL "DSP B" near this DSP



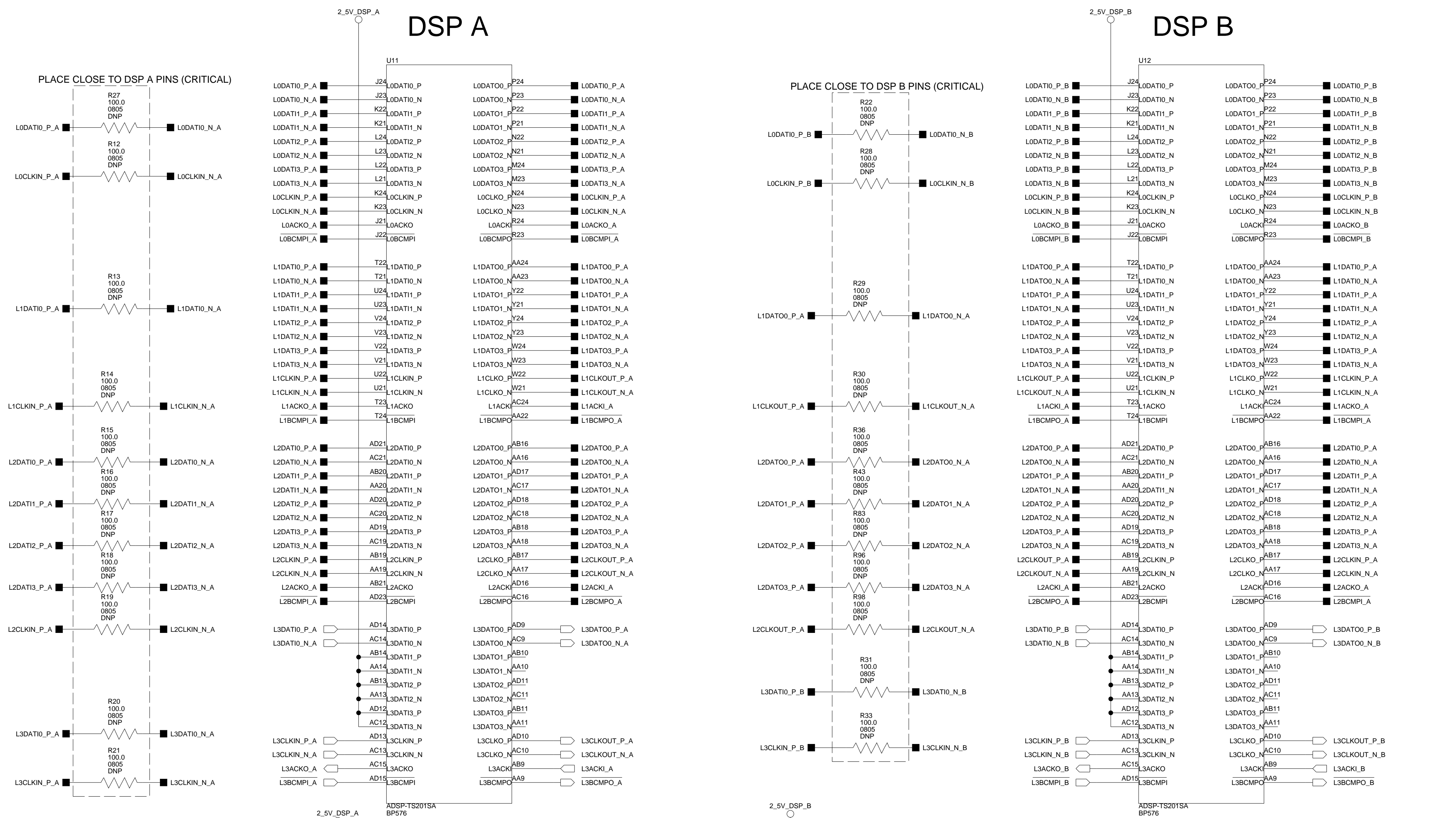
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Size C	Board No.	A0178-2002	
Date	1-10-2007_10:57	Sheet	3 of 15
		Rev	2.1C

ALL NETS ON THIS PAGE EXCEPT L?ACK?_? and L?BCMP?_? ARE DIFFERENTIAL PAIRS
 THESE SIGNAL SHOULD BE ROUTING ACCORDING THE GUIDELINES SET IN EE-179

	DSP A	DSP B
Link Port 0	DSP A	DSP B
Link Port 1	DSP B	DSP A
Link Port 2	DSP B	DSP A
Link Port 3	RJ45	RJ45

DSP A

DSP B



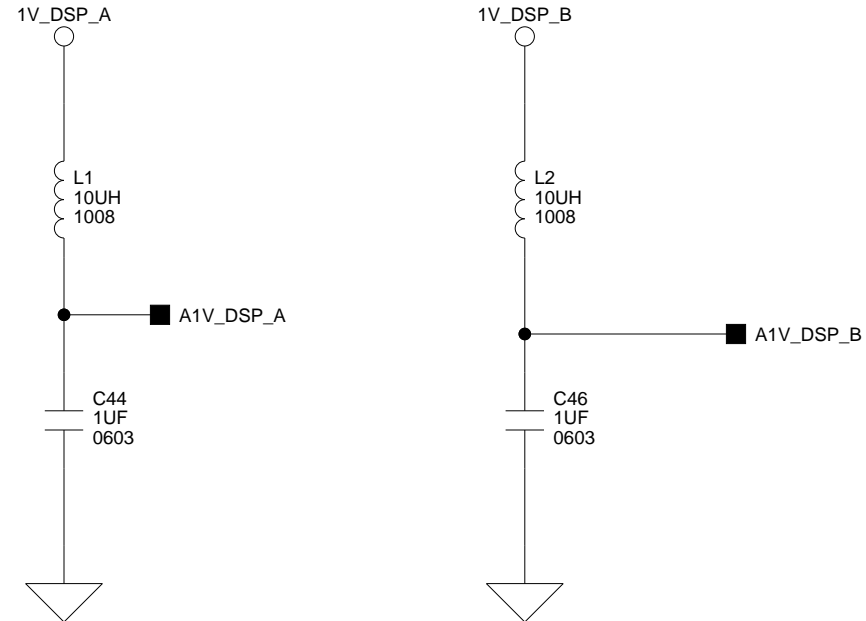
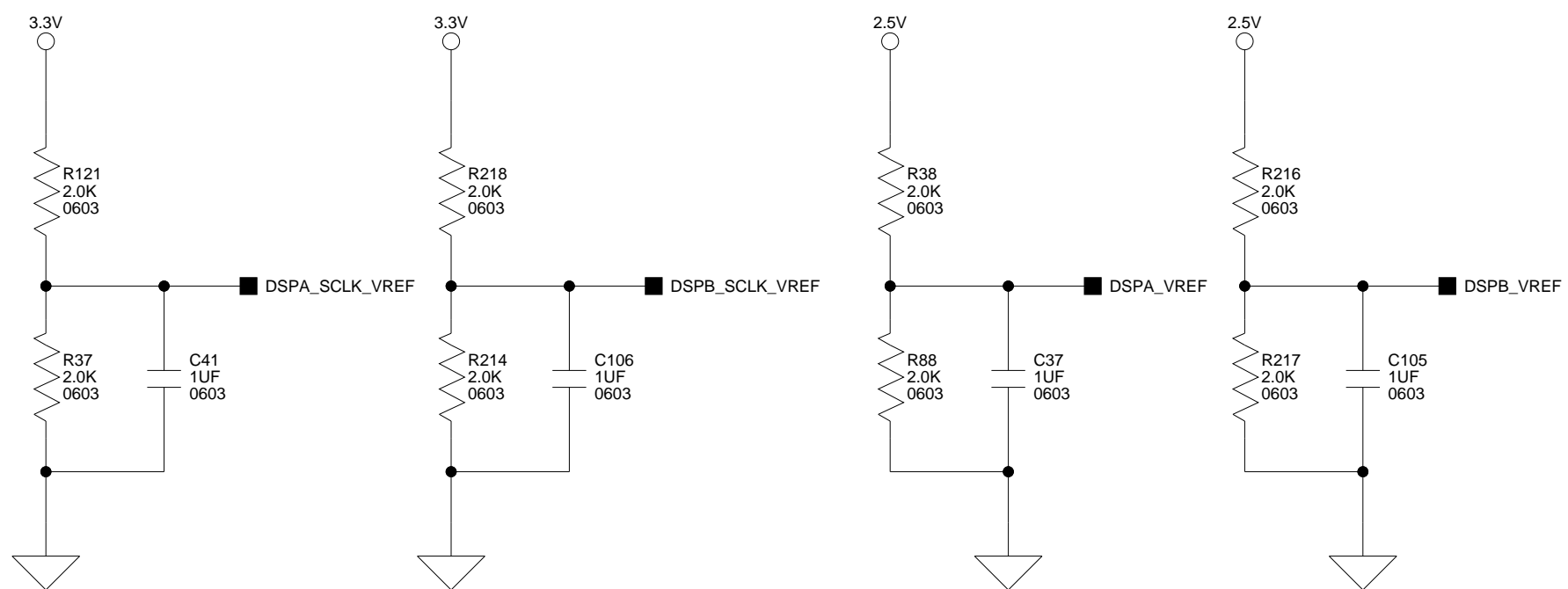
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- L1BCMPI_A
- L2BCMPI_A
- L3BCMPI_A

- LOBCMPI_B
- L1BCMPO_A
- L2BCMPO_A
- L3BCMPI_B

ANALOG DEVICES

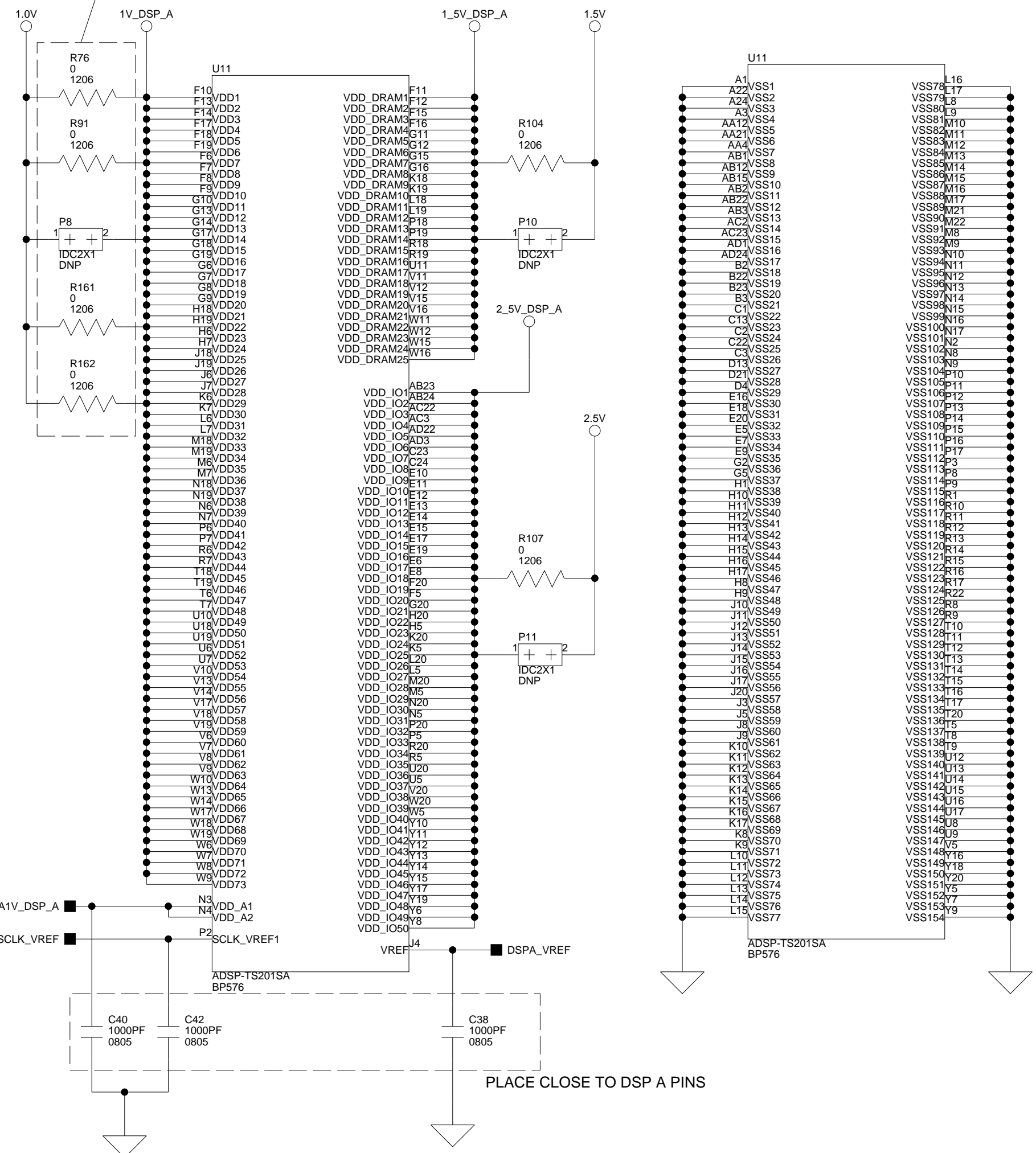
20 Cotton Road
 Nashua, NH 03063
 PH: 1-800-ANALOGD

Title		ADSP-TS201S EZ-KIT LITE DSP LINK PORTS	
Size C	Board No.	A0178-2002	Rev
Date		Sheet	
1-10-2007_10:57		4 of 15	



PLACE CLOSE TOGETHER
USE at least 3 vias per connection

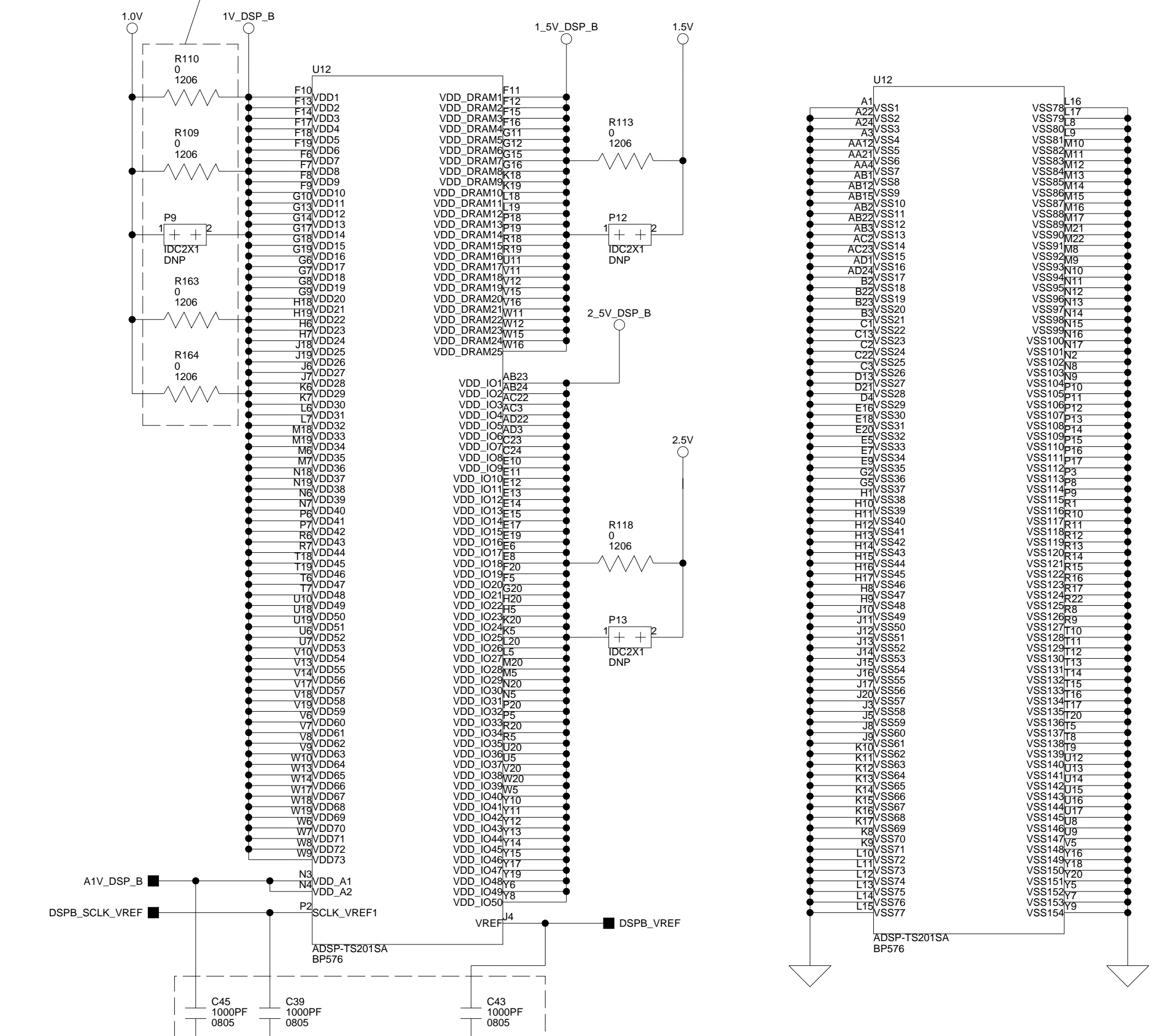
DSP A



PLACE CLOSE TO DSP A PINS

PLACE CLOSE TOGETHER
USE at least 3 vias per connection

DSP B

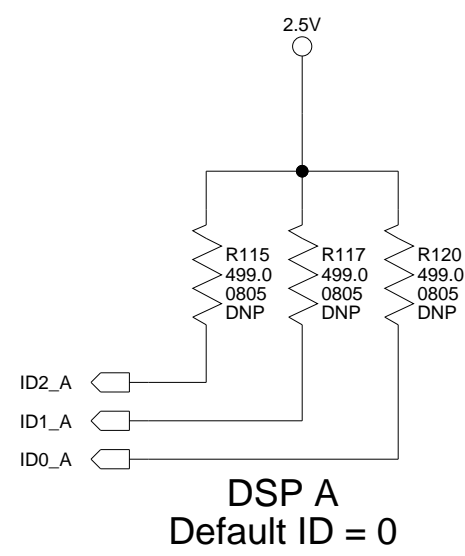


PLACE CLOSE TO DSP B PINS

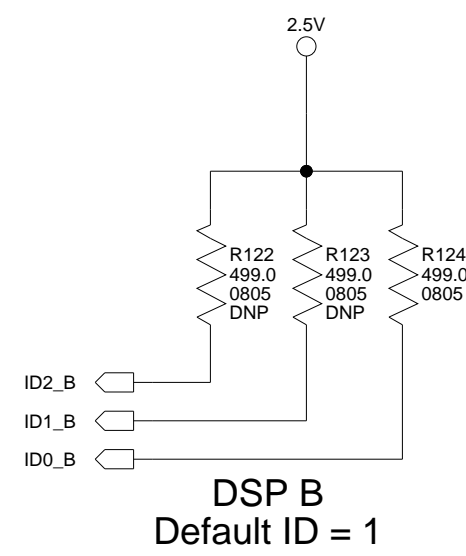
ANALOG DEVICES

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Title ADSP-TS201S EZ-KIT LITE DSP POWER			
Size C	Board No. A0178-2002	Rev 2.1C	
Date 1-10-2007_10:57	Sheet 5 of 15		



DSP A
Default ID = 0

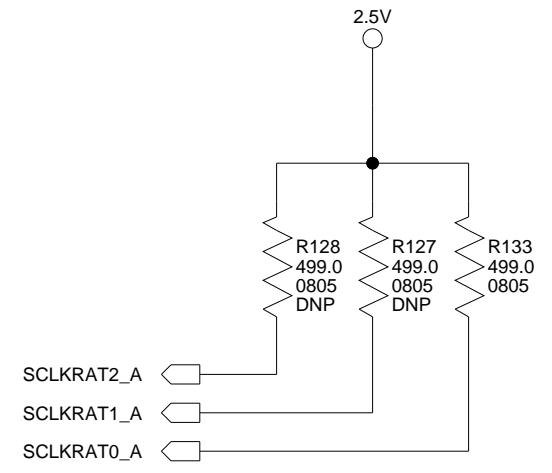


DSP B
Default ID = 1

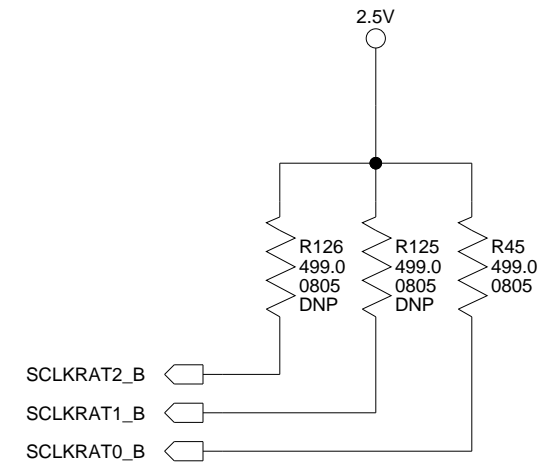
ID[2-0] have internal 5Kohm pull-down resistors

ID(2-0)	Proc ID
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

THESE RESISTORS DO NOT NEED TO BE VERY CLOSE TO THE DSP
IF POSSIBLE I WOULD LIKE THEM ALL ON THE BOTTOM OF THE BOARD
ORGANIZED IN GROUPS SIMILAR TO SHOW HERE
DEPENDING ON HOW MUCH ROOM YOU CAN LEAVE NEAR THEM
I WOULD LIKE TO LABEL SOME OF THEM



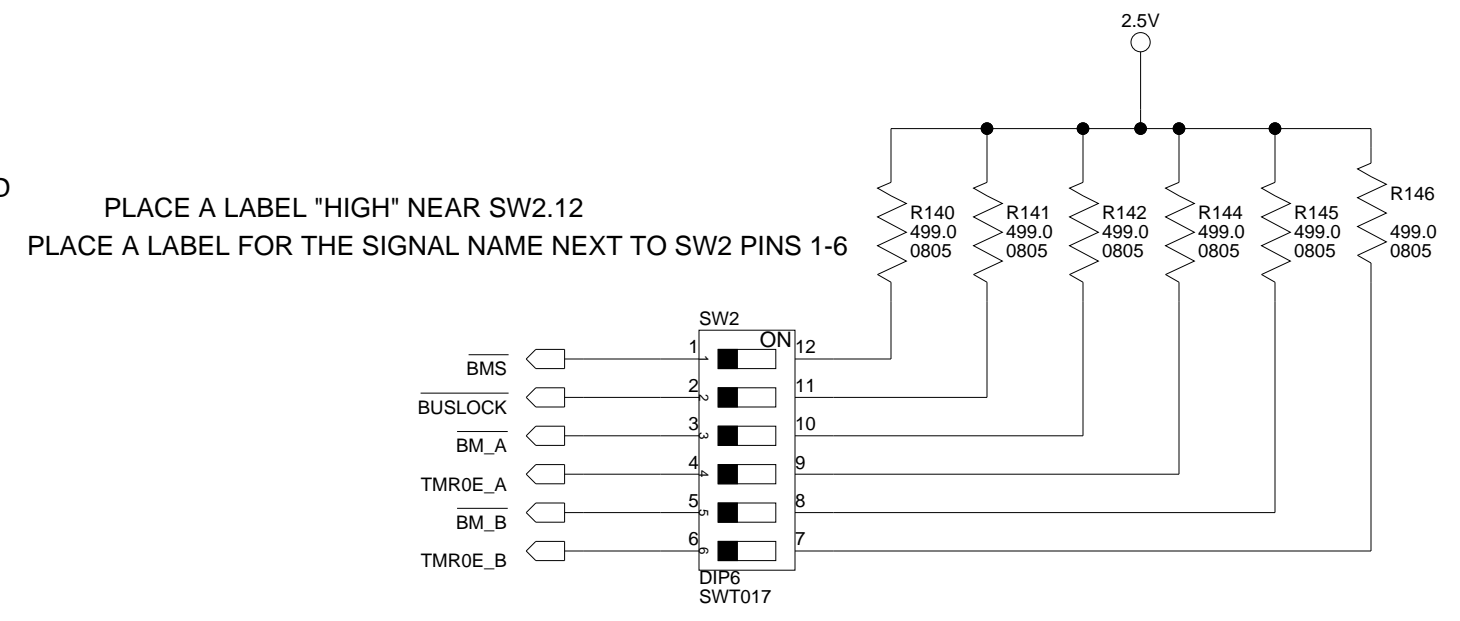
DSP A
Default PLL Ratio = 5X
CCLK = 500MHz



DSP B
Default PLL Ratio = 5X
CCLK = 500MHz

SCLKRAT[2-0] have internal 5Kohm pull-down resistors

SCLKRAT(2-0)	PLL Ratio
000	4
001	5
010	6
011	7
100	8
101	10
110	12
111	RESERVED

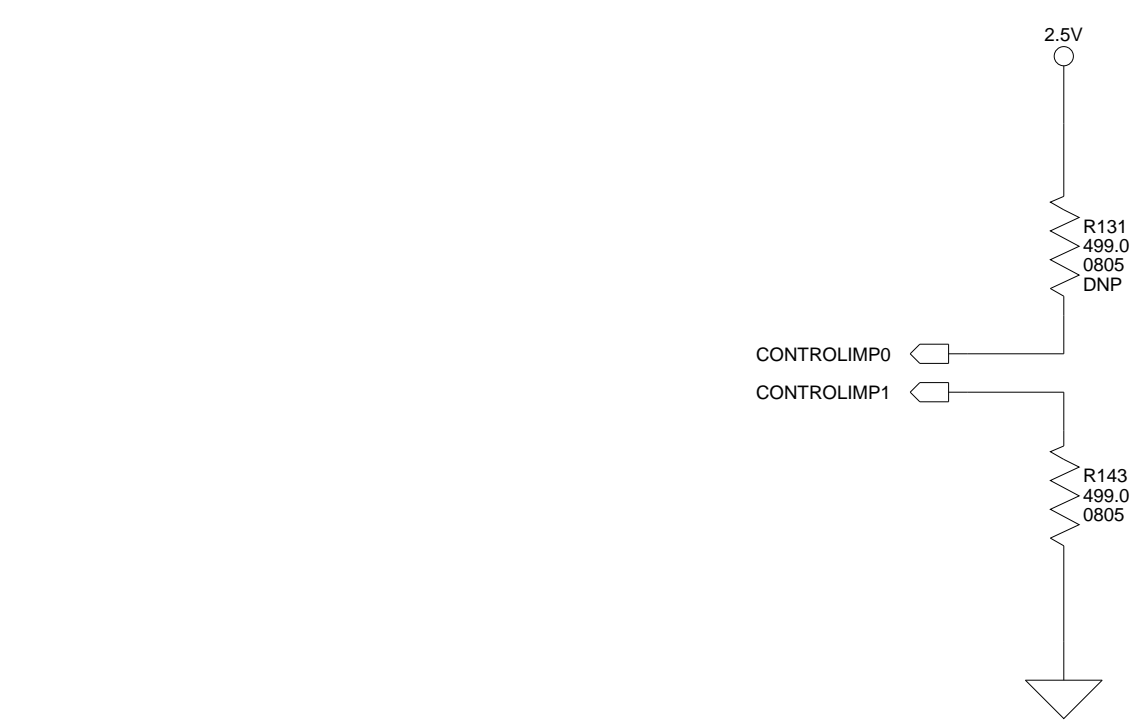


PLACE A LABEL "HIGH" NEAR SW2.12
PLACE A LABEL FOR THE SIGNAL NAME NEXT TO SW2 PINS 1-6

All strap pins have internal 5Kohm pull-down resistors during DSP reset

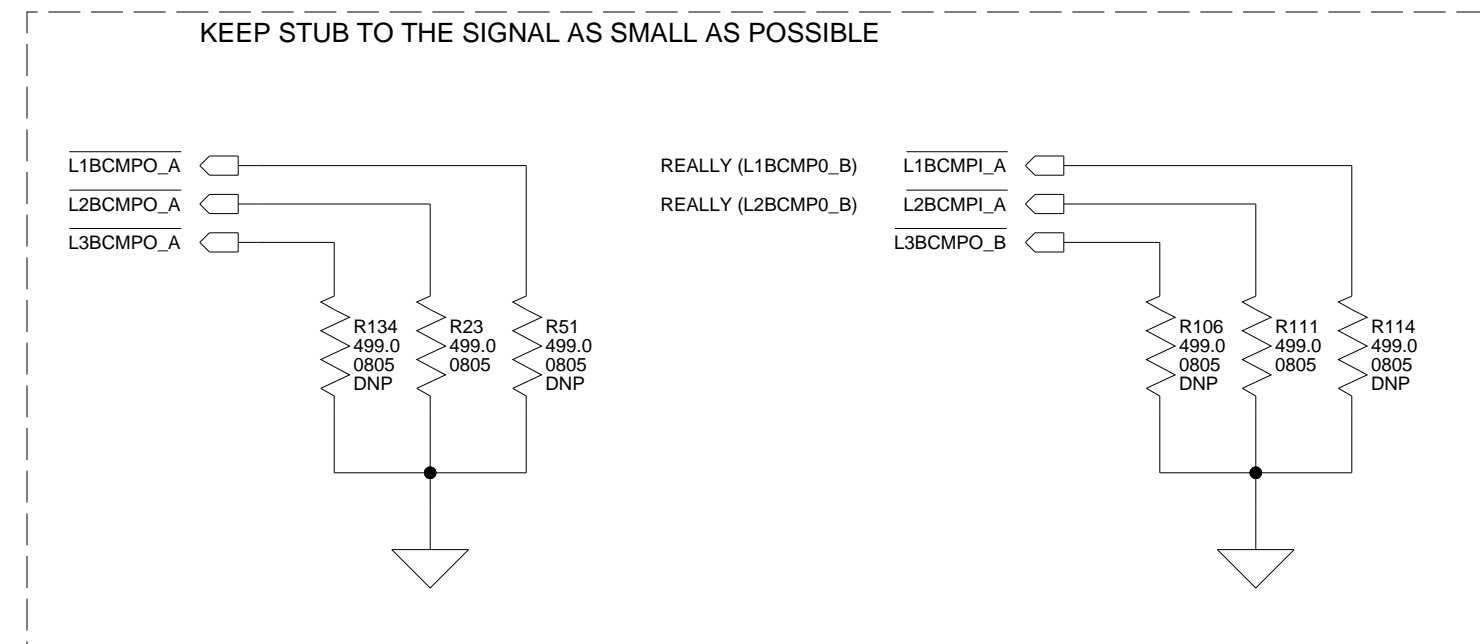
	Switch OFF (Signal Pulled Low)	Switch ON (Signal Pulled High)
BMS	* EPROM Boot	External or link port boot
BM	* Disable interrupts, level sensitive	Enable interrupts, edge sensitive
TMR0E	* 1-bit Link Port Data Width	4-bit Link Port Data Width
BUSLOCK	* SYSCON/SDRCON one-time writable	SYSCON/SDRCON always writable

* indicates DEFAULT

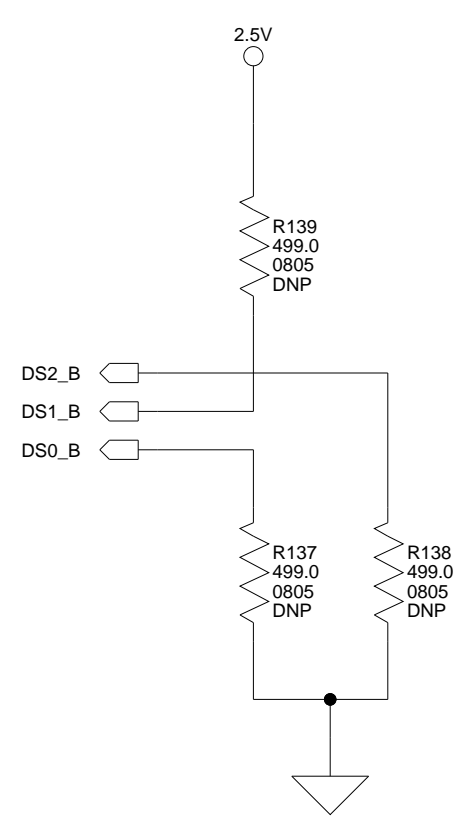
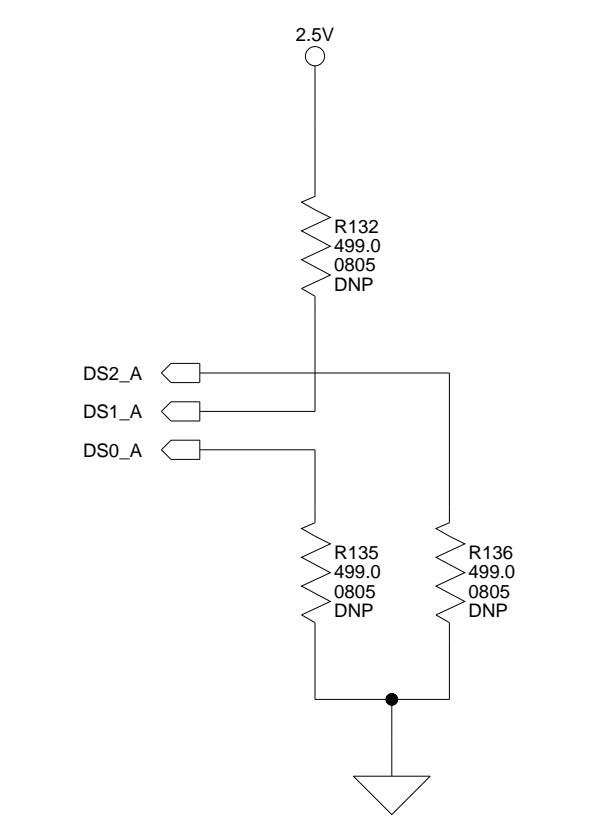


DEFAULT = NORMAL
CONTROLIMP0 has an internal 5Kohm pull-down resistor
CONTROLIMP1 has an internal 5Kohm pull-up resistor

CONTROLIMP(1:0)	Driver Mode
00	Normal
01	Pulse Mode
10	A/D Mode
11	Pulse Mode, A/D Mode



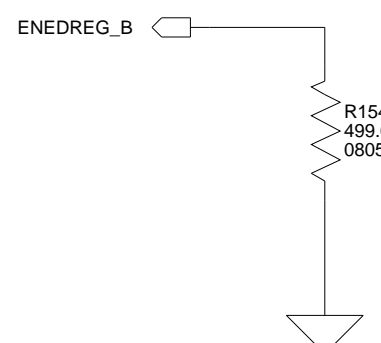
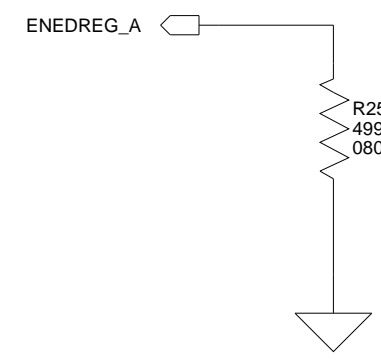
KEEP STUB TO THE SIGNAL AS SMALL AS POSSIBLE



DS1 has internal 5Kohm pull-down resistor
DS2 and DS0 have internal 5Kohm pull-up resistors

DS(2-0)	Drive Strength	OUTPUT IMP
000	11.1%	26
001	23.8%	32
010	36.5%	40
011	49.2%	50
100	61.9%	62
101	74.6%	70
110	87.3%	96
111	100%	120

DEFAULT



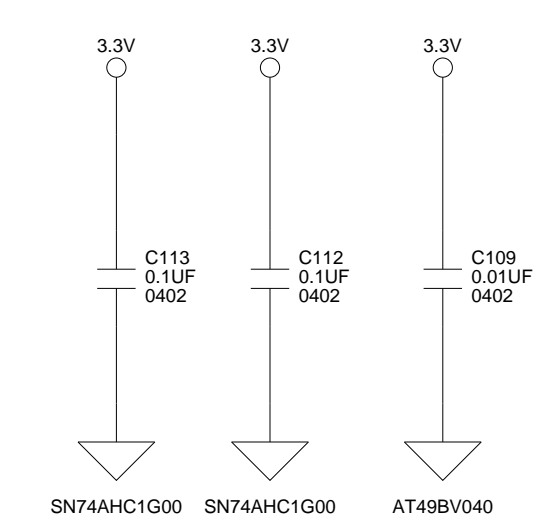
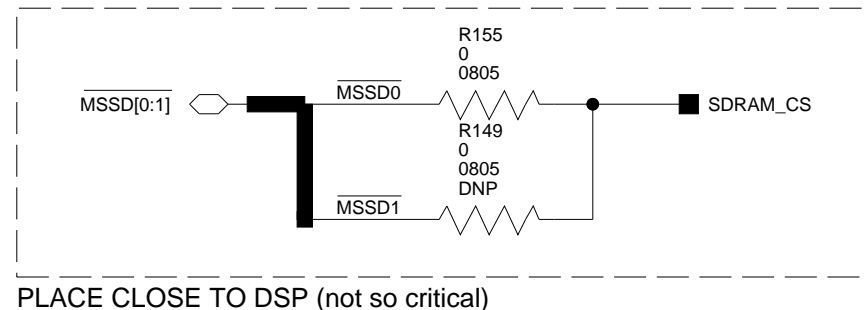
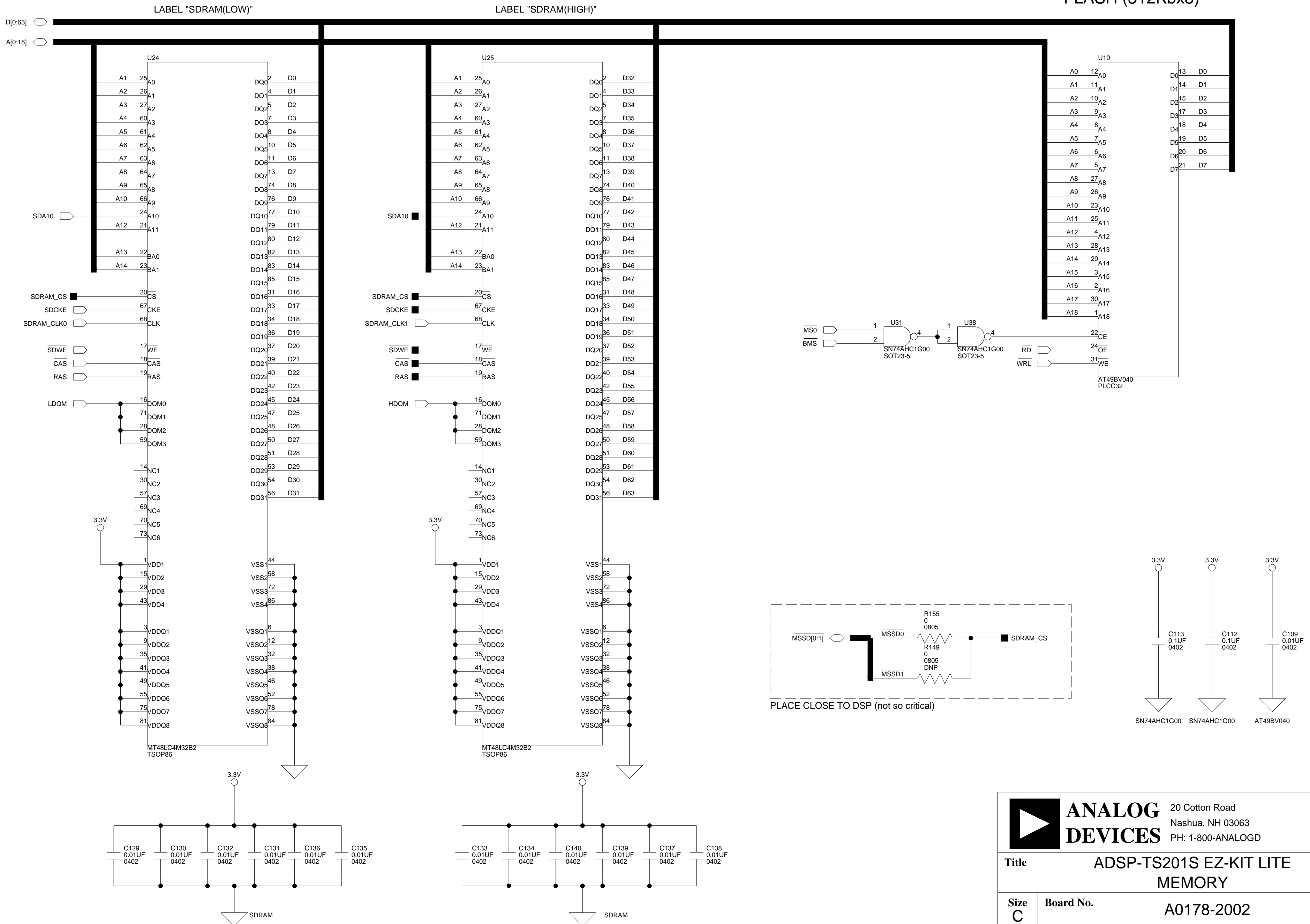
ANALOG DEVICES

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Title ADSP-TS201S EZ-KIT LITE CONFIGURATION		
Size C	Board No. A0178-2002	Rev 2.1C
Date 4-9-2007_14:58	Sheet 6 of	15

SDRAM 256Mb
(32MB - 4M x 64bits)

FLASH (512Kbx8)



		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-TS201S EZ-KIT LITE MEMORY	
Size C	Board No.	A0178-2002	
Date	1-10-2007_10:57	Sheet	7 of 15
		Rev	2.1C

KEEP ALL OF THESE COMPONENTS OVER THE AGND PLANE

PLACE NEAR CONNECTOR

TRY TO KEEP ALL TRACES AS SHORT AS POSSIBLE

LABEL "LINE IN"

VREF_AUDIO

ADC LEFT

ADC

SLAVE MODE
MCLK IS 256 x Fs
48 KHZ SAMPLE RATE
I S I/F MODE

PLACE NEAR CONNECTOR

ADC RIGHT

KEEP THESE CLOSE TO AD1871

THE GND AND AGND PLANES SHOULD GO FROM PIN 8 TO PIN 21 of U9

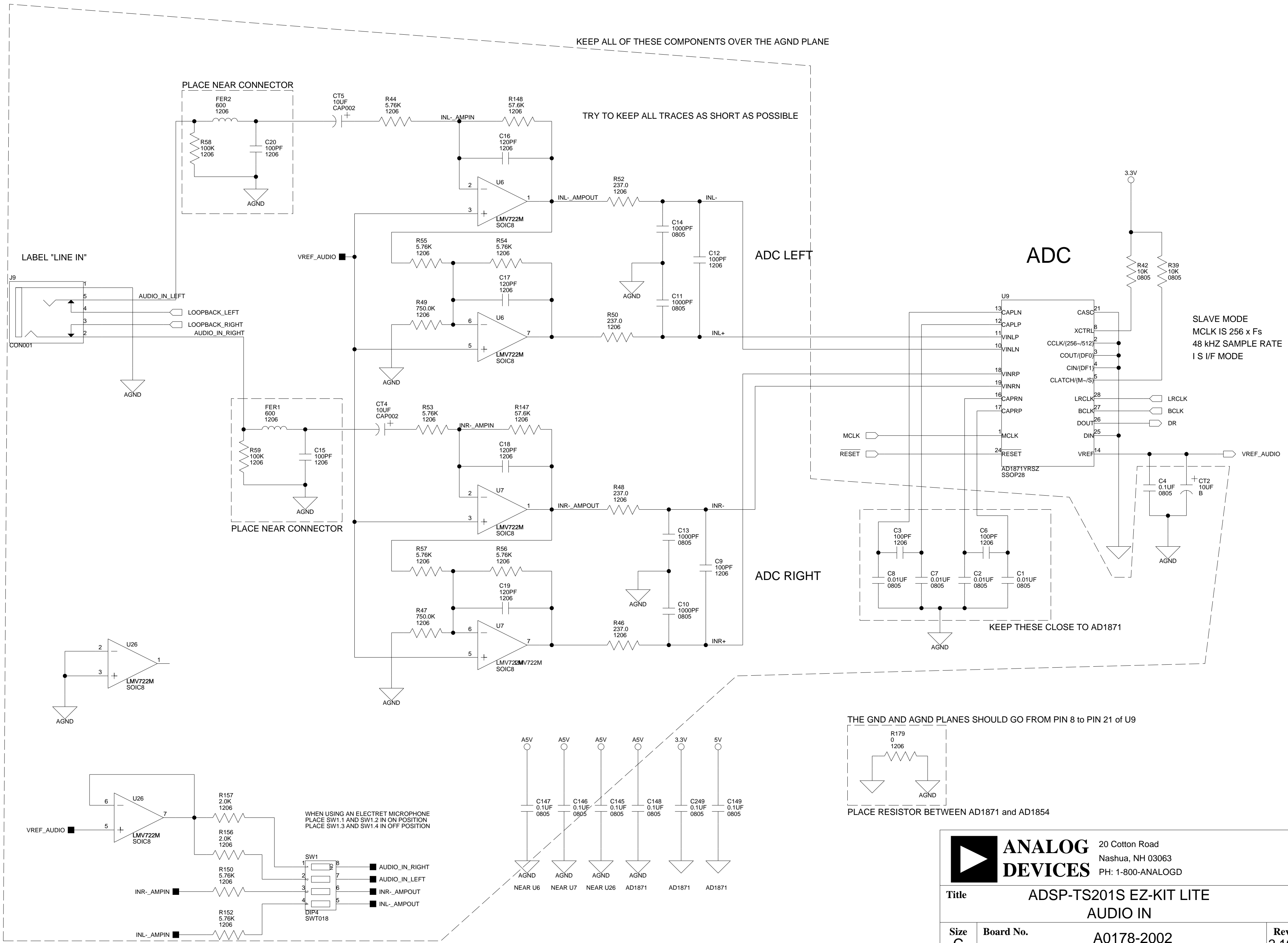
PLACE RESISTOR BETWEEN AD1871 and AD1854

WHEN USING AN ELECTRET MICROPHONE
PLACE SW1.1 AND SW1.2 IN ON POSITION
PLACE SW1.3 AND SW1.4 IN OFF POSITION

ANALOG DEVICES 20 Cotton Road
Nashua, NH 03063
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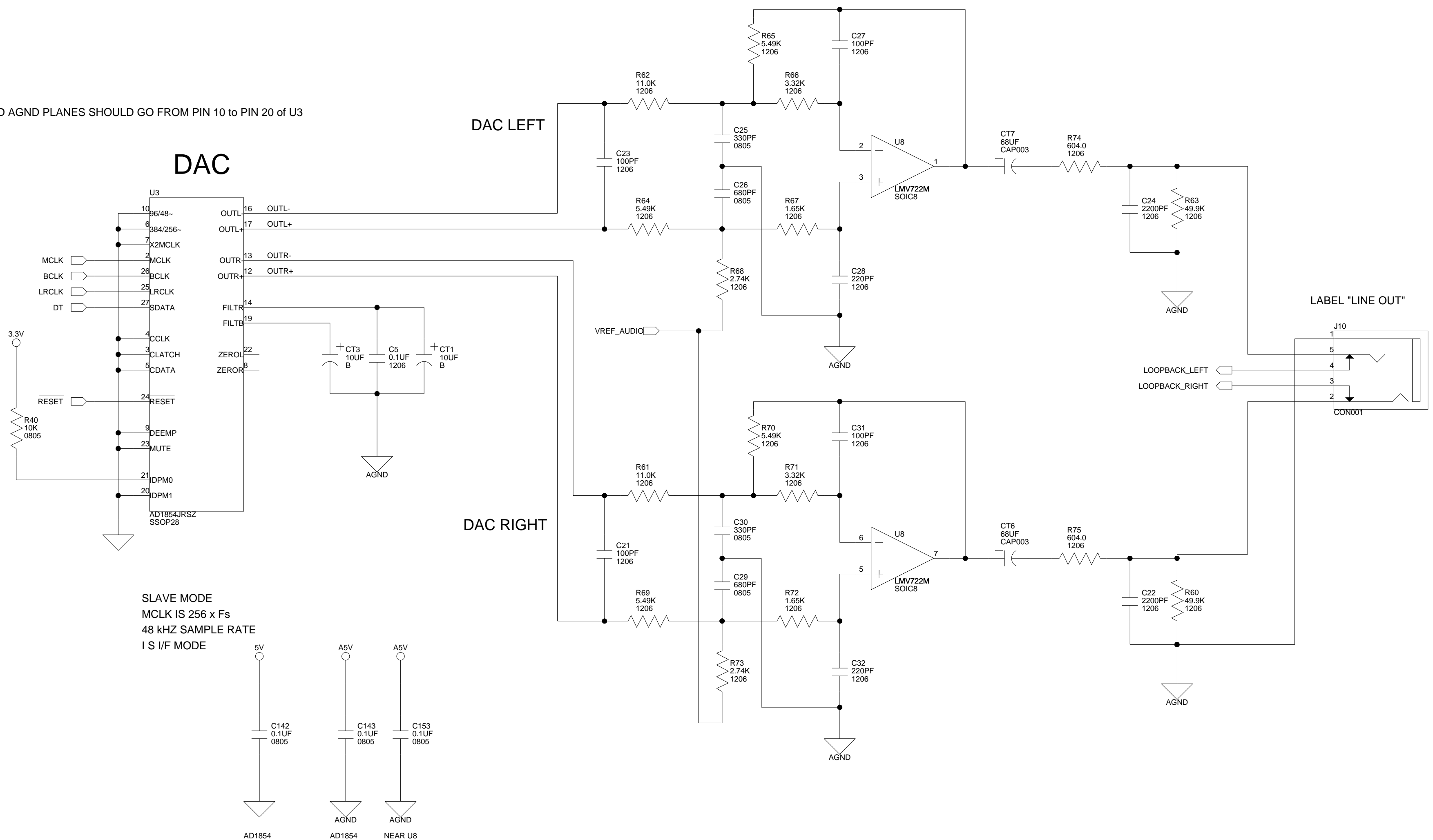
Title ADSP-TS201S EZ-KIT LITE
AUDIO IN

Size C	Board No. A0178-2002	Rev 2.1C
Date 1-10-2007_10:57	Sheet 8 of 15	

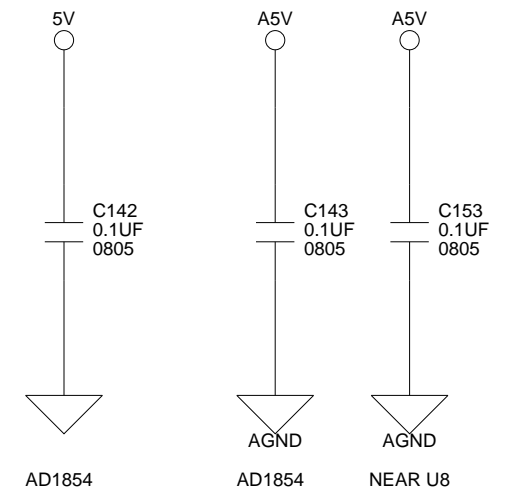


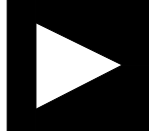
THE GND AND AGND PLANES SHOULD GO FROM PIN 10 to PIN 20 of U3

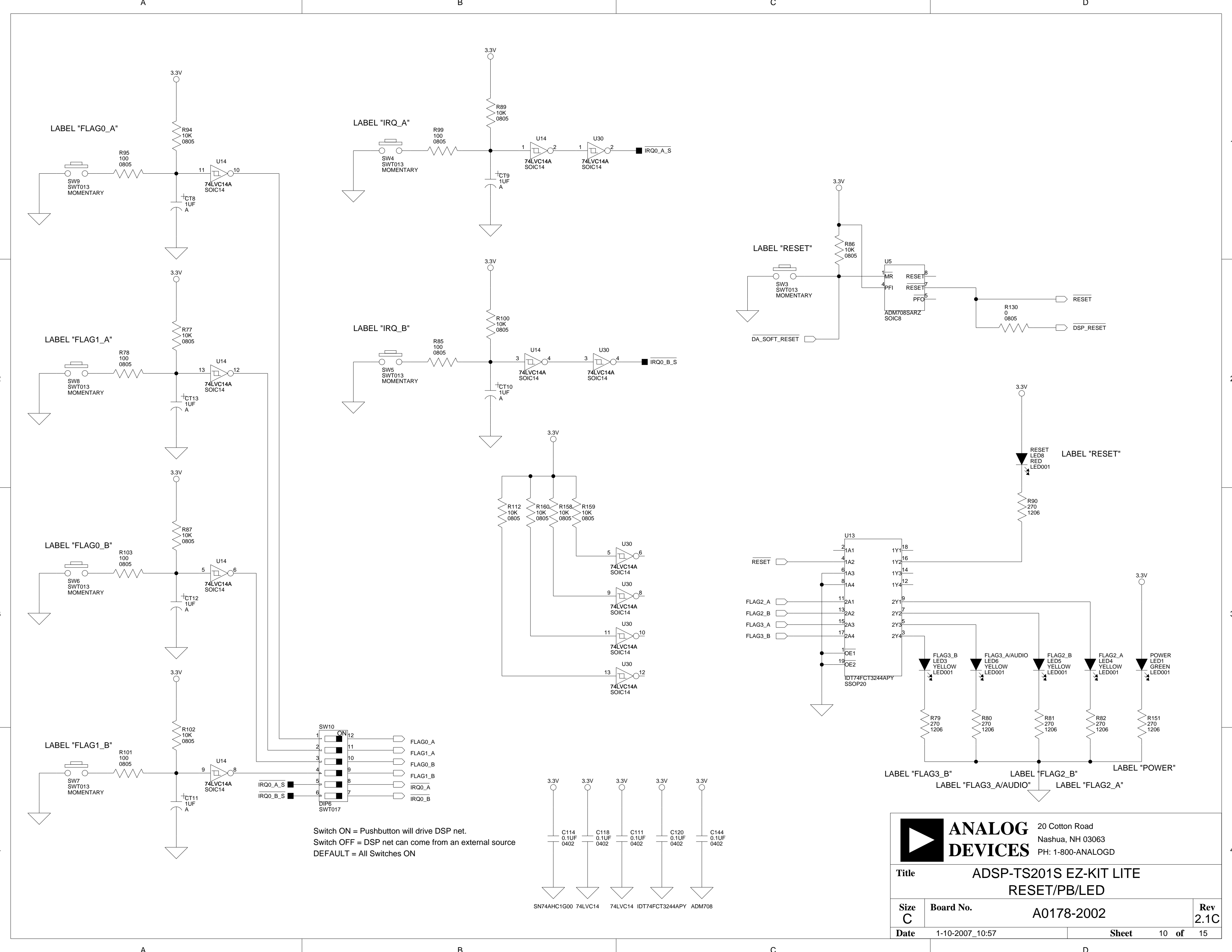
KEEP ALL OF THESE COMPONENTS OVER THE AGND PLANE



SLAVE MODE
MCLK IS 256 x Fs
48 KHZ SAMPLE RATE
I S I/F MODE



 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-TS201S EZ-KIT LITE AUDIO OUT	
Size C	Board No. A0178-2002	Rev 2.1C	
Date 1-10-2007_10:57	Sheet 9 of		15

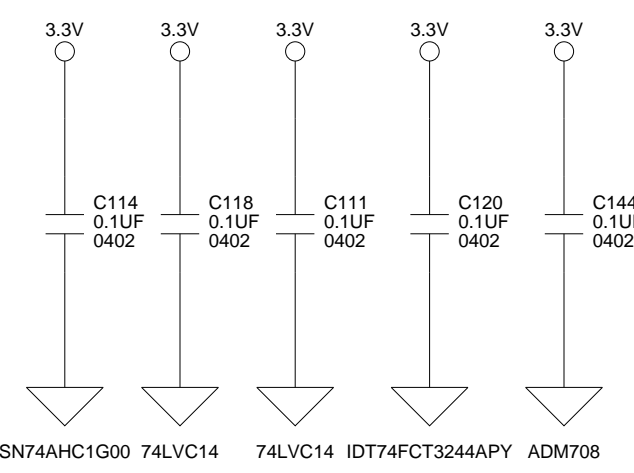


SW10 ON

1	12	FLAG0_A
2	11	FLAG1_A
3	10	FLAG0_B
4	9	FLAG1_B
5	8	IRQ0_A
6	7	IRQ0_B

DIP6 SWT017

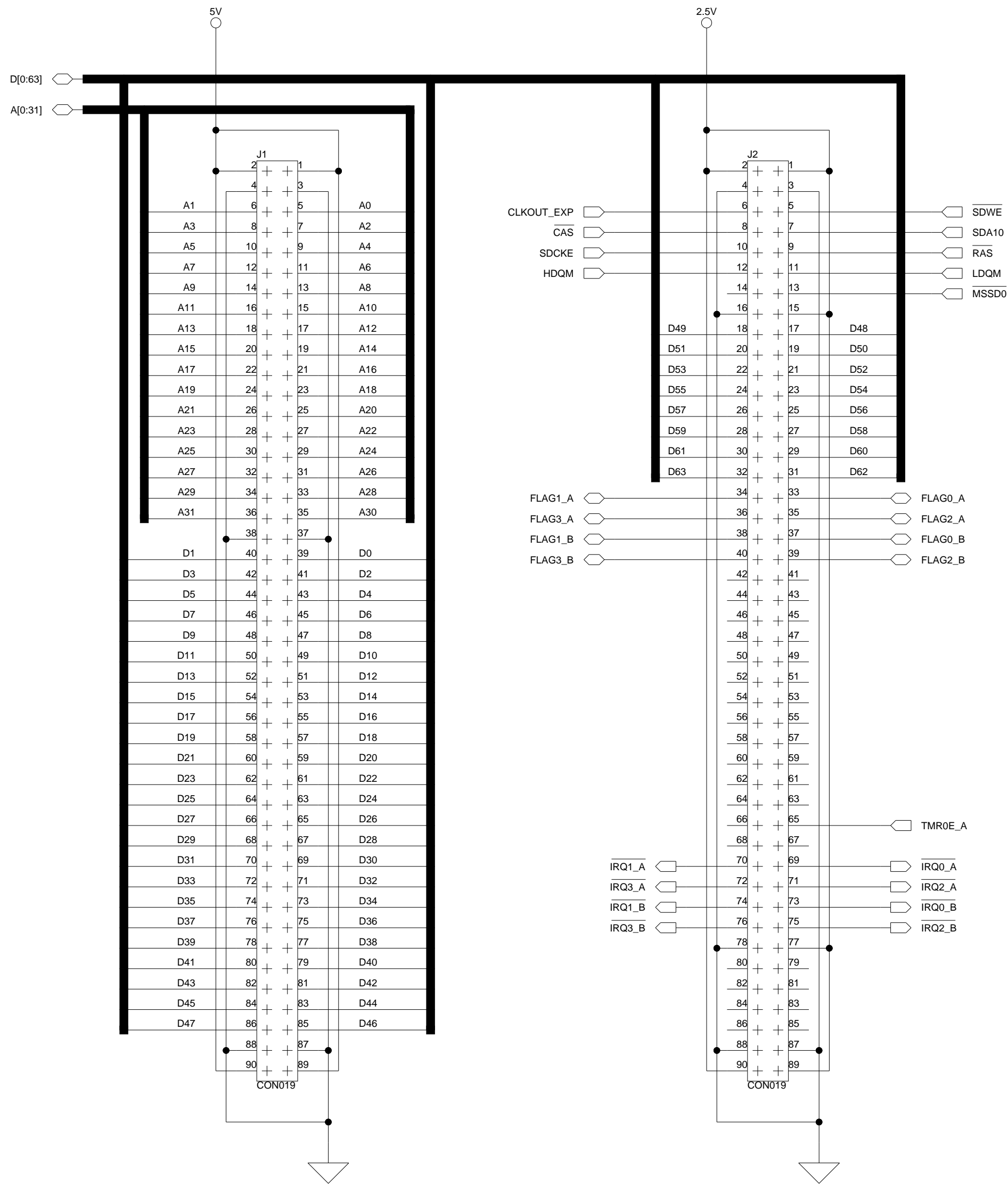
Switch ON = Pushbutton will drive DSP net.
 Switch OFF = DSP net can come from an external source
 DEFAULT = All Switches ON



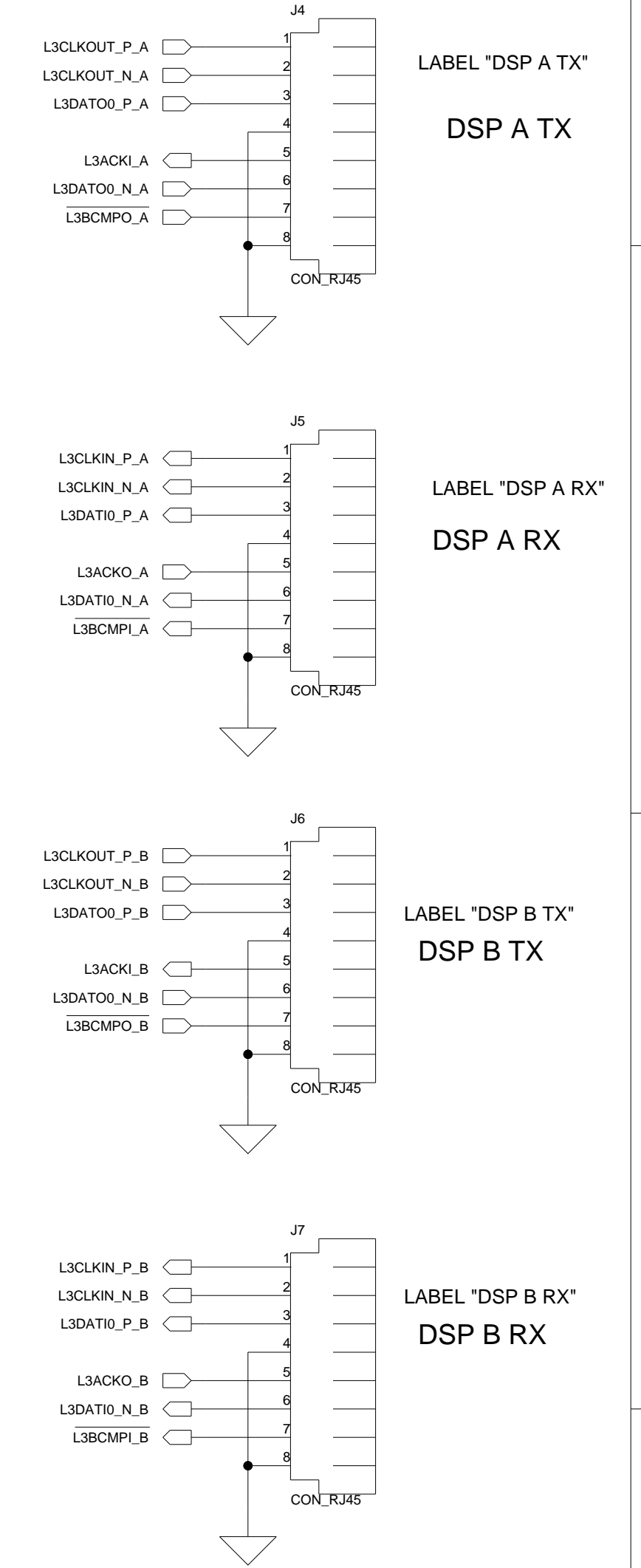
		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-TS201S EZ-KIT LITE RESET/PB/LED	
Size C	Board No. A0178-2002	Rev 2.1C	
Date 1-10-2007_10:57	Sheet 10 of 15		

Expansion Interface (TYPE A)

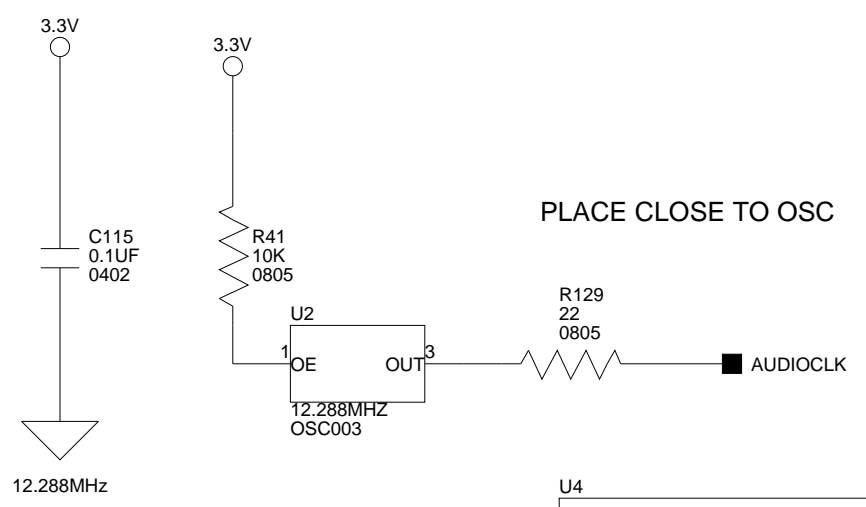
PLACE LABEL "EXPANSION INTERFACE (TYPE A)" NEAR MIDDLE CONNECTOR



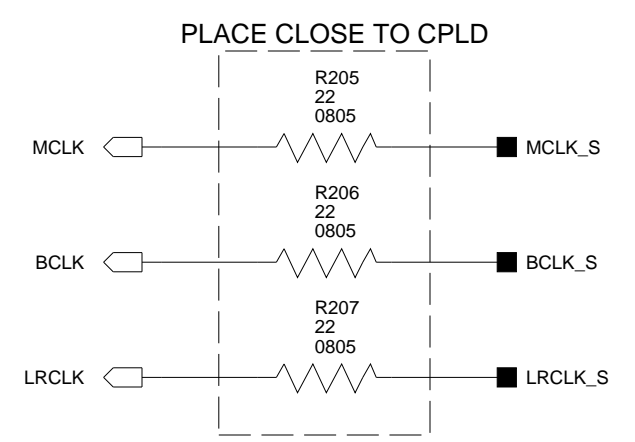
**WARNING: WHEN CONNECTING TO ANOTHER BOARD
MAKE SURE TX CONNECTOR GOES TO A RX CONNECTOR
DO NOT USE CROSSOVER CABLE**



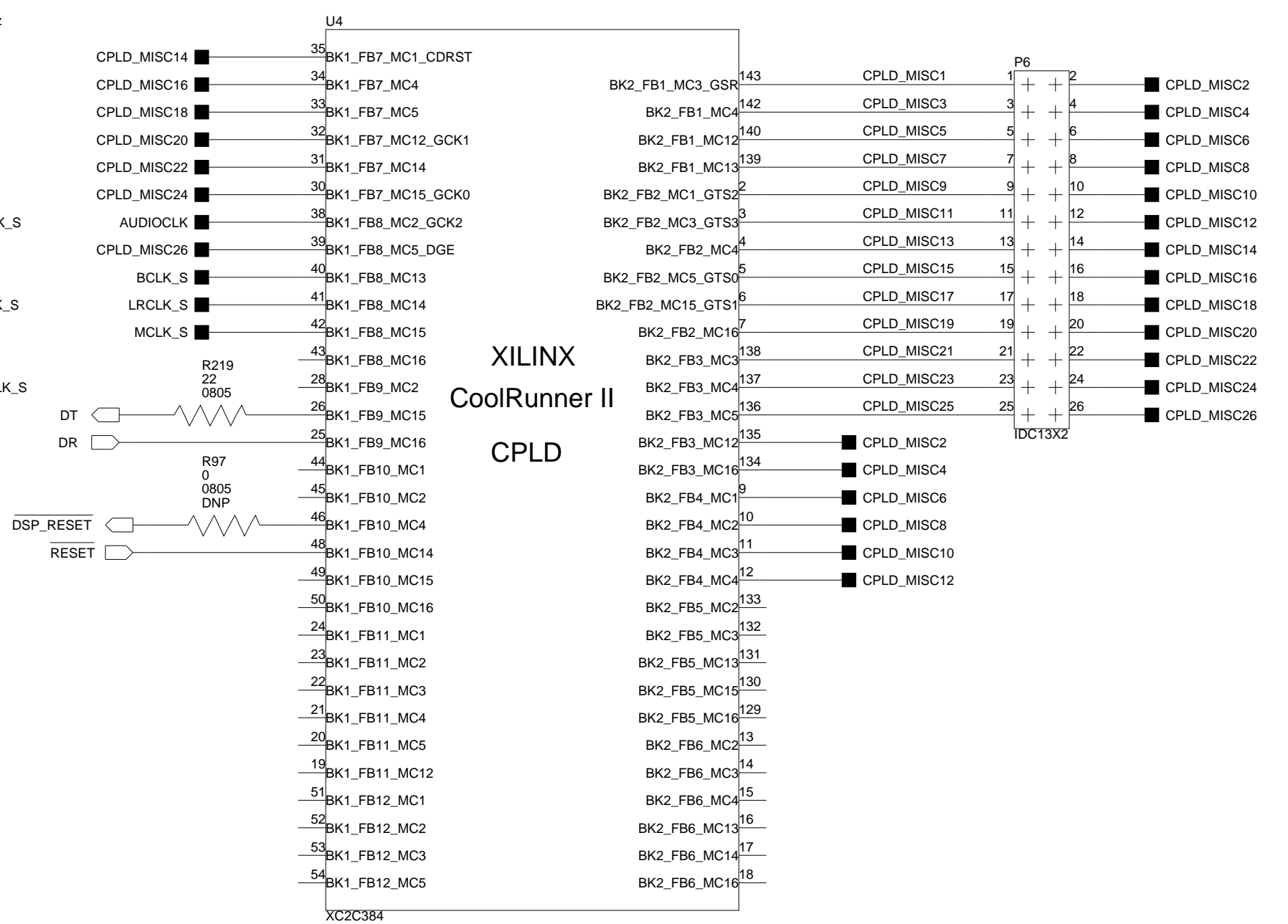
 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-TS201S EZ-KIT LITE EXPANSION INTERFACE	
Size C	Board No. A0178-2002	Rev 2.1C	
Date 1-10-2007_10:57	Sheet 11 of 15		



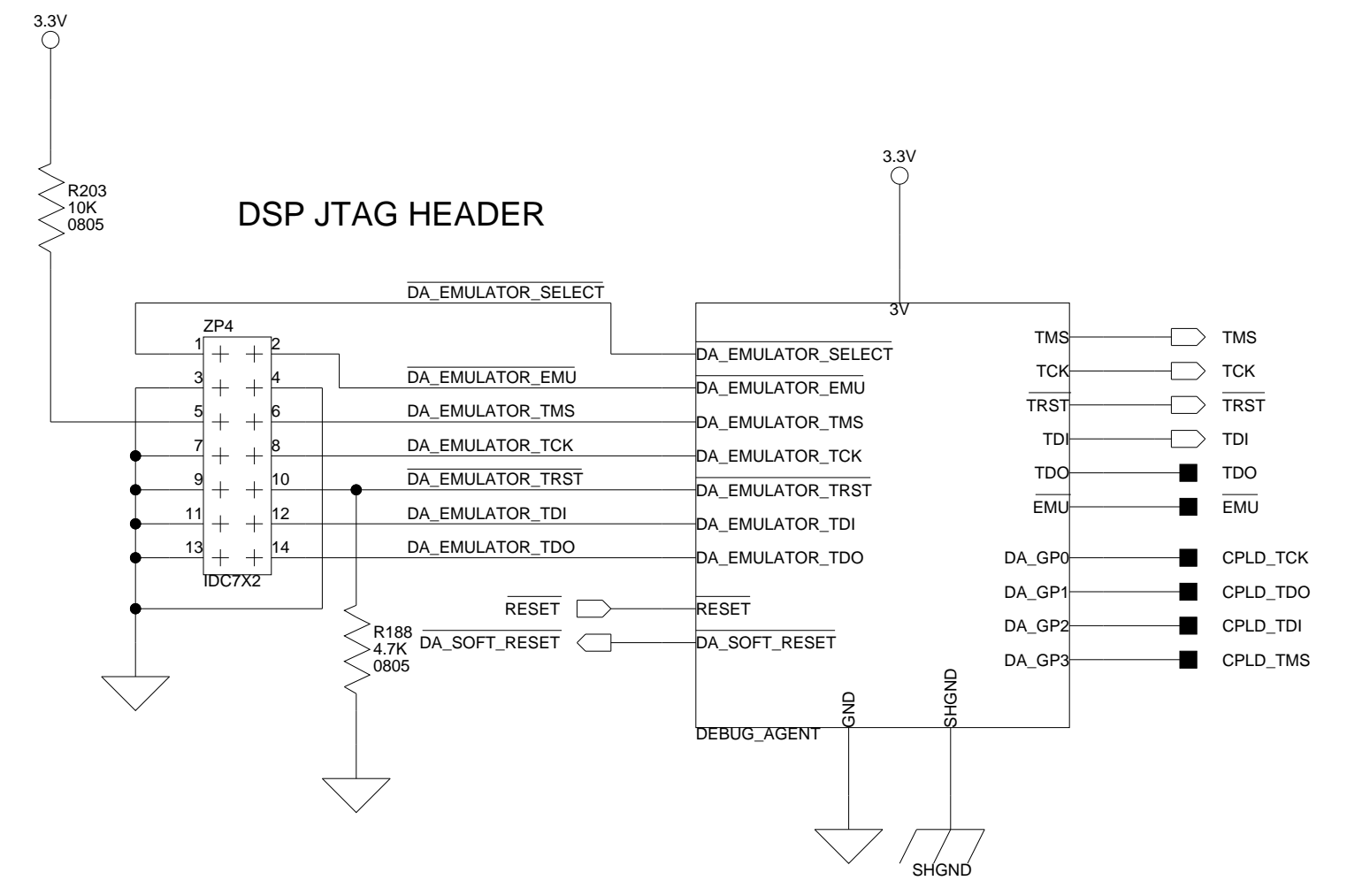
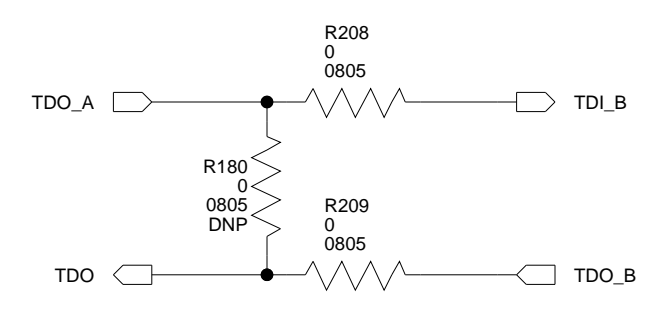
PLACE CLOSE TO OSC



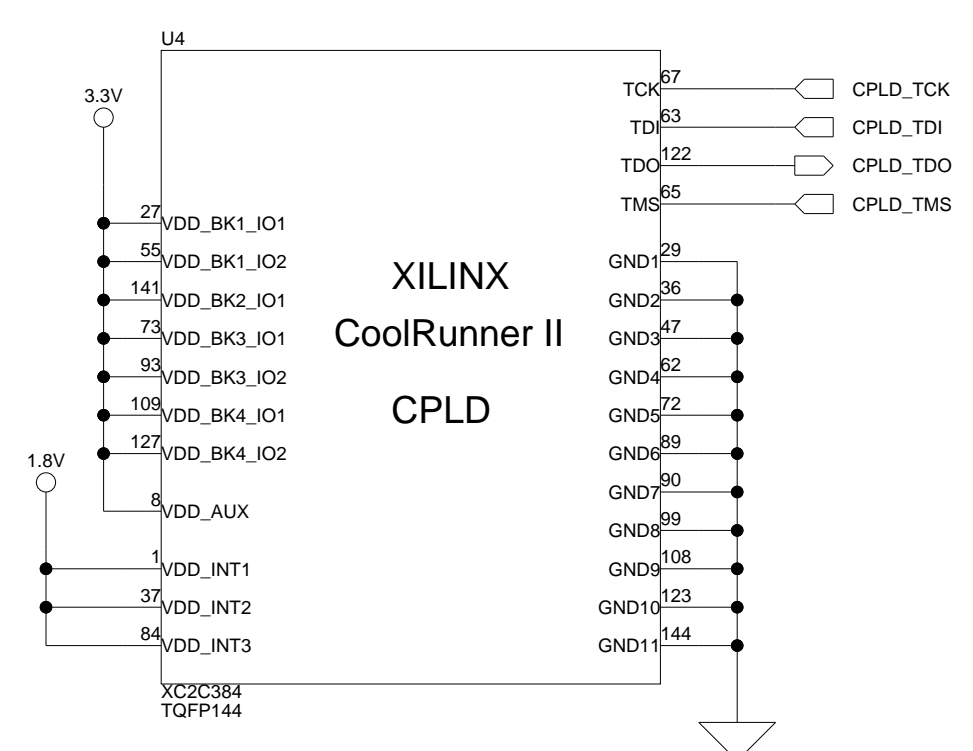
PLACE CLOSE TO CPLD



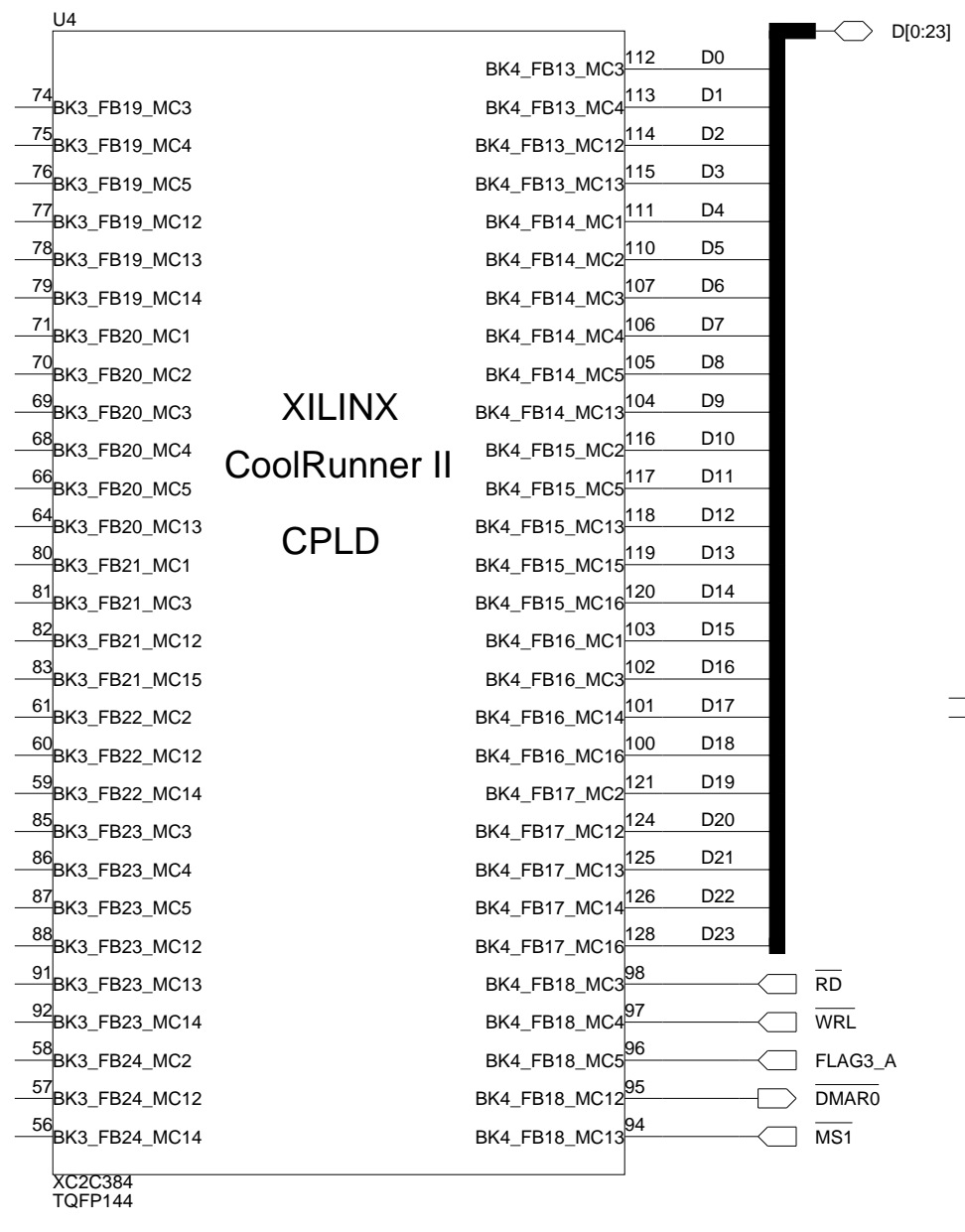
XILINX CoolRunner II CPLD



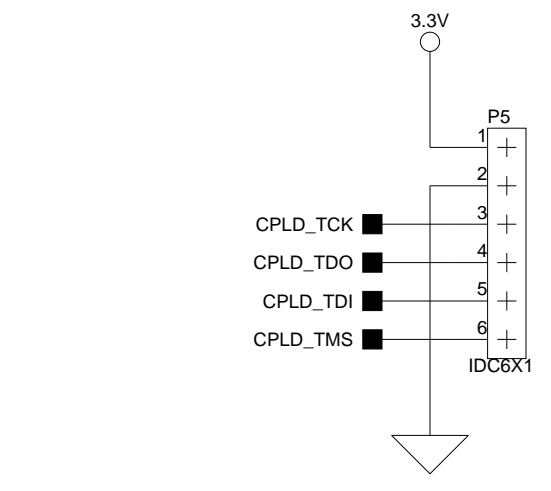
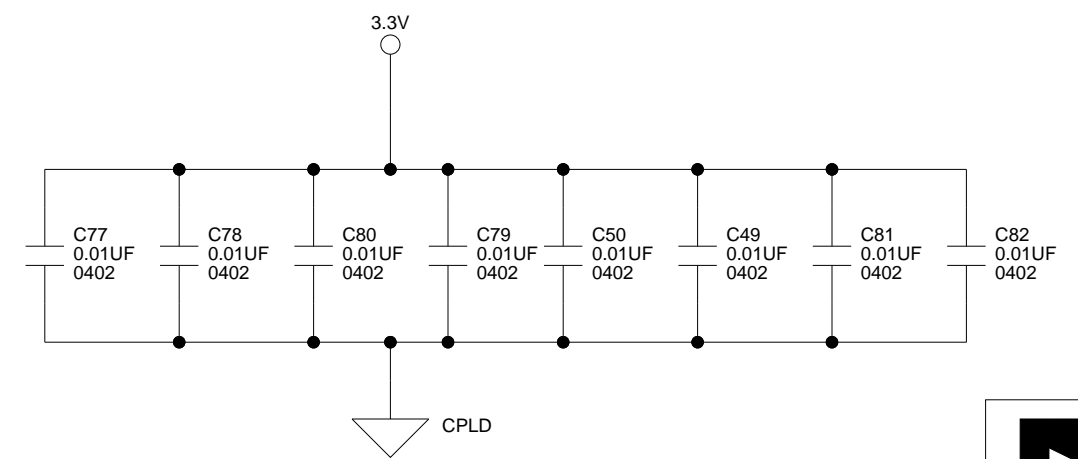
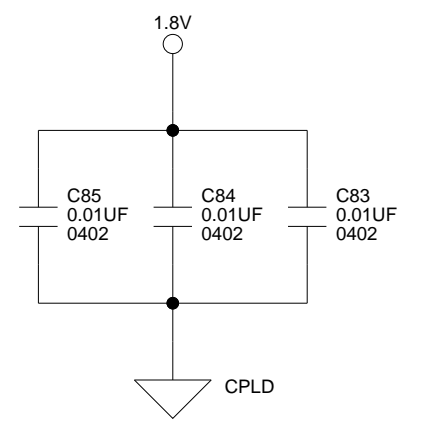
DSP JTAG HEADER



XILINX CoolRunner II CPLD



XILINX CoolRunner II CPLD

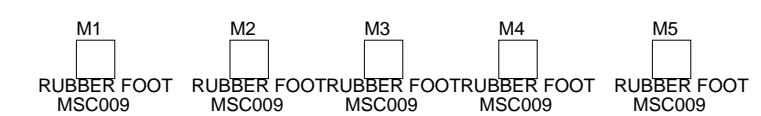
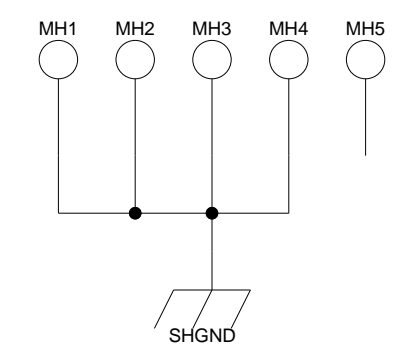
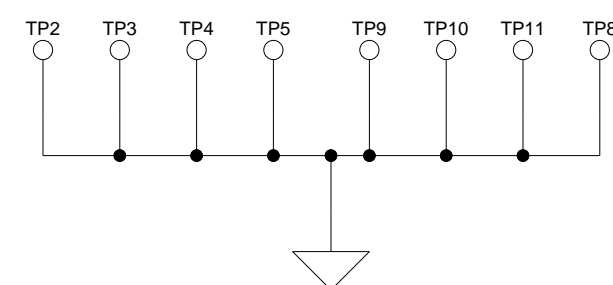
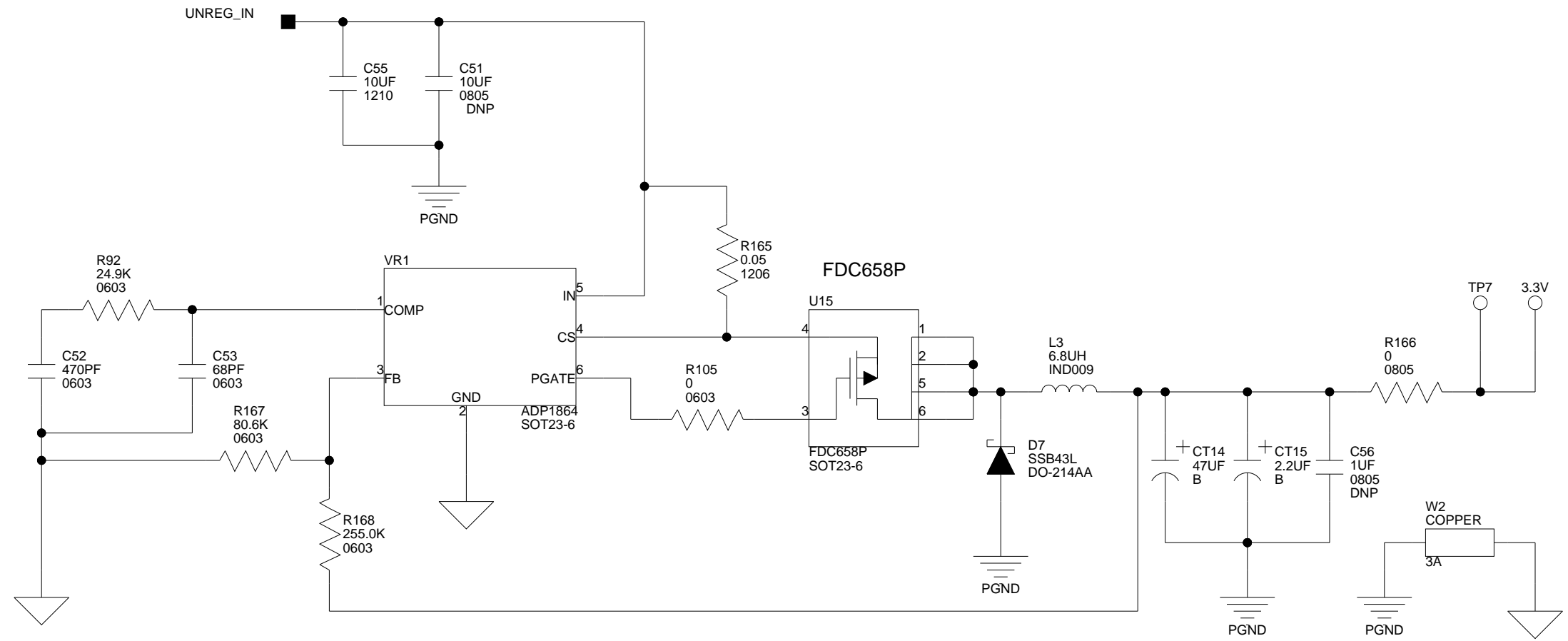
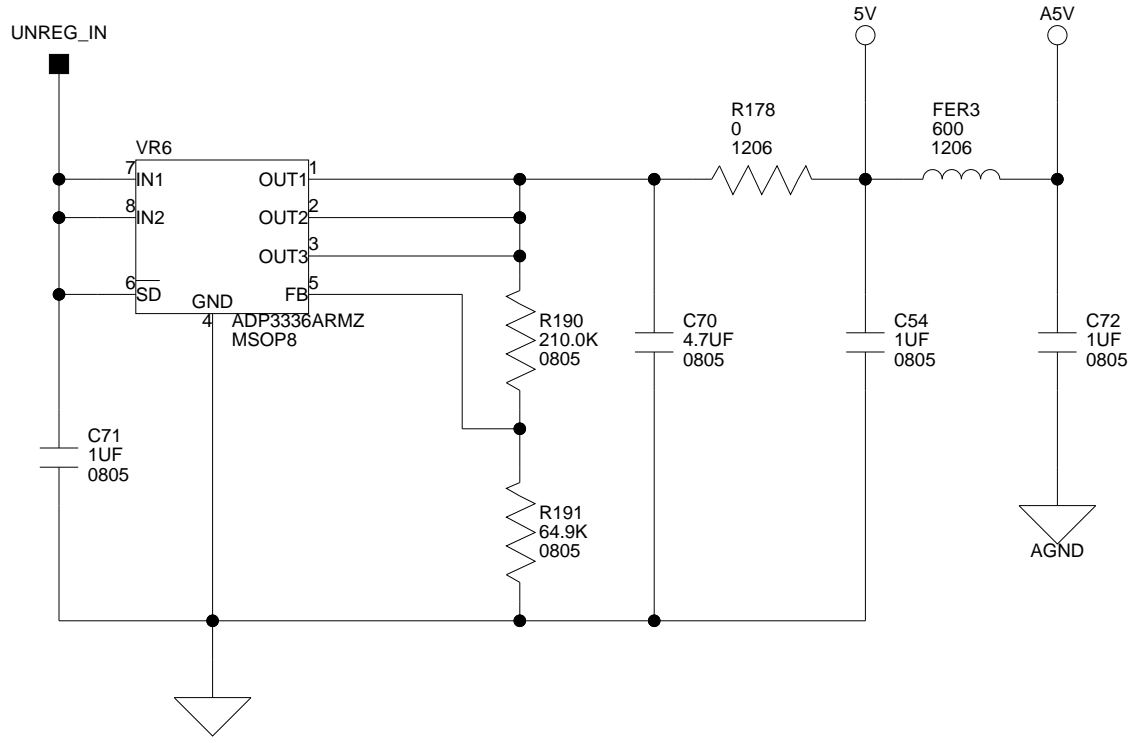
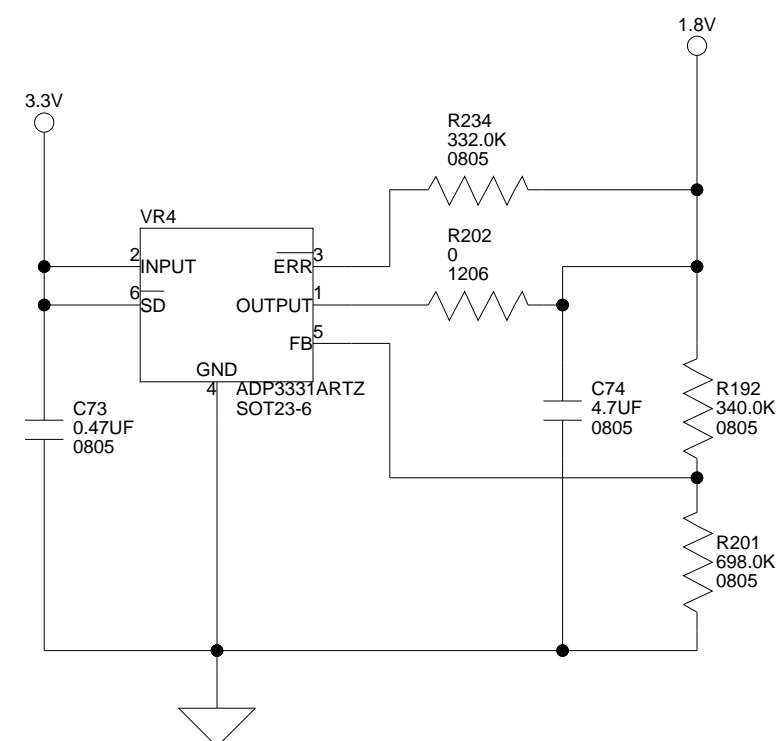
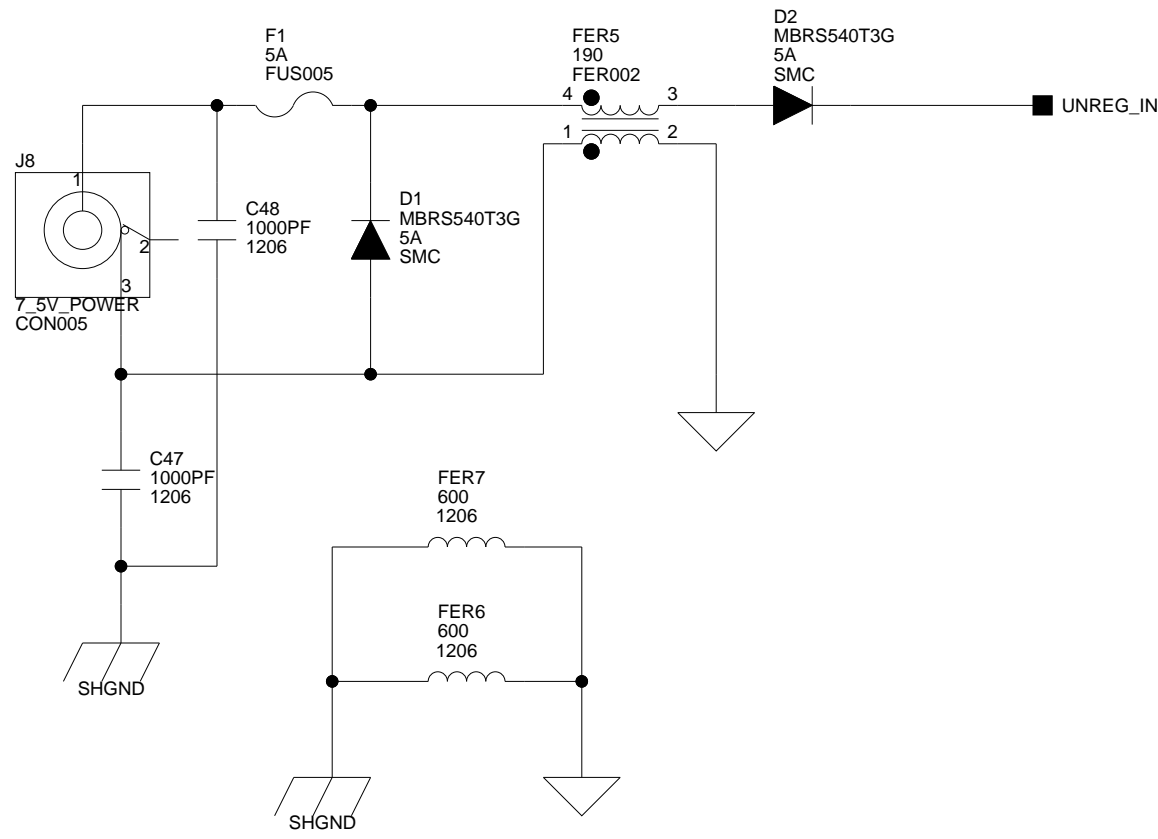


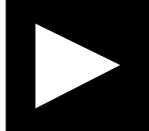
All USB interface is considered proprietary and has been omitted from this schematic.

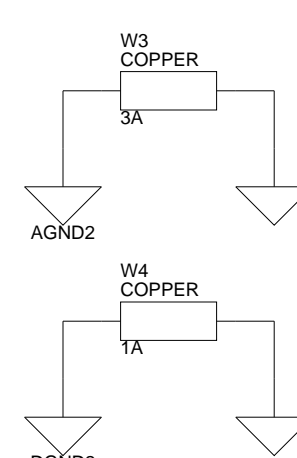
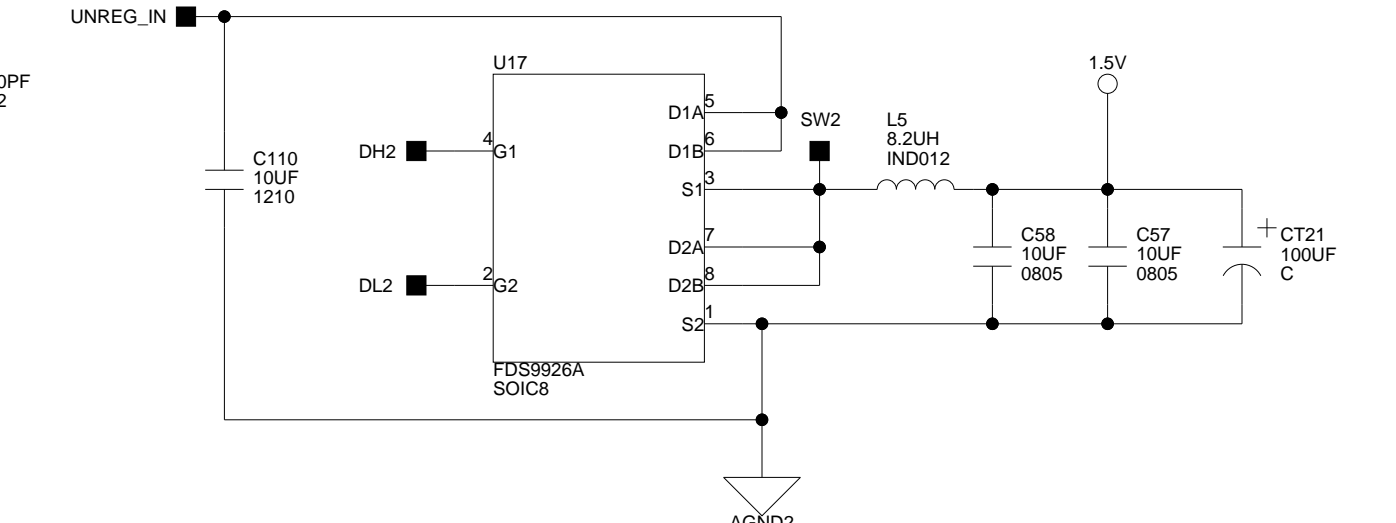
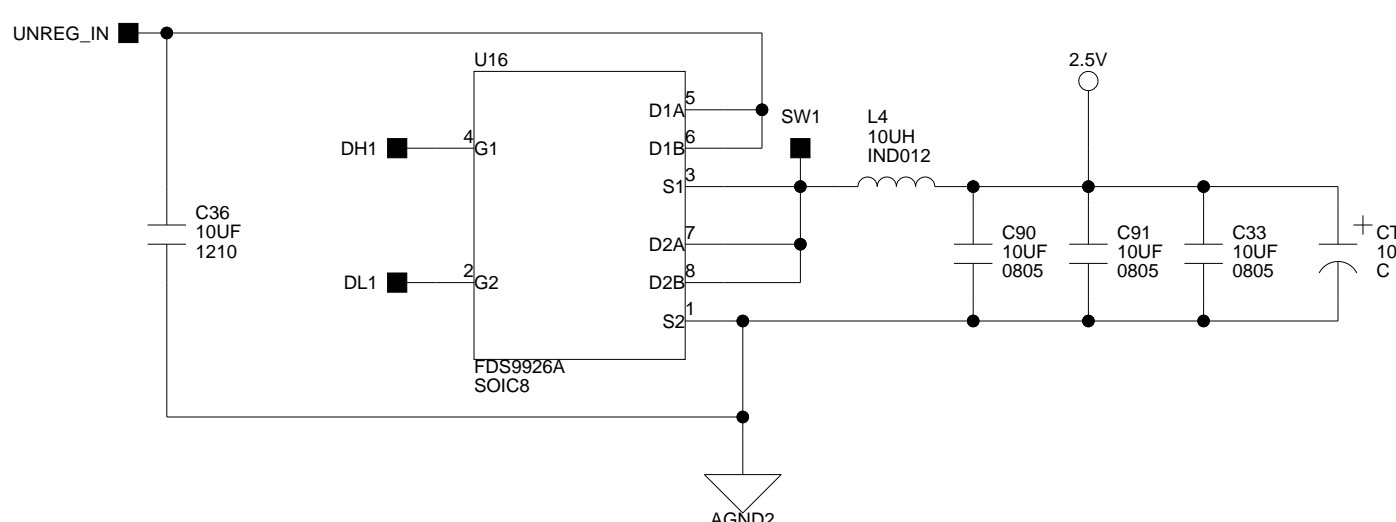
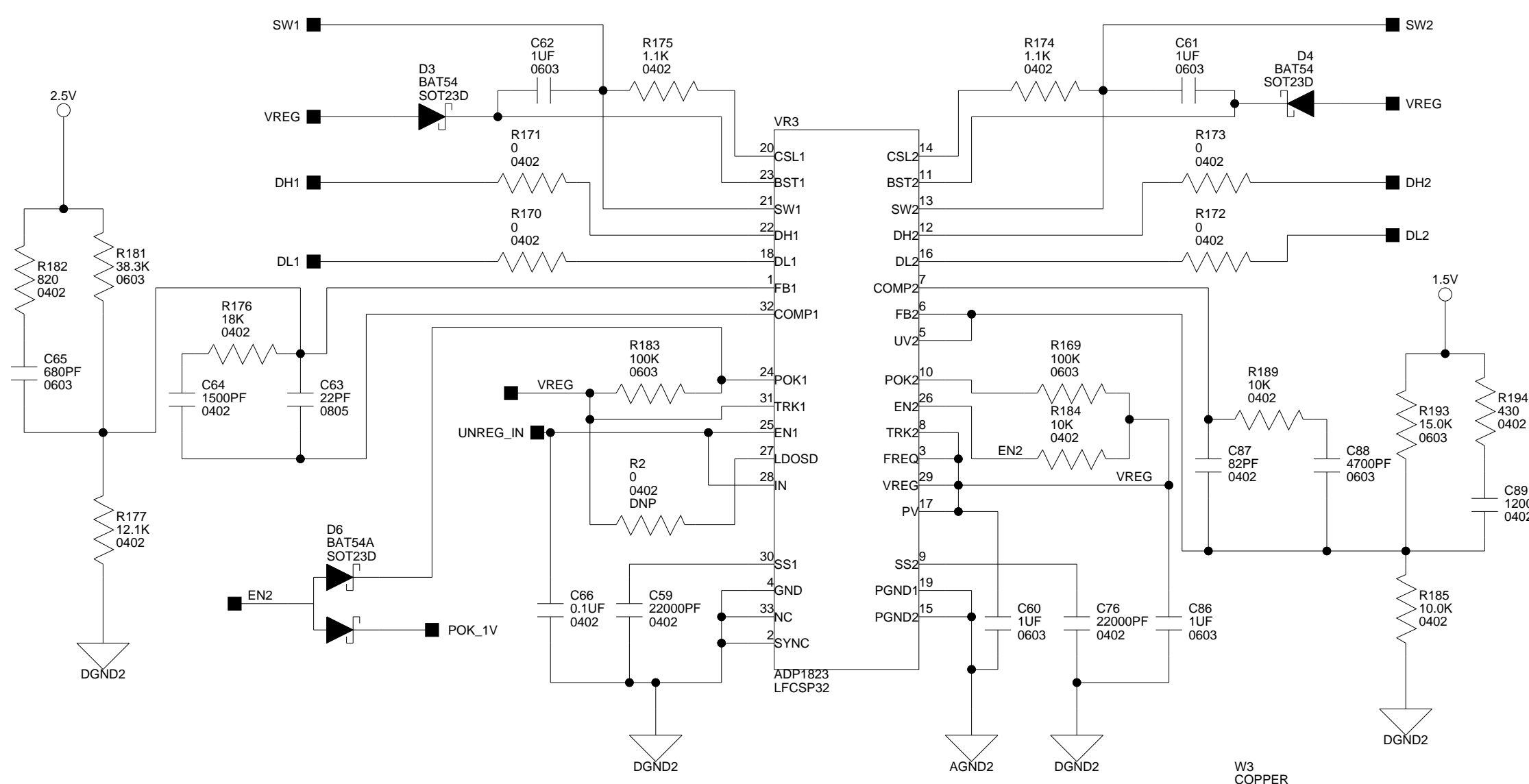
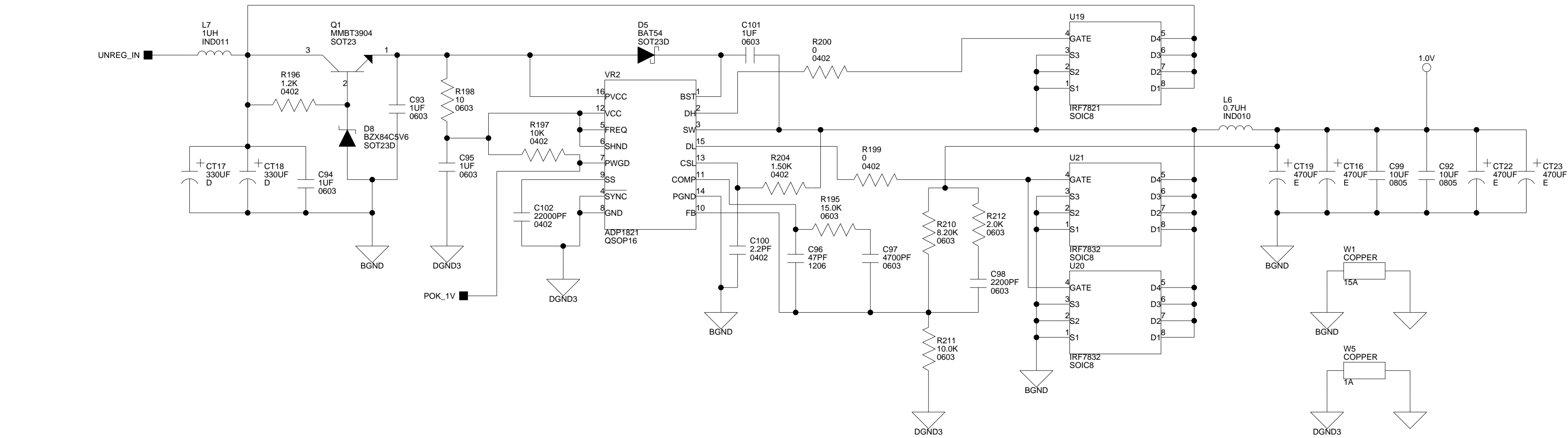
When designing your JTAG interface please refer to the Engineer to Engineer Note EE-68 which can be found at <http://www.analog.com>

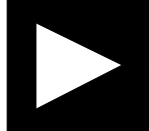
20 Cotton Road
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Title		ADSP-TS201S EZ-KIT LITE JTAG/CPLD FOR AUDIO	
Size C	Board No.	A0178-2002	Rev 2.1C
Date	1-10-2007_10:57	Sheet 12 of	15

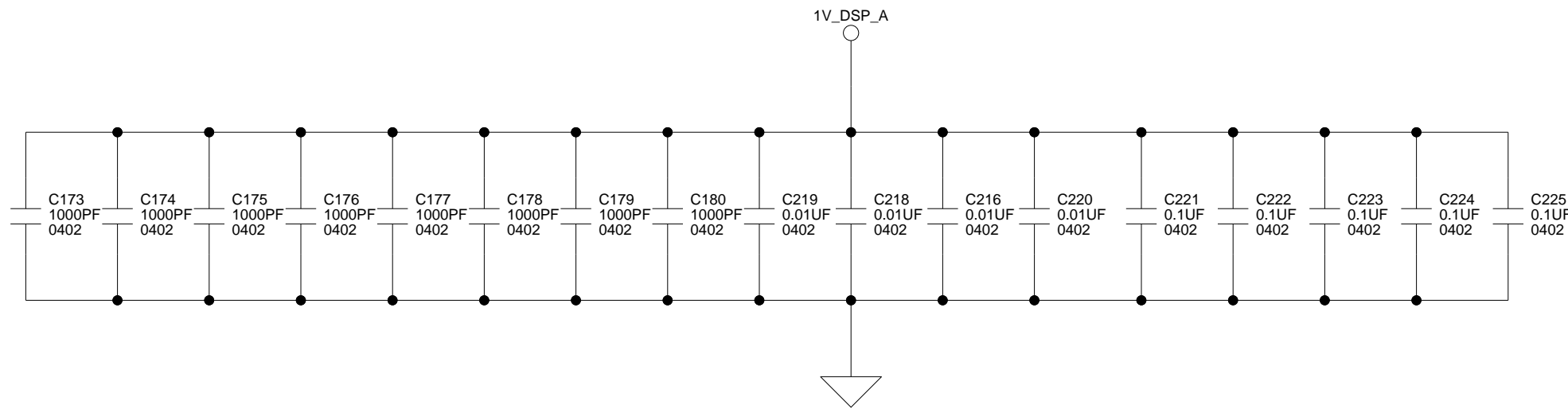


 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-TS201S EZ-KIT LITE POWER PAGE1	
Size C	Board No. A0178-2002	Rev 2.1C	
Date 1-10-2007_10:57	Sheet 13 of		15



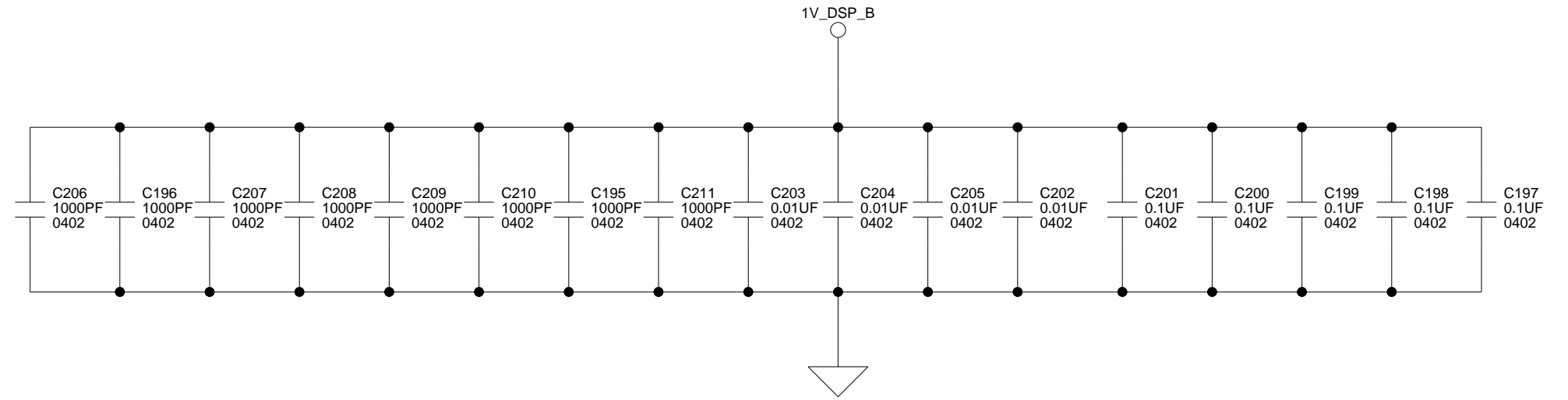
 ANALOG DEVICES		20 Cotton Road Nashua, NH 03063 PH: 1-800-ANALOGD	
		Title ADSP-TS201S EZ-KIT LITE POWER PAGE2	
Size C	Board No. A0178-2002	Rev 2.1C	
Date 1-10-2007_10:57	Sheet 14 of		15

VDD (1.0V) Bypass Caps (per DSP)
 (8) 1nF
 (4) 0.01uF
 (5) 0.1uF
 (1) 100uF

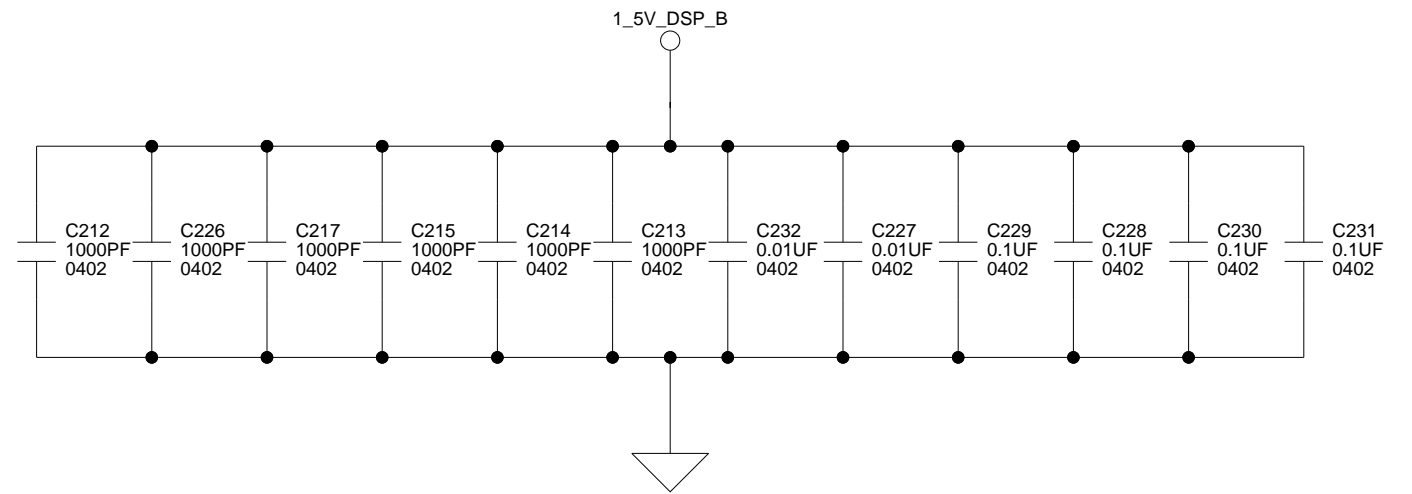
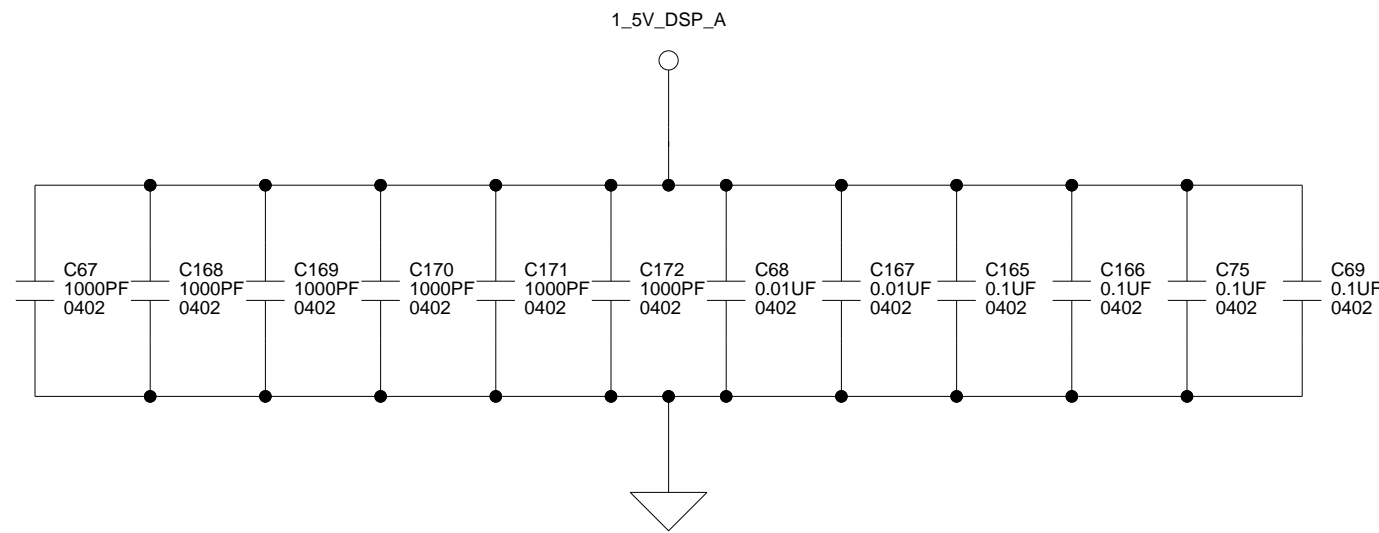


ALL BYPASS CAPS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE CORISpondING IC TRACES FROM COMPONENT TO CAPACITOR AND FROM THE CAPACITOR TO GND SHOULD BE AS SHORT AS POSSIBLE THE PRIORITY FOR THE PLACEMENT:

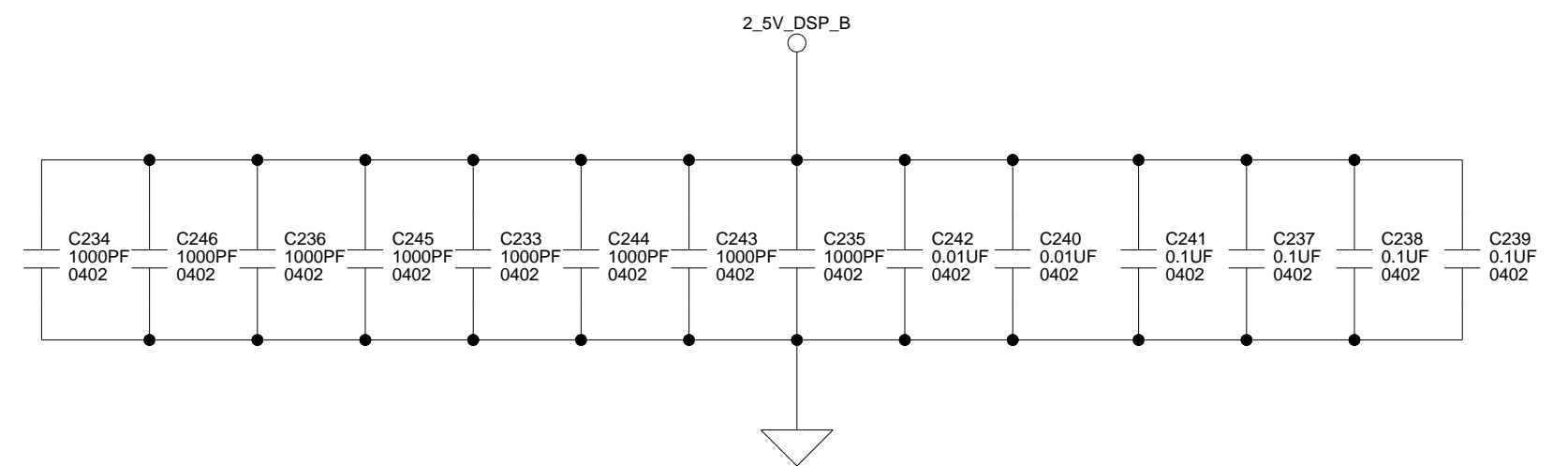
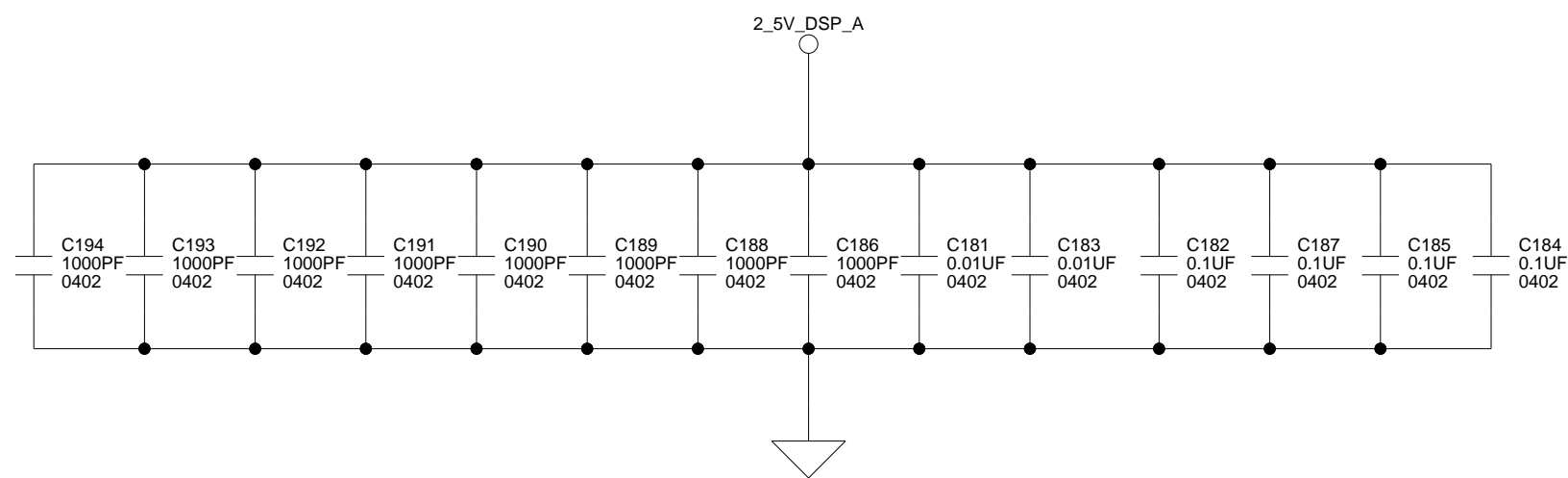
- 1V_DSP_X
- 1.5V_DSP_X
- 2.5V_DSP_X

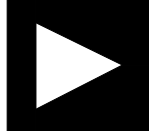


VDD_DRAM (1.5V) Bypass Caps (per DSP)
 (6) 1nF
 (2) 0.01uF
 (4) 0.1uF
 (1) 100uF



VDD_IO (2.5V) Bypass Caps (per DSP)
 (8) 1nF
 (2) 0.01uF
 (4) 0.1uF
 (1) 100uF



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		Title ADSP-TS201S EZ-KIT LITE DSP BYPASS CAPS	
Size C	Board No. A0178-2002	Rev 2.1C	
Date 1-10-2007_10:57	Sheet 15 of 15		

I INDEX

A

- AD1854 digital-to-analog converters (DACs),
1-12
- AD1871 analog-to-digital converters (ADCs),
1-12
- amplification gains, 2-5
- audio
 - amplification selection (SW1), 2-5
 - connectors (J9-10), 2-21
 - interface, 1-12

B

- bill of materials, A-1
- BMS boot memory select pins, 1-7, 2-3
- board schematic, B-1
- boot mode switch (SW2), 2-7
- bus control configuration, 1-9

C

- CLKIN pins, 2-12
- CLKOUT pins, 2-4
- clock
 - frequency, 2-12
 - generator (U1), 2-3, 2-12
 - ratio settings, 2-13
- codecs, *See* AD1871, AD1854
- complex programmable logic device (CPLD),
1-12
- configuration, of this EZ-KIT Lite, 1-3
- configuration resistors, 2-10

connectors

- diagram of locations, 1-4, 2-20
- J10 (audio out), 2-21
- J1 (expansion), 2-3, 2-22
- J2 (expansion), 2-3, 2-22
- J3 (expansion), 2-3, 2-22
- J4-7 (link ports), 2-23
- J8 (power), 2-21
- J9 (audio in), 2-5, 2-21
- ZJ1 (USB), 2-22
- ZP4 (JTAG), 2-4, 2-21

- contents, of this EZ-KIT Lite package, 1-2
- CONTROLIMP1-0 resistors, 2-14
- control impedance selection (R131, R143),
2-14

core

- power regulators, 2-2
- speed, 2-3
- customer support, xiv

D

- D23-0 pins, 1-12
- default configuration, of this EZ-KIT Lite, 1-3
- DIP switches
 - diagram of locations, 2-5
 - SW10, 2-5, 2-9
 - SW1 (audio amplification) switch, 2-5
 - SW2, 2-5, 2-7, 2-8
- driver mode resistors (CONTROLIMP1-0),
2-14
- drive strength selection (R132, R135-136), 2-15

INDEX

DS2-0 pins, 2-15

E

EPROM boot mode, 2-7

example programs, 1-13

expansion interface, 2-3, 2-9, 2-22

external

interrupts, 1-11

memory, xi, 1-7, 2-4

memory space (MSSD0), 1-8

ports, 2-3

voltage regulator, 2-3

EZ-KIT Lite board architecture, 2-2

F

features, of this EZ-KIT Lite, x

field-programmable gate arrays (FPGAs), ix

FLAG

LEDs (LED3-6), 2-17

push buttons (SW6-9), 2-18

source switch (SW10), 2-9

FLAG0_A (SW9) pins, 1-11, 2-18

FLAG0_B (SW6) pins, 1-11, 2-18

FLAG1_A (SW8) pins, 1-11, 2-18

FLAG1_B (SW7) pins, 1-11, 2-18

FLAG2_A (LED4) pins, 1-11, 2-18

FLAG2_B (LED5) pins, 1-11, 2-18

FLAG3_A (LED6) pins, 1-11, 1-12, 2-18

FLAG3_B (LED3) pins, 1-11, 1-12, 2-18

FLAGREG registers, 1-10

flash memory

boot memory select pins, 2-3

map of, 1-9

frequency, 1-13, 2-12

G

general-purpose IO pins, -xi, 2-18

GND pins, 2-23

I

impedance selection, 2-14

input clock, 2-3

installation, of this EZ-KIT Lite, 1-5

interface connectors, xi

internal

DRAM power regulator, 2-2

memory, 1-7, 1-8, 2-4

interrupt

enable settings (SW2), 2-8

pins (IRQ3-0), 1-11

push buttons (SW4-5), 2-19

source switch (SW10), 2-9

IRQ0_A (SW4) interrupt pins, 1-11, 2-19

IRQ0_B (SW5) interrupt pins, 1-11, 2-19

J

JTAG

connector (ZP4), 2-4, 2-21

emulation port, 2-4

L

LEDs

diagram of locations, 1-4, 2-16

LED1 (power), 2-16

LED3 (FLAG3_B), 1-11, 2-18

LED4 (FLAG2_A), 1-11, 2-18

LED5 (FLAG2_B), 1-11, 2-18

LED6 (FLAG3_A), 1-11, 2-18

LED8 (master reset), 2-16

ZLED3 (USB monitor), 1-5, 2-18

license restrictions, 1-7

link ports

connections, 1-12

width settings (SW2), 2-8

LVDS signaling, 1-12

M

master processors, [2-10](#)
 memory
 map, of this EZ-KIT Lite, [1-7](#)
 select pins, See [~BMS](#), [~MS0](#), [1-7](#)
 microphones, [2-5](#)
 ~MS0 memory bank 0 select pins, [1-7](#), [1-8](#), [2-3](#)
 MSSD0 external memory space, [1-8](#)

N

notation conventions, [xxi](#)

O

oscillators (U18), [2-3](#), [2-12](#)

P

package contents, [1-2](#)
 power
 connector (J8), [2-21](#)
 LED (LED1), [2-16](#)
 regulators, [2-2](#)
 supply specifications, [2-23](#)
 processor IDs, [1-8](#), [1-12](#), [2-10](#), [2-15](#)
 programmable flag pins, See [flags by name](#)
 (FLAGS)
 push buttons
 See *also* [push buttons by name \(SWx\)](#)
 diagram of locations, [2-16](#)

R

registration, of this product, [1-3](#)
 reset
 master (LED8), [2-16](#)
 processor, [2-6](#)
 push button (SW3), [2-19](#)

resistors

 diagram of locations, [2-10](#)
 clock mode settings, [2-12](#)
 control impedance selection, [2-14](#)
 drive strength selection, [2-15](#)
 processor ID settings, [2-11](#)
 restrictions, of the license, [1-7](#)
 RJ-45 connectors, [1-12](#), [2-23](#)
 RX port, [1-12](#)

S

schematic, of this EZ-KIT Lite, [B-1](#)
 SCLK pins, [2-14](#)
 SCLKRAT2-0 pins, [2-3](#), [2-12](#), [2-13](#)
 SDRAM
 interface, [1-8](#)
 start/end addresses, [1-8](#)
 SDRCON registers, [1-8](#), [2-7](#)
 setup, of this EZ-KIT Lite, [1-4](#)
 SOC registers, [1-8](#)
 specifications, of the power supply, [2-23](#)
 SQSTAT registers, [1-10](#)
 startup, of this EZ-KIT Lite, [1-5](#)
 SW10 (FLAG/IRQ) DIP switch, [2-9](#)
 SW1 (audio amplification) switch, [2-5](#)
 SW2 DIP switch, [2-7](#), [2-8](#)
 SW3 (reset) push button, [2-19](#)
 SW4 (IRQ0_A) push button, [1-11](#), [2-19](#)
 SW5 (IRQ0_B) push button, [1-11](#), [2-19](#)
 SW6 (FLAG0_B) push button, [1-11](#), [2-18](#)
 SW7 (FLAG1_B) push button, [1-11](#), [2-18](#)
 SW8 (FLAG1_A) push button, [1-11](#), [2-18](#)
 SW9 (FLAG0_A) push button, [1-11](#), [2-18](#)
 SYSCON registers, [1-8](#), [2-7](#)
 system architecture, of this EZ-KIT Lite, [2-2](#)

T

TX port, [1-12](#)

INDEX

U

USB

- cable, [1-3](#)
- connector (ZJ1), [2-22](#)
- interface, [1-9](#), [2-7](#), [2-21](#)
- monitor LED (ZLED3), [2-18](#)

V

VisualDSP++

- documentation, [xix](#)
- environment, [1-5](#)
- online Help, [xviii](#)
- voltage regulators, [xi](#), [2-2](#)