QPRO Family of XC1700E Configuration PROMs

DS670 (v1.0) December 3, 2010

Product Specification

Features

- Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams of Xilinx FPGA devices
- On-chip address counter, incremented by each rising edge on the clock input
- Simple interface to the FPGA requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- Low-power CMOS EPROM process
- Available in 5V version only
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages

Description

The XC1700E QPRO™ family of configuration PROMs provide an easy-to-use, cost-effective method for storing Xilinx FPGA configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the FPGA D_{IN} pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When the FPGA is in Slave Serial mode, the PROM and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx Alliance™ or the Foundation™ series development systems compiles the FPGA design file into a standard HEX format which is then transferred to most commercial PROM programmers.

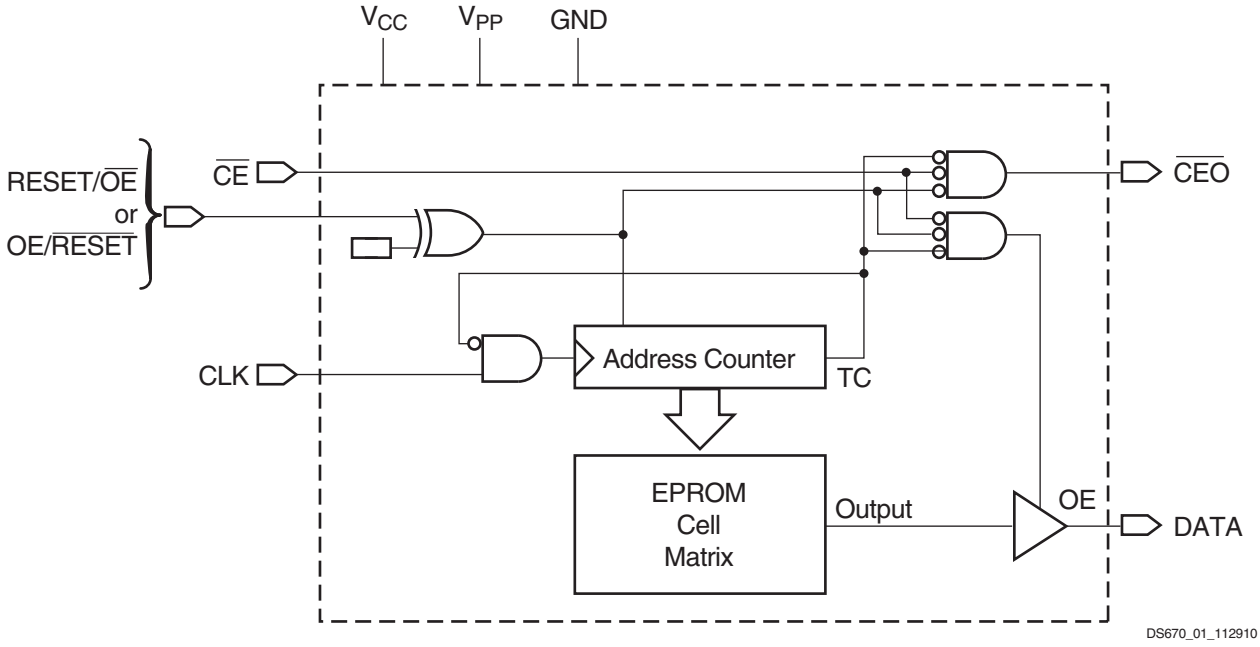


Figure 1: **Simplified Block Diagram (Does Not Show Programming Circuit)**

Pin Description

DATA

Data output, 3-stated when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O.

Note: $\overline{OE}$ can be programmed to be either active High or active Low.

CLK

Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.

RESET/$\overline{OE}$

When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is put in a high-impedance state. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be driven by the FPGA's $\overline{INIT}$ pin.

The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 programmer software. Third-party programmers have different methods to invert this pin.

CE

When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low-I_{CC} standby mode.

CEO

Chip enable output, to be connected to the $\overline{CE}$ input of the next PROM in the daisy chain. This output is Low when the $\overline{CE}$ and $\overline{OE}$ inputs are both active AND the internal address counter has been incremented beyond its terminal count (TC) value. In other words: when the PROM has been read, $\overline{CEO}$ will follow $\overline{CE}$ as long as $\overline{OE}$ is active. When $\overline{OE}$ goes inactive, $\overline{CEO}$ stays High until the PROM is reset.

Note: $\overline{OE}$ can be programmed to be either active High or active Low.

V_{PP}

Programming voltage. No overshoot above the specified maximum voltage is permitted on this pin. For normal read operation, this pin *must* be connected to V_{CC}. Failure to do so can lead to unpredictable, temperature-dependent operation and severe problems. Do not leave V_{PP} floating!

V_{CC} and GND

V_{CC} is positive supply pin and GND is ground pin.

PROM Pinouts

Table 1: **PROM Pinouts**

Pin Name	Pin Number
DATA	1
CLK	2
RESET/$\overline{OE}$ ($OE/\overline{RESET}$)	3
$\overline{CE}$	4
GND	5
$\overline{CEO}$	6
V_{PP}	7
V_{CC}	8

Capacity

Table 2: **Capacity**

Devices	Configuration Bits
XC1765E	65,536
XC17256E	262,144

Number of Configuration Bits, Including Header, for Xilinx FPGAs and Compatible PROMs

Table 3: **Number of Configuration Bits, Including Header, for Xilinx FPGAs and Compatible PROMs**

Device	Configuration Bits	PROM
XC3000/A series	14,819 to 94,984	XC1765E to XC17256E
XC4000 series	95,008 to 247,968	XC17256E
XQ4005E	95,008	XC17256E
XQ4010E	178,144	XC17256E
XQ4013E	247,968	XC17256E

Controlling PROMs

Connecting the FPGA device with the PROM.

- The DATA output(s) of the PROM(s) drives the D_{IN} input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The $\overline{RESET}$/OE input of all PROMs is best driven by the $\overline{INIT}$ output of the lead FPGA device. This connection assures that the PROM address counter is reset before the start of any reconfiguration, even when a reconfiguration is initiated by a V_{CC} glitch. Other methods—such as driving $\overline{RESET}$/OE from $\overline{LDC}$ or system reset—assume the PROM internal power-on-reset is always in step with the FPGA's internal power-on-reset. This might not be a safe assumption.
- The PROM $\overline{CE}$ input can be driven from either the $\overline{LDC}$ or DONE pins. Using $\overline{LDC}$ avoids potential contention on the D_{IN} pin.
- The $\overline{CE}$ input of the lead (or only) PROM is driven by the DONE output of the lead FPGA device, provided that DONE is not permanently grounded. Otherwise, $\overline{LDC}$ can be used to drive $\overline{CE}$, but must then be unconditionally High during user operation. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the configurable logic block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. The Xilinx PROMs have been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an FPGA. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function D_{IN} pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. Xilinx FPGAs take care of this automatically with an on-chip default pull-up resistor.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple FPGA-configurations for a single FPGA are stored in a PROM, the $\overline{OE}$ pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{OE}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

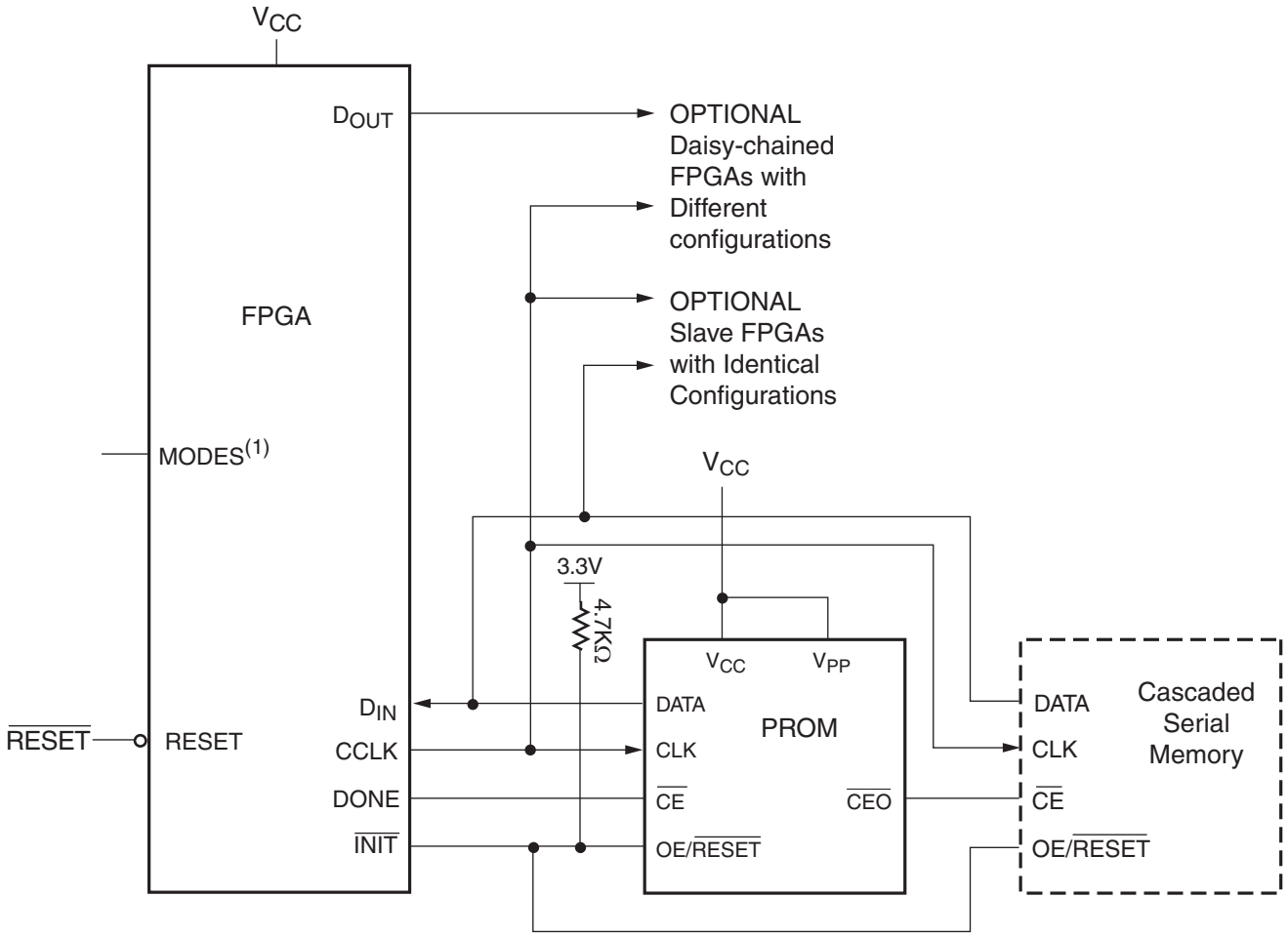
This method fails if a user applies $\overline{RESET}$ during the FPGA configuration process. The FPGA aborts the configuration and then restarts a new configuration, as intended, but the PROM does not reset its address counter, since it never saw a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the FPGA is the master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and DONE goes High. However, the FPGA configuration will be completely wrong, with potential contentions inside the FPGA and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

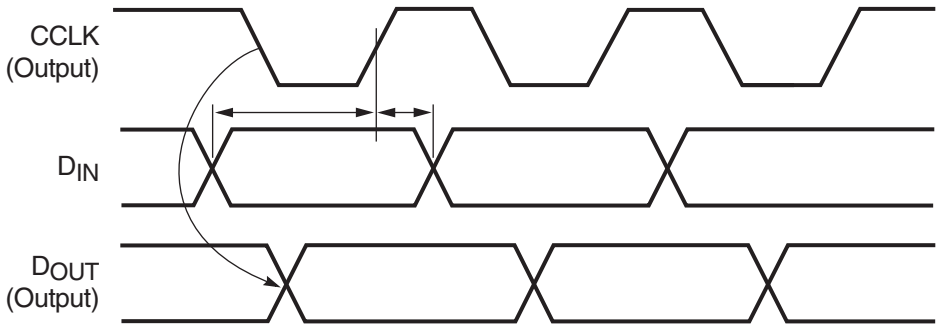
Cascading Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for future FPGAs requiring larger configuration memories, cascaded PROMs provide additional memory. After the last bit from the first PROM is read, the next clock signal to the PROM asserts its $\overline{CEO}$ output Low and disables its DATA line. The second PROM recognizes the Low level on its CE input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded PROMs are reset if the FPGA $\overline{RESET}$ pin goes Low, assuming the PROM reset polarity option has been inverted.

To reprogram the FPGA with another program, the DONE line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of D_{IN}.





Notes:
1. For mode pin connections, refer to the appropriate FPGA data sheet.
2. The one-time-programmable PROM supports automatic loading of configuration programs.
3. Multiple devices can be cascaded to support additional FPGAs.
4. An early DONE inhibits the PROM data output one CCLK cycle before the FPGA I/Os become active.

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Figure 2: **Master Serial Mode**

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Programming

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

Table 4: **Truth Table for XC1700 Control Inputs**

Control Inputs		Internal Address	Outputs		
RESET(1)	**CE**		**DATA**	**CEO**	**I_{CC}**
Inactive	Low	If address ≤ TC: increment If address > TC: don't change(2)	Active High-Z	High Low	Active Reduced
Active	Low	Held reset	High-Z	High	Active
Inactive	High	Not changing	High-Z(3)	High	Standby
Active	High	Held reset	High-Z(3)	High	Standby

Notes:

1. The XC1700 RESET input has programmable polarity
2. TC = Terminal Count = highest address value with valid data.
3. Pull DATA pin to GND or V_{CC} to meet I_{CCS} standby current.

Note: Always tie the V_{PP} pin to V_{CC} in your application. Never leave V_{PP} floating.

XC1765E and XC17256E

Absolute Maximum Ratings

Table 5: **Absolute Maximum Ratings**

Symbol	Description	Range	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND	–0.5 to +12.5	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to V_{CC} + 0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_j	Junction temperature (10s @ 1/16 in.)	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Table 6: **Operating Conditions**

Symbol	Description	Min	Max	Units
V_{CC}[(1)]	Supply voltage relative to GND (T_C = –55°C to +125°C)	4.50	5.50	V

Notes:

1. During normal read operation V_{PP} *must* be connected to V_{CC}

DC Characteristics Over Operating Condition

Table 7: **DC Characteristics Over Operating Condition**

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –4 mA)		3.7	–	V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)		–	0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency)		–	10	mA
I_{CCS}	Supply current, standby mode	XC17256E	–	50[(1)]	µA
		XC1765E	–	1.5[(1)]	mA
I_L	Input or output leakage current		–10	10	µA
C_{IN}	Input capacitance (V_{IN} = GND, f = 1.0 MHz) sample tested		–	10	pF
C_{OUT}	Output capacitance (V_{IN} = GND, f = 1.0 MHz) sample tested		–	10	pF

Notes:

1. I_{CCS} standby current is specified for DATA pin that is pulled to V_{CC} or GND.

AC Characteristics Over Operating Condition

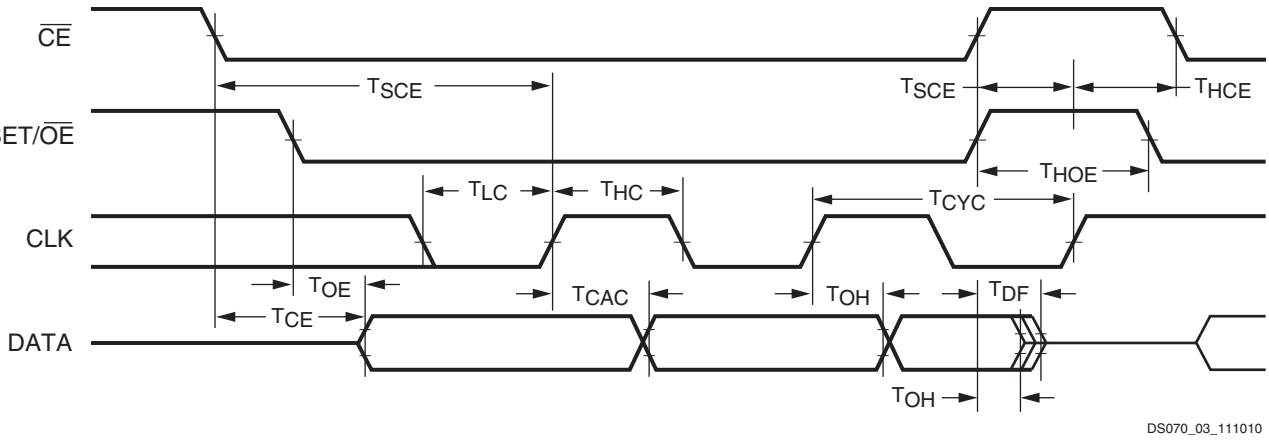

Figure 3: **AC Characteristics Over Operating Condition**

Table 8: **AC Characteristics Over Operating Condition(1)(2)**

Symbol	Description	XC1765E		XC17256E		Units
		Min	Max	Min	Max	
T_{OE}	$\overline{OE}$ to data delay	–	45	–	25	ns
T_{CE}	$\overline{CE}$ to data delay	–	60	–	45	ns
T_{CAC}	CLK to data delay	–	150	–	50	ns
T_{OH}	Data hold from $\overline{CE}$, $\overline{OE}$, or CLK(3)	0	–	0	–	ns
T_{DF}	$\overline{CE}$ or $\overline{OE}$ to data float delay(3)(4)	–	50	–	50	ns
T_{CYC}	Clock periods	200	–	80	–	ns
T_{LC}	CLK Low time(3)	100	–	20	–	ns
T_{HC}	CLK High time(3)	100	–	20	–	ns
T_{SCE}	$\overline{CE}$ setup time to CLK (to guarantee proper counting)	25	–	20	–	ns
T_{HCE}	$\overline{CE}$ hold time to CLK (to guarantee proper counting)	0	–	0	–	ns
T_{HOE}	$\overline{OE}$ hold time (guarantees counters are reset)	100	–	20	–	ns

Notes:

1. AC test load = 50 pF
2. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
3. Guaranteed by design, not tested.
4. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.

AC Characteristics Over Operating Condition When Cascading

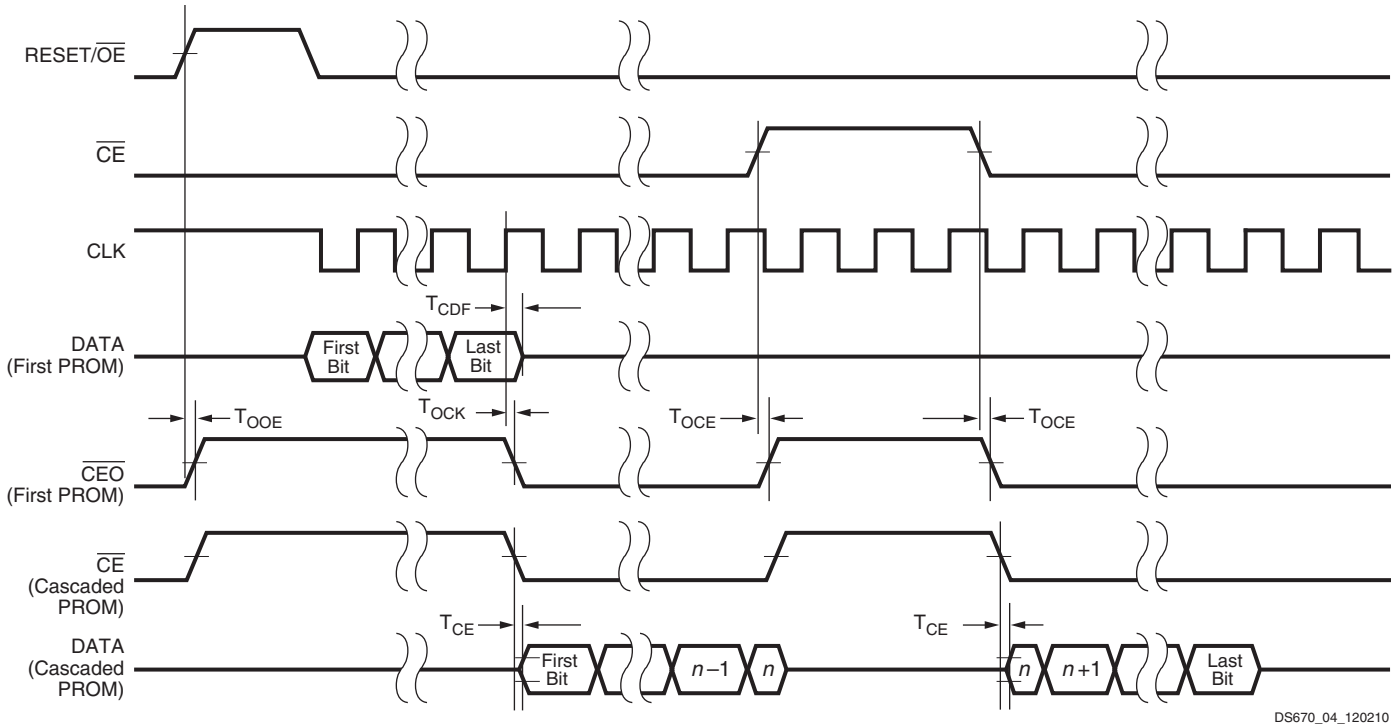

Figure 4: **AC Characteristics Over Operating Condition When Cascading**

Table 9: **AC Characteristics Over Operating Condition When Cascading(1)(2)**

Symbol	Description	XC1765E		XC17256E		Units
		Min	Max	Min	Max	
T_{CDF}	CLK to data float delay(3)(4)	–	50	–	50	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3)	–	65	–	30	ns
T_{OCE}	CE to $\overline{CEO}$ delay(3)	–	45	–	35	ns
T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ delay(3)	–	40	–	30	ns

Notes:

1. AC test load = 50 pF
2. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
3. Guaranteed by design, not tested.
4. Float delays are measured with 5 pF AC loads. Transition is measured at ±200mV from steady state active levels.

Ordering Information

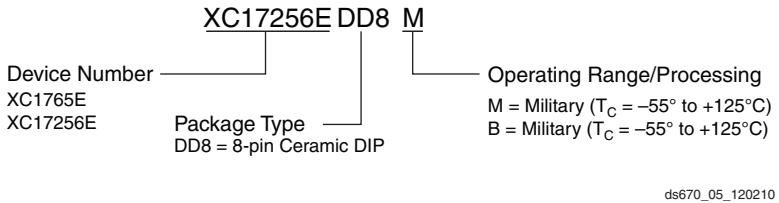

Figure 5: **Ordering Information**

Valid Ordering Combinations

Table 10: **Valid Ordering Combinations**

XC17256EDD8M	XC1765EDD8M
XC17256EDD8B	XC1765EDD8B

Marking Information

Due to the small size of the PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Devices are marked as shown in Figure 6.

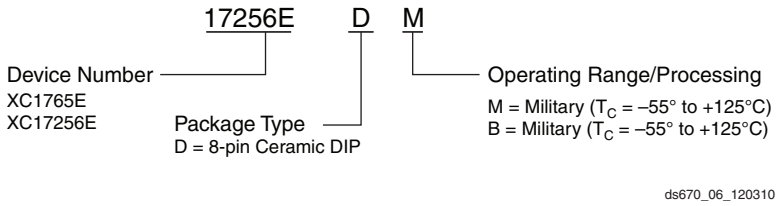

Figure 6: **Marking Information**

Revision History

The following table shows the revision history for this document.

Date	Version	Revisions
12/03/10	1.0	Initial Xilinx release.

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