

# MN103SL7 Series

## 32-bit Single-chip Microcontroller

### Overview

The MN103S is a 32-bit microcontroller combining ease of use intended for programs development in the C language with a simple, high-performance architecture made possible through pursuit of cost performance.

This LSI series is well suited for in-vehicle electrical compressor control, in-vehicle body control, air conditioner, electrical power control and other applications.

Built around a compact 32-bit CPU with a basic instruction word length of 1 byte, this LSI includes internal memory for instructions and data, DMA controller, a clock generator, bus controller, interrupt controller, watchdog timer, standard peripheral circuitry such as timers and serial interfaces, PWM circuit best suited to controlling 3-phase motors, arithmetic unit for speed-up of inverter control and A/D converters for motor position control. The MN103S Series' high-speed CPU coupled with abundance of peripheral features provides an easy means of developing low-cost, high-performance and multifunctional system on LSI for motor and power control applications requiring fast response - a feature previously unavailable with conventional microcontrollers.

### Product Summary

This datasheet describes the following model.

Model	ROM Size	RAM Size	Classification	Package
MN103SFL7G	128 KB	12 KB	Flash EEPROM version	TQFP048-P-0707F
MN103SFL7K	256 KB			

## Features

### CPU core

MN103S core  
4 GB of memory space (for instructions / data)  
LOAD/STORE architecture with 5-stage pipeline  
46 basic instructions + 23 extended arithmetic instructions  
6 addressing modes  
Instruction set of 1 byte in word length  
Extended arithmetic unit incorporated (high-speed multiply/divide instructions)  
Machine cycle: 16.7 ns (oscillation frequency: 10 MHz, 6 multiplying)  
Operation mode: NORMAL mode, SLEEP mode, HALT mode, STOP mode

### Oscillation Circuit

External high-speed oscillation (crystal/ ceramic)  
Internal high-speed oscillation (10 MHz)  
Internal low-speed oscillation for Watchdog timer 2 (35 kHz)

### Clock Multiplication Circuit

PLL output clock (IOCLK): High-speed oscillation is multiplied by 3 to 15

### Internal Memory

ROM 128 KB (MN103SFL7G), ROM 256 KB (MN103SFL7K)  
RAM 12 KB

### DMA Controller

Channel : 2 ch  
Transfer requests : 46 types  
(External interrupts: 8, Timer: 17, Serial: 6, IIC: 3, A/D converter: 4, CAN: 1, LIN: 1, PWM: 4,  
Power Voltage Detection: 1, Software: 1)  
Transfer mode : 3 modes (One word transfer / Burst transfer / Intermittent transfer)

Features (continued)

Interrupts

Internal interrupts 48 interrupts

~~DWFKGRWLP~~HURHURZLQWHUUSWV

System error interrupts

Fail safe function interrupts

~~DWFKGRWLP~~HURHURZLQWHUUSWV ~~ORENHUURUGHWHEWLRQSHLMWHUSURWHEW~~

Power voltage detection interrupts

<Timer Interrupts>

~~7LPHUQGHURZLQWHUUSW~~

~~7LPHUQGHURZLQWHUUSW~~

~~7LPHUQGHURZLQWHUUSW~~

~~7LPHUQGHURZLQWHUUSW~~

~~7LPHUQGHURZLQWHUUSW~~

~~7LPHUQGHURZLQWHUUSW~~

~~7LPHUQGHURZLQWHUUSW~~

~~7LPHUQGHURZLQWHUUSW~~

~~7LPHURHURZQGHURZLQWHUUSW~~

Timer 16 compare/capture A interrupt

Timer 16 compare/capture B interrupt

~~7LPHURHURZQGHURZLQWHUUSW~~

Timer 18 compare/capture A interrupt

Timer 18 compare/capture B interrupt

~~7LPHURHURZQGHURZLQWHUUSW~~

Timer 19 compare/capture A interrupt

Timer 19 compare/capture B interrupt

<Serial interface>

Serial 0 UART reception completion interrupt

Serial 0 clock synchronous communication completion /UART transmission completion interrupt

Serial 0 transmission data buffer empty interrupt

Serial 1 UART reception completion interrupt

Serial 1 clock synchronous communication completion /UART transmission completion interrupt

Serial 1 transmission data buffer empty interrupt

IIC stop condition detection interrupt

IIC communication end interrupt

IIC transmission data buffer empty interrupt

LIN interrupt

CAN interrupt

<PWM>

~~3:0RHURZLQWHUUSW~~

~~3:0QGHURZLQWHUUSW~~

PWM0 synchronous A/D conversion start A interrupt

PWM0 synchronous A/D conversion start B interrupt

<A/D>

A /D 0 conversion end interrupt

A /D 0 conversion end B interrupt

A /D 1 conversion end interrupt

A /D 1 conversion end B interrupt









Features (continued)

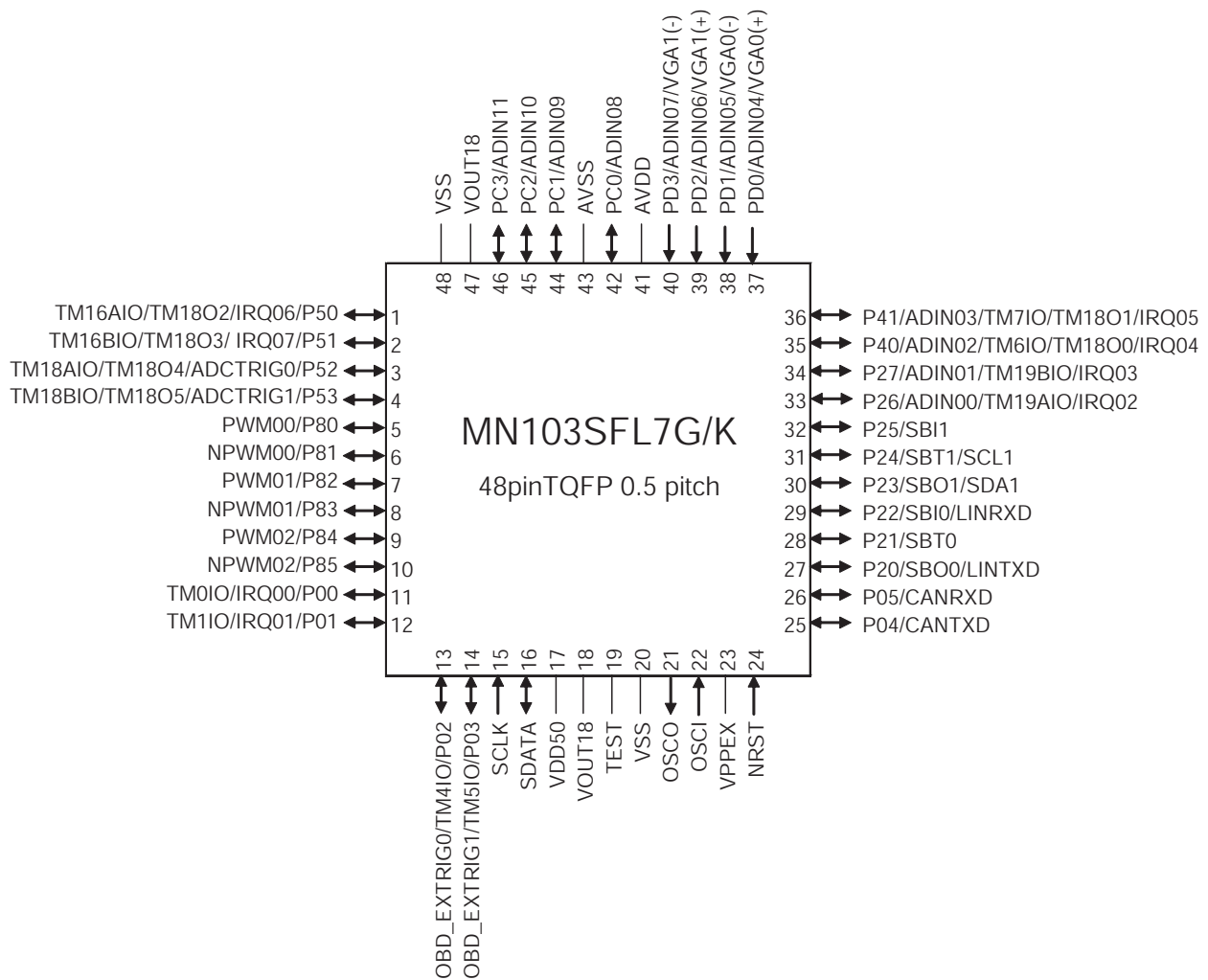
Port / pins

I/O ports	30 pins
Motor control output	6 pins
External interrupt	8 pins
A/D input	8 pins
Input ports	4 pins
VGA, A/D input	4 pins
Special pins	14 pins
Reset input pin	1 pin
Oscillation pin	2 pins
Test mode input pin	2 pins
Power pin	7 pins
On-board debugger pin	2 pins

Package Code name

TQFP48 (7 mm square, 0.5 mm pitch, halogen free)  
TQFP048-P-0707F

Pin Description





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