CAN/LIN SBC Family with DC/DC Voltage Regulator E521.02/03/04/12/13/14

PRODUCTION DATA – Mar 7, 2016

Features

- High efficiency 5V DC/DC buck converter
- Optional DC/DC boost converter
- Wakeable HS-CAN transceiver (ISO11898-2 and -5)
- Up to four LIN transceiver LIN 2.1, SAE-J2602 conformance
- Operating range 2.5V up to 28V
- Typ. 45µA sleep current consumption
- Typ. 85µA standby current consumption with active DC/DC buck converter
- Configurable µC watchdog (cycle time and type)
- BUS pins ESD-protected 8kV according to IEC-61000-4-2
- Package QFN44L7

with Booster	*Without Booster*	*No. of LINs*
E521.12	E521.02	2
E521.13	E521.03	3
E521.14	E521.04	4

Applications

- Body control units, gateways

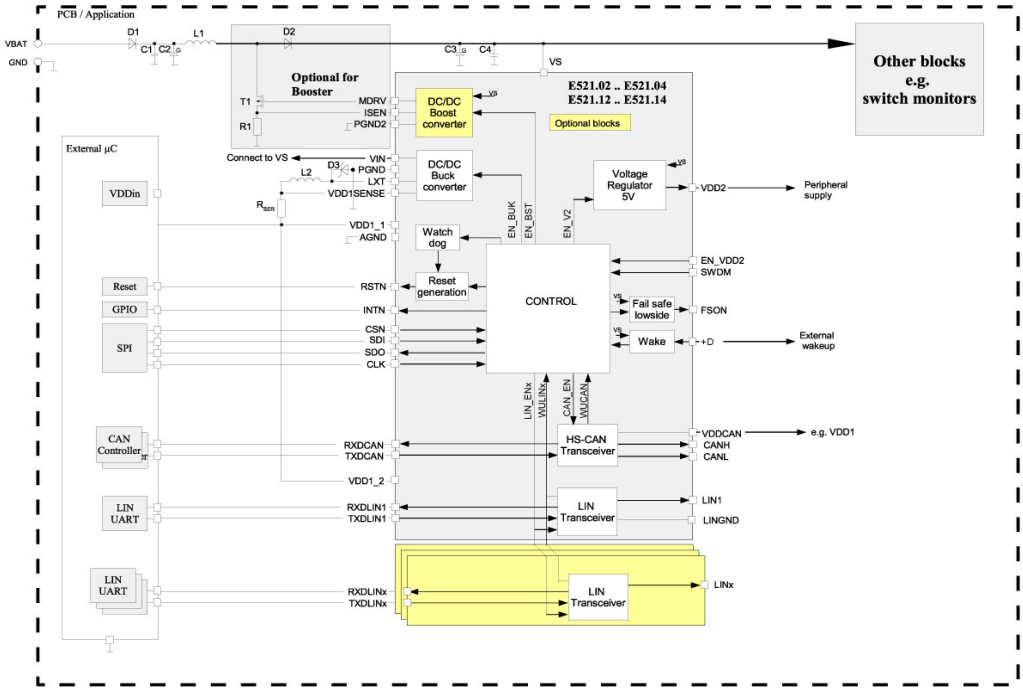
General Description

The CAN/LIN SBC family with DC/DC voltage regulator provides beside the CAN and LIN tranceivers the main µC power supply with a high efficiency DC/DC converter. An additional linear regulator can be used independently as peripheral supply. All supplies are monitored and can signalize a fail event by SPI interface. The main DC/DC supply monitor can generate a µC reset. System failure can activate a fail-safe output signal for limp home support.

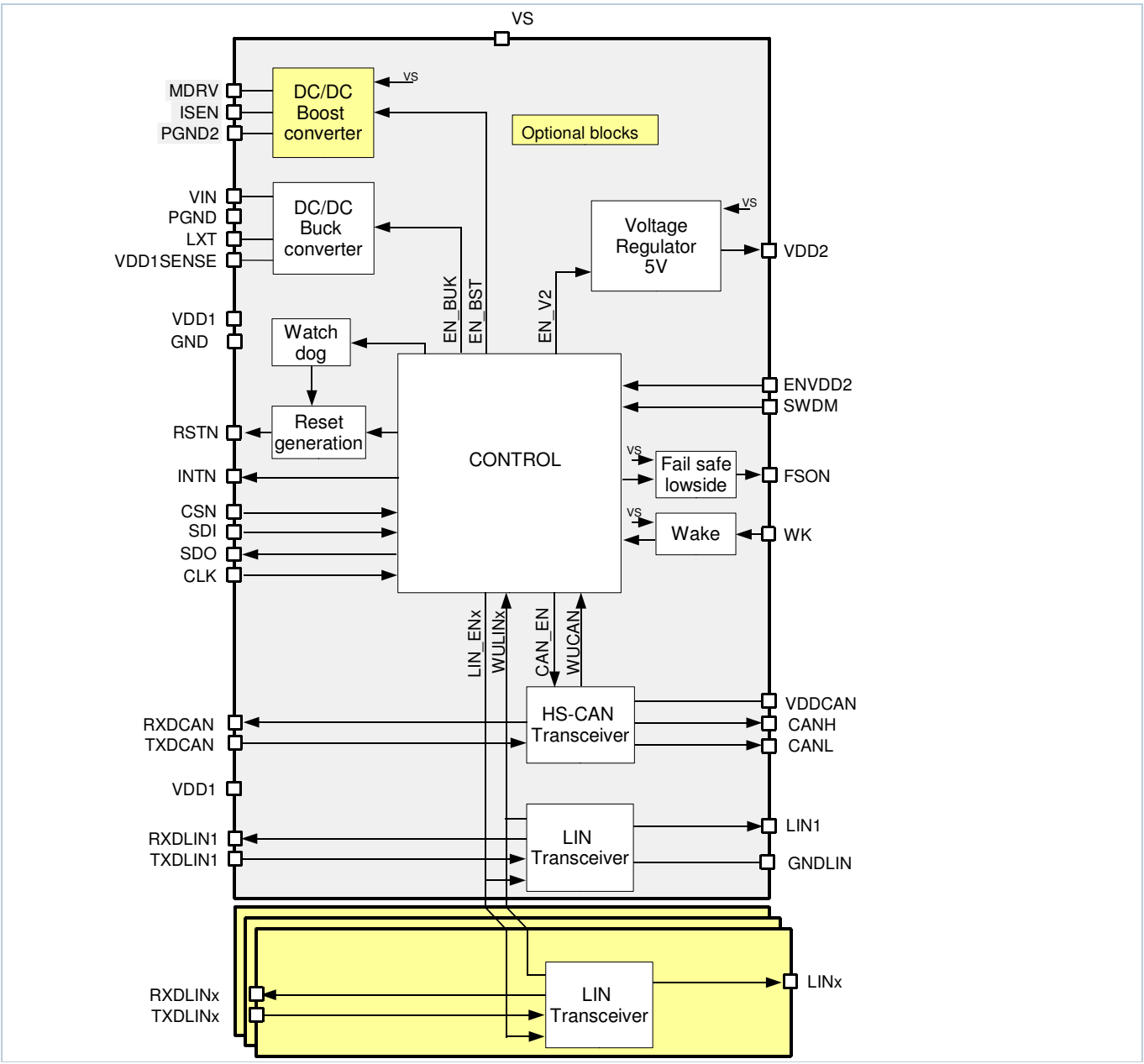
The CAN/LIN SBC family provides SLEEP, STOP, ACTIVE and FAILSAFE states.

The device is capable of detecting local and remote wake-up events which can be individually enabled via SPI.

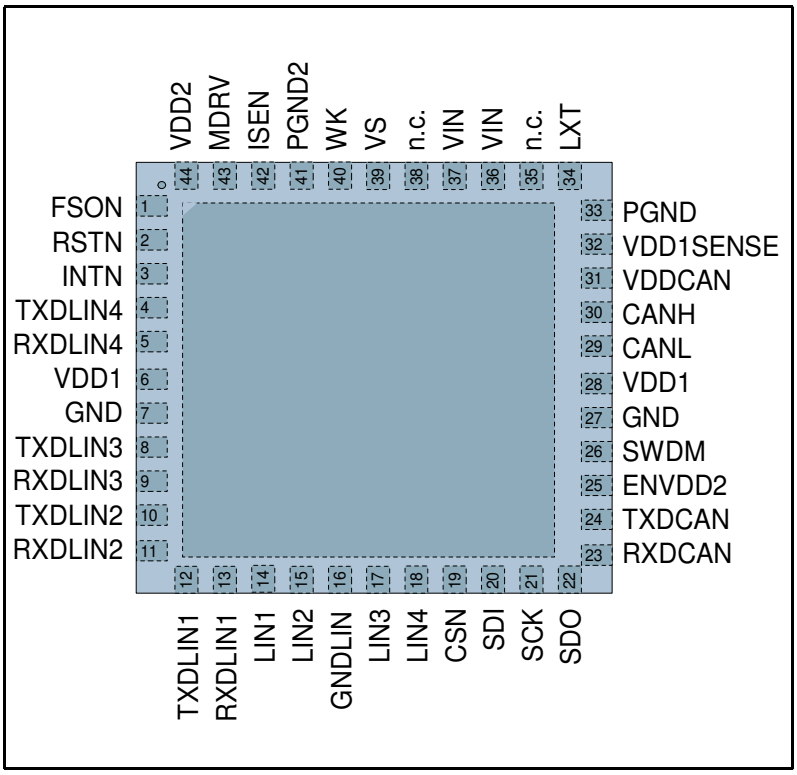
Typical Applications Circuit



Functional Diagram



Pin Configuration



Note: Top view, not to scale

Pin Description

Pin	*Name*	*Type*	*Description*
1	FSON	O	Fail safe output, open drain stage, low active
2	RSTN	IO	Reset output, low active, pull up
3	INTN	IO	Interrupt output, low active, pull up Setup for bit SBC.CFG
4	TXDLIN4	I	LIN4 transmit data, pull up, optional E521.04/.14, only all other versions are not connected
5	RXDLIN4	O	LIN4 receive data E521.04/.14 only, all other versions are not connected
6	VDD1	S	Voltage Supply 1
7	GND	S	Ground
8	TXDLIN3	I	LIN3 transmit data, pull up, optional E521.03/.04/.13/.14 only, all other versions are not connected

Pin	Name	Type	Description
9	RXDLIN3	O	LIN3 receive data E521.03/.04/.13/.14 only, all other versions are not connected
10	TXDLIN2	I	LIN2 transmit data, pull up
11	RXDLIN2	O	LIN2 receive data
12	TXDLIN1	I	LIN1 transmit data, pull up
13	RXDLIN1	O	LIN1 receive data
14	LIN1	IO	LIN1 bus line
15	LIN2	IO	LIN2 bus line
16	GND	S	LIN ground
17	LIN3	IO	LIN3 bus line, E521.03/.04/.13/.14 only, all other versions are not connected
18	LIN4	IO	LIN4 bus line, E521.04/.14 only, all other versions are not connected
19	CSN	I	SPI chip select, low active, pull up
20	SDI	I	SPI serial data input
21	SCK	I	SPI clock, pull down
22	SDO	O	SPI serial data output
23	RXDCAN	O	CAN receive data
24	TXDCAN	I	CAN transmit data, pull up
25	ENVDD2	I	Enables VDD2
26	SWDM	I	Must be connected to GND in application Enables software development function, pull down
27	GND	S	Ground
28	VDD1	S	Voltage Supply 1
29	CANL	IO	CANL bus Line
30	CANH	IO	CANH bus Line
31	VDDCAN	S	HS-CAN supply
32	VDD1SENSE	IO	VDD1 Sense Back to DCDC Buck Converter
33	PGND	S	DCDC Buck Converter Power Ground
34	LXT	IO	DCDC Buck Converter Integrated Highside Switch Output

Pin	Name	Type	Description
35	n.c.		Not connected
36	VIN	S	DCDC Supply
37	VIN	S	DCDC Supply
38	n.c.		Not connected, leave open
39	VS	S	Battery supply voltage
40	WK	I	Local wake up input, pull up or pull down
41	PGND2	S	Power ground 2 (Boost Converter), E521.12/.13/.14 only, all other versions are not connected
42	ISEN	I	Sense Input (Boost Converter), E521.12/.13/.14 only, all other versions are not connected
43	MDRV	O	Main Gate Driver Output (Boost Converter), E521.12/.13/.14 only, all other versions are not connected
44	VDD2	S	Peripheral voltage supply
-	EP	S	Exposed Pad. Connect to large copper ground plane for optimal heat dissipation. Connect to GNDA and GNDD.

Note: S = Supply, I/O = Input/Output

1 Absolute Maximum Ratings

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. **These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied.** Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages with respect to ground. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

Description	Condition	Symbol	Min	Max	Unit
Voltage at VS [1], [2]	continuous	V_{VS}	-0.3	40	V
Voltage at VIN [1], [2]	continuous	V_{VS}	-0.3	40	V
Voltage at WK, FSON, ENVDD	continuous	V_{WK}	-0.3	40	V
Voltage at LIN1..4, CANL, CANL	continuous	V_{CANL}	-27	40	V
Voltage at LXT	continuous	V_{LXT}	-2	V_{VIN} + 0.3	V
Voltage at VDDCAN	continuous	V_{VDDCAN}	-0.3	5.5	V
Voltage at SWDM	continuous	V_{SWDM}	-0.3	5.5	V
Voltage at digital pins TXDLIN1..4, RXDLIN1..4, TXDCAN, RXDCAN	continuous	V_{TXDLIN}	-0.3	V_{VDD1}+0.3	V
Voltage at VDD1	continuous	V_{VDD1}	-0.3	5.5	V
Voltage at VDD2	continuous	V_{VDD2}	-5	40	V
Current at WK	continuous	I_{WK}	-15	1	mA
Current of VDD1	continuous	I_{VDD1}	-500		mA
Current of VDD2, internally limited	continuous	I_{VDD2}	-200	1	mA
Current at ENVDD2	continuous	I_{ENVDD2}	-15	1	mA
Maximum load at RXDCAN		$C_{RXDCAN,LOAD}$		10	pF
Junction temperature	continuous	T_{JUNC}	-40	150	°C
Storage temperature	continuous	T_{STG}	-55	125	°C

[1] The device is implicitly protected against load dump

[2] The device is implicitly protected against jump start

2 ESD Protection

Description	Condition	Symbol	Min	Max	Unit
ESD HBM protection pins VDD2, LINx, WK, CANH and CANL	[1]	$V_{ESD(HBM)}$	-8	+8	kV
ESD HBM protection all other pins	[1]	$V_{ESD(HBM)}$	-2	+2	kV
ESD system level protection pins VDD2, LINx, WK, CANH and CANL	[3] to ground	$V_{ESD(IEC)}$	-6	+6	kV
ESD CDM Protection at all Pins	[2]	$V_{ESD(CDM)}$	-500	+500	V
ESD CDM Protection at Edge Pins	[2]	$V_{ESD(CDM)C}$	-750	+750	V

[1] According to AEC-Q100-002 (HBM) chip level test, C=100pF, R=1.5kΩ
[2] According to AEC-Q100-011 (CDM) chip level test, R=1Ω
[2] Similar to IEC61000-4-2, C=150pF, R=330Ω

3 Recommended Operating Conditions

Description	Condition	Symbol	Min	Typ	Max	Unit
Functional range E521.02..04		$V_{VS,FUNC}$	5.5	-	28	V
Functional range E521.12..14		$V_{VS,FUNC}$	2.5	-	28	V
Limited functional range E521.02..04		$V_{VS,FL,LR}$	2.5	-	5.5	V
Limited functional range E521.02..04, E521.12..14		$V_{VS,FL,HR}$	28	-	40	V
Ambient temperature		T_{AMB}	-40	-	125	℃

4 Electrical Characteristics

(V_{VS} = 5.5V to 28V, T_{AMB} = -40°C to +125°C, unless otherwise noted. Typical values are at V_{VS} = 12.0V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

4.1 Power Supply and References; pins VS, GND

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Current consumption in SBC mode SLEEP [1)]	SBC mode SLEEP, $V_S = V_{LIN} = V_{WK}$ = 13.5V, I_{VDD1}= 0mA, I_{VDD2}= 0mA, T_J<40°C, Booster is off All wake up sources enabled	$I_{VS,SLEEP}$		45	110	µA
1a	Current consumption in SBC mode SLEEP [1)]	SBC mode SLEEP, $V_S = V_{LIN} = V_{WK}$ = 13.5V, I_{VDD1}= 0mA, I_{VDD2}= 0mA, T_J>40°C, Booster is off All wake up sources enabled	$I_{VS,SLEEP,40}$		65	150	µA
2	Current share for CAN wake up capability in SBC mode SLEEP	V_S = 13.5V Not production tested	$I_{VS,CAN,SLEEP}$		5	10	µA
3	Current share for LIN wake up capability in SBC mode SLEEP	V_S = 13.5V Not production tested	$I_{VS,LIN,SLEEP}$		2	5	µA

Table 1: DC Characteristics SLEEP

1) not production tested

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Current consumption in SBC mode STOP without booster	SBC mode STOP, V_{VS} = V_{LIN} = V_{WK} = 13.5V, I_{VDD1}= 0mA, CAN off, LIN off, VDD2 off, All wake up sources enabled, T_J>40°	$I_{VS,STB,T<=125℃}$		100	170	µA
1a	Current consumption in SBC mode STOP without booster	SBC mode STOP, V_{VS} = V_{LIN} = V_{WK} = 13.5V, I_{VDD1}= 0mA, CAN off, LIN off, VDD2 off, All wake up sources enabled, T_J<40°	$I_{VS,STB,T<=40℃}$		85	140	µA
2	Additional current if **VDD2** has load	V_{VS} = 13.5V, I_{VDD2} = -40mA	$I_{VS,VDD2}$		0.1*I_{VDD2}		mA
3	Current consumption of VDD2 voltage regulator in case of low load of 0.2mA [1)]	V_{VS} = 13.5V, I_{VDD2} = -0.2mA	$I_{VS,VDD2,0.2mA}$		1		mA
4	Additional current in SBC mode STOP if cyclic wake up enabled [1)]	STOP Mode, V_{VS} = V_{LIN} = V_{WK} = 13.5V, Cyclic wake up enabled	$I_{VS,STB,CYCLIC}$		10		µA

Table 2: DC Characteristics STOP

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	NORMAL mode current consumption		$I_{VS,NOM}$		150	400	µA
2	Current consumption in active mode for all LINs not production tested	LIN dominant	$I_{VS,LIN,ACT,DOM}$		1.5	3	mA
3	Current consumption in active mode for all LINs	LIN recessive	$I_{VS,LIN,ACT,REC}$		0.25	0.5	mA
4	Current consumption in active mode for CAN	CAN recessive	$I_{VDDCAN,CAN,ACT,REC}$		1	3	mA
5	Current consumption in active mode for CAN not production tested	CAN dominant	$I_{VDDCAN,CAN,ACT,DOM}$		40	105	mA

Table 3: DC Characteristics NORMAL

1) not production tested

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Power on threshold according to pin **VS**		$V_{VS,PU}$	4		5	V
2	Power down threshold according to pin **VS**		$V_{VS,PD}$	2.0		2.5	V

Table 4: DC Characteristics POR

4.1.1 Internal Time Base

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Internal time base, started automatically on demand. Most times specified are derived from this internal time base directly or by using prescalers.		t_{OSC}	0.875		1.125	µs

Table 5: AC Characteristics

4.2 SBC Operating Modes

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	time out in SBC states INIT and RESTART		$t_{TO,INIT}$	230	256	290	ms
2	time out in SBC states INIT and RESTART for VDD1 start up	VS rises above $V_{ON-OFF,VS}$ in before and not fallen below $V_{ON-OFF\_f,VS}$	$t_{TO,VDD1}$	1.4	1.5	1.8	s
3	duration for changes between SBC states	detection of vaild state change condition	t_{MODE_CHANGE}		8		µs
4	VS voltage threshold to be exceeded in order to start timeout $t_{TO,VDD1}$ 1)		$V_{ON-OFF,VS}$	6.3	6.6	6.9	V
5	VS voltage threshold to be underflow in order to deactivate timeout $t_{TO,VDD1}$ 1)		$V_{ON-OFF\_f,VS}$	5.75	6.05	6.35	V

Table 6: AC Characteristics

1) Hysteresis is designed to 550mV, Not production tested

VDD1 current observation in STOP mode

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Timeout for whole system to enter STOP mode and therefore to decrease current consumption	SPI command for STOP mode sent	t_{TRAN_STOP}	2.3	2.6	3.2	ms
2	Threshold for VDD1 observation, 5V system. Upper limit ensures a safe voltage difference to VDD1 of 50mV using production test data for each particular IC.	SBC mode STOP	$k1_{VDD1,5V}$	4.625		V_{VDD1} - 50mV	V
3	Minimum time VDD1 needs to stay above $k1_{VDD1}$ After this time DCDC is switched on for $t_{ON\_REG,STOP}$ in order to recharge VDD1	VDD1_CFG[7:6]= 0h	$t1_0$	4.7		6.4	ms
4	Minimum time VDD1 needs to stay above $k1_{VDD1}$ After this time DCDC is switched on for $t_{ON\_REG,STOP\ P}$ in order to recharge VDD1	VDD1_CFG[7:6]= 1h (default)	$t1_1$	9.7		12.4	ms
5	Minimum time VDD1 needs to stay above $k1_{VDD1}$ After this time DCDC is switched on for $t_{ON\_REG,STOP}$ in order to recharge VDD1	VDD1_CFG[7:6]= 2h	$t1_2$	19.5		24.5	ms
6	Minimum time VDD1 needs to stay above $k1_{VDD1}$ After this time DCDC is switched on for $t_{ON\_REG,STOP}$ in order to recharge VDD1	VDD1_CFG[7:6]= 3h	$t1_3$	39.5		48.6	ms
7	On time of DCDC during regular recharge phase	STOP mode	$t_{ON\_REG,STOP}$	110		160	µs
8	Internal delay of DCDC after switching on request		$t_{DEL,ON}$	-	10	25	µs

Table 7: Characteristics

4.2.1 Configuration for transition behaviour to states FAILSAFE or RESTART

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Pull down resistance active during determination phase for SBC_CFG.CFG	SBC state INIT	$R_{INTN,SBC\_CFG.CFG,PD}$	80	105	150	kΩ
2	Voltage level for detecting logic level low at **INTN**	SBC state INIT	$V_{INTN,SBC\_CFG,L}$			0.7	V
3	Voltage level for detecting logic level high at **INTN**	SBC state INIT	$V_{INTN,SBC\_CFG,H}$	2.6			V

Table 8: DC Characteristics

Software Development function; pin SWDM

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Voltage to be applied to pin **SWDM** in order to enable software development function		$V_{ENABLE,SWDM}$	0.7			VDD1
2	Pull down resistance		$R_{PD,SWDM}$	80	120	200	kΩ

Table 9: DC Characteristics

Over temperature behaviour

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	CAN over temperature detected	CAN enabled	$T_{OT,CAN}$	150			°C
2	LIN over temperature detected. Each LIN has its own sensor.	LIN enabled	$T_{OT,LIN}$	150			°C
3	VDD1 over temperature detected [1)]	VDD1 enabled	$T_{OT,VDD1}$	150	165		°C
4	VDD1 over temperature detection hysteresis [1)]	VDD1 enabled	$T_{OT,VDD1,HYST}$		40		°C
5	VDD2 over temperature warning detected	VDD2 enabled	$T_{OT,VDD2,WARN}$	120			°C
6	Temperature difference between failure and warning threshold	VDD2 enabled	$T_{OT,VDD2,FAIL\ to\ WARN}$	10			°C
7	VDD2 over temperature detected	VDD2 enabled	$T_{OT,VDD2,FAIL}$	140		180	°C
8	Over temperature for aux. internal structures detected	System in state NORMAL	$T_{OT,INT}$	140			°C
9	Over temperature detection hys-teresis, valid for all sensors except otherwise stated [1)]	Temperature sensor enabled	$T_{OT,HYST}$		20		°C

Table 10: OT Characteristics

1) Not production tested

SPI communication; pins SCK, SDI, SDO, CSN

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	High level input voltage		$V_{CSN,INH}$	0.7			VDD1
2	Low level input voltage		$V_{CSN,INL}$			0.3	VDD1
3	High level input current	$V_{CSN} = V_{VDD1}$	$I_{CSN,LEAK}$	-1	0	1	µA
4	Pull up resistor	$V_{CSN} = 0V$	$R_{CSN,PU}$		120		kΩ
5	High level input voltage		$V_{SCK,INH}$	0.7			VDD1
6	Low level input voltage		$V_{SCK,INL}$			0.3	VDD1
7	Pull down resistor	$V_{SCK} = V_{VDD1}$	$R_{SCK,PD}$		120		kΩ
8	High level input voltage		$V_{SDI,INH}$	0.7			VDD1
9	Low level input voltage		$V_{SDI,INL}$			0.3	VDD1
10	Low level output voltage	$I_{SDO} = 1mA$	$V_{SDO,OUTL}$			0.4	V
11	High level output voltage	$I_{SDO} = -1mA$	$V_{SDO,OUTH}$	V_{VDD1} - 0.4			V

Table 11: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Serial clock cycle **(1)**	SCK	t_{SCYC}	125			ns
2	SCK "H" pulse width **(1)**	SCK	t_{SHW}	50			ns
3	SCK "L" pulse width **(1)**	SCK	t_{SLW}	50			ns
4	data setup time (WR) **(1)**	SDI	t_{SDS}	50			ns
5	data hold time **(1)**	SDI	t_{SDH}	50			ns
6	access time **(1)**	SDO	t_{ACC}			50	ns
7	output enable time **(1)**	SDO	t_{OE}			50	ns
8	output disable time **(1)**	SDO	t_{OD}			50	ns
9	SCK-CSN **(1)**	CSN	t_{SCC}	50			ns
10	CSN "H" pulse **(1)** Minimum time between two consecutive SPI accesses	CSN	t_{CHW}	5			us
11	CSN-SCK time **(1)**	CSN	t_{CSS}	125			ns
12	output disable time **(1)**	CSN	t_{CSH}	120			ns

Table 12: AC Characteristics

(1) not production tested

4.3 Watchdog; pin RSTN

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Minimum watchdog time base important for safe trigger area		$t_{WD,PER,MIN}$	0.85			$t_{WD,PER}$
2	Maximum watchdog time base important for safe trigger area		$t_{WD,PER,MAX}$			1.15	$t_{WD,PER}$
3	First open window	open window after **RSTN** is released	$t_{WD,FOW}$	230		290	ms
4	Watchdog reset time		$t_{WD,RSTN}$	450		650	µs

Table 13: AC Characteristics

4.3.1 External Reset / Reset clamping

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	output low level	I_{RSTN}= 1mA V_{VDD1} > 3V	$V_{RSTN,OUTL}$			0.4	V
2	internal pull up resistor	V_{RSTN} = 0V	$R_{RSTN,PU}$	22	32	42	kΩ
3	Voltage level for detecting low at **RSTN**		$V_{RSTN,INL}$			0.7	V
4	Voltage level for detecting high at **RSTN**		$V_{RSTN,INH}$	2.6			V

Table 14: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	debounce time for external applied reset		$t_{RSTN,DEB}$		4		ms
2	time out for short detection to **VDD1**		$t_{RSTN,TO,VDD}$		16		ms
3	time out for short detection to **GND**, can only be detected after $t_{WD,RSTN}$ or $t_{VDD1,RSTN}$		$t_{WDRSTN,TO,GND}$		16		ms

Table 15: AC Characteristics

4.4 Local wake up; pin WK

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Threshold of local wake up, V_{WK} rising	V_{WK} rising	$V_{WK,TH,LH}$	0.6		0.8	VS
2	Threshold of local wake up, V_{WK} falling	V_{WK} falling	$V_{WK,TH,HL}$	0.5		0.7	VS
3	Pull up current	V_{WK} > V_{WK,TH,LH_max} VS - V_{WK} > 1V	$I_{WK,PU}$	-100		-10	µA
4	Pull down current	V_{WK} < V_{WK,TH,HL_min} V_{WK} > 1V	I_{WK_PD}	10		100	µA
5	Leakage current	VS = 12V, V_{WK} = 0V or V_{WK} = V_{VS}	I_{WK_LEAK}	-2		+2	µA

Table 16: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Local wake up debounce time	Threshold crossing transition detected	$t_{WK,DEB}$	20		30	µs

Table 17: AC Characteristics

4.5 LIN Transceiver; pins LIN1 to LIN4, TXDLIN1 to TXDLIN4, RXDLIN1 to RXDLIN4, GND-LIN

4.5.1 Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	functional range LIN transceiver		$V_{LIN,VS}$	7	-	18	V
2	recessive output voltage	**TXDLINx** = 1	$V_{LIN,REC}$	V_{VS} -1V	-	V_{VS}	-
3	dominant output voltage	**TXD** = 0, V_{VS} = 7.0V, R_{LIN} = 0.5kΩ to V_{VS}	$V_{LIN,DOM}$	-	-	1.2	V
4	dominant output voltage	**TXDLINx** = 0, V_{VS} = 18V, R_{LIN} = 0.5kΩ to V_{VS}	$V_{LIN,DOM1}$	-	-	2.0	V
5	receiver dominant level		$V_{LIN,THDOM}$	-	-	0.4	VS
6	receiver recessive level		$V_{LIN,THREC}$	0.6	-	-	VS
7	LIN bus center voltage	$V_{LINx,BUSCNT}$ = ($V_{LINx,THDOM}$ + $V_{LINx,THREC}$) / 2	$V_{LIN,BUSCNT}$	0.475	-	0.525	VS
8	receiver hysteresis	$V_{LINx,THREC}$ - $V_{LIN,THDOM}$	$V_{LIN,HYS}$	0.02	-	0.175	VS
9	output current limitation	V_{LINx} = $V_{VS,MAX}$ = 18V	$I_{LIN,LIM}$	40	-	200	mA
10	pull up resistance		$R_{LIN,SLAVE}$	20	33	60	kΩ
11	leakage current flowing into pin **LIN**	transmitter passive, 7V < V_{VS} < 18V, 7V < V_{LINx} < 18V, V_{LINx} > V_{VS}	$I_{LIN,BUSREC}$	-	-	20	µA
12	pull up current flowing out of pin **LIN**	transmitter passive, 7V < V_{VS} < 18V, V_{LINx} = 0V	$I_{LIN,BUSDOM}$	-1	-	-	mA
13	leakage current, ground disconnected (**GND** device = **VS**)	V_{VS} = 13.5V, 0V < V_{LINx} < 18V	$I_{LIN,NOGND}$	-1	-	0.1	mA
14	leakage current, supply disconnected	V_{VS} = 0V, 0V < V_{LINx} < 18V	I_{LIN}	-	-	20	µA
15	leakage current, supply disconnected, T_J = 85°C, not production tested	V_{VS} = 0V, 0V < V_{LINx} < 18V	$I_{LIN,85}$	-	-	15	µA
16	clamping voltage, not production tested	V_{VS} = 0V, I_{LINx} = 1mA	$V_{LIN,CLAMP}$	40		-	V

Table 18: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	input capacitance, not production tested!	7V < V_{VS} < 18V	$C_{LIN,PIN}$	-	-	30	pF
2a	receive propagation delay		$t_{RXD,PDR}$,$t_{RXD,PDF}$	-	-	6	µs
2b	receive propagation delay in FLASH mode[1)]		$t_{RXD,PDR,FLASH}$, $t_{RXD,PDF,FLASH}$	-	-	2.5	µs
3	receive propagation delay sym-metry		$t_{RXD,SYM}$	-2	-	2	µs
4	wake up debounce time		$t_{LIN,WU}$	70		150	µs
5	Duty cycle 1 [1)]	$V_{LIN,THREC}$(max) = 0.744*V_{VS}, $V_{LIN,THDOM}$(max) = 0.581*V_{VS}, V_{VS} = 7-18V, t_{BIT} = 50us, $D_{LIN,1}$ = t_{BUSREC}(min)/(2*t_{BIT})	$D_{LIN,1}$	0.396	-	-	-
6	Duty cycle 2 [1)]	$V_{LIN,THREC}$(min) = 0.422*V_{VS}, $V_{LIN,THDOM}$(min) = 0.284*V_{VS}, V_{VS} = 7-18V, t_{BIT} = 50us, $D_{LIN,2}$ = $t_{BUS-REC}$(max)/(2*t_{BIT})	$D_{LIN,2}$	-	-	0.581	-
7	Duty cycle 3 [1)]	$V_{,LIN,THREC}$(max) = 0.778*V_{VS}, $V_{LIN,THDOM}$(max) = 0.616*V_{VS}, V_{VS} = 7-18V, t_{BIT} = 96us, $D_{LIN,3}$ = t_{BUSREC}(min)/(2*t_{BIT})	$D_{LIN,3}$	0.417	-	-	-
8	Duty cycle 4 [1)]	$V_{LIN,THREC}$(min) = 0.389*V_{VS}, $V_{LIN,THDOM}$(min) = 0.251*V_{VS}, V_{VS} = 7-18V, t_{BIT} = 96us, $D_{LIN,4}$ = $t_{BUS-REC}$(max)/(2*t_{BIT})	$D_{LIN,4}$	-	-	0.590	-
9	receive data baud rate [2)]	flash mode, V_{VS} = 13V	$B_{LIN,RXD}$			250	kBd/s
10	transmit data baud rate [2)]	flash mode,C_{LIN} = 200PF, R_{LIN} = 0.5kΩ V_{VS} = 13V	$B_{LIN,TXD}$			125	kBd/s

Table 19: AC Characteristics

1) Bus load conditions (C_{LIN},R_{LIN}): 1nF, 1kΩ or 6.8nF, 660Ω or 10nF, 500Ω

2) Not production tested

4.5.2 LIN TXD/RXD

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	output low level range	$I_{RXD,LINx}$ = 1mA	$V_{RXD,LINx,OUTL}$	-	-	0.4	V
2	output high level range	$I_{RXD,LINx}$ = -1mA	$V_{RXD,LINx,OUTH}$	V_{VDD1}-0.4	-	-	V
3	input low voltage range		$V_{TXD,LINx,INL}$	-	-	0.3	VDD1
4	input high voltage range		$V_{TXD,LINx,INH}$	0.7	-	-	VDD1
5	Internal TXD pull up resistor	$V_{TXD,LINx}$ = 0V	$R_{TXD,LINx,PU}$	80	110	150	kΩ

Table 20: DC Characteristics

4.5.3 LIN Failure detection and recovery

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	time out for txd dominant clamping failure		$t_{LIN,TXD,DOM}$	8.5		12.5	ms
2	time out for LIN dominant clamping failure		$t_{LIN,BUS,DOM}$	8.5		12.5	ms

Table 21: AC Characteristics

HS-CAN Transceiver; pins CANH, CANL, RXDCAN, TXDCAN, VDDCAN

(V_{VS} = 5.5V to 28V, T_{AMB} = -40°C to +125°C, V_{CAN}=-12V to +12V unless otherwise noted. Typical values are at V_{VS} = 12.0V and T_{AMB} = +25°C. Positive currents flow into the device pins.)

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	**CANH** dominant output voltage	V_{TXDCAN} = 0V R_L = 50Ω to 65Ω	$V_{DOM\_OUT\_H}$	3.0		4.5	V
2	**CANL** dominant output voltage	V_{TXDCAN} = 0V R_L = 50Ω to 65Ω	$V_{DOM\_OUT\_L}$	0.5		2.0	V
3	Matching of dominant output voltages (V_{VDDCAN} - (V_{CANH} + V_{CANL}))	V_{TXDCAN} = 0V R_L = 50Ω to 65Ω	$V_{DOM\_OUT\_MATCH}$	-400		400	mV
4	Differential bus dominant output voltages (V_{CANH}-V_{CANL})	V_{TXDCAN} = 0V R_L = 50Ω to 65Ω	$V_{DIFF\_OUT\_DOM}$	1.5		3.0	V
5	Recessive output voltage on **CANH** and **CANL**	V_{TXDCAN} = V_{VDD1} CAN NORMAL and LISTEN mode	V_{REC_OUT}	2.0	V_{VDDCAN}/ 2	3.0	V
6	Differential receiver threshold voltage	CAN NORMAL and LISTEN mode	V_{DIFF_TH}	500	700	900	mV
7	Differential receiver threshold voltage, CAN off and wake up detection capability enabled	CAN off, wakeable	$V_{DIFF\_TH\_OFF}$	400		1150	mV
8	Differential receiver hysteresis voltage	CAN NORMAL and LISTEN mode	V_{DIFF_HYST}		60		mV
9	Differential bus recessive output voltages (V_{CANH} - V_{CANL})	CAN recessive, no load	$V_{REC\_OUT\_OFF}$	-100		50	mV
9a	Recessive output voltage at CANH and CANL, low power mode	CAN recessive, no load	$V_{REC,LP}$	-100		100	mV
10	Short circuit output current on CANL	V_{TXDCAN} = 0V V_{CANL} = 40V	$I_{SC\_OUT\_CANL}$	40		100	mA
11	Short circuit output current on **CANH**	V_{TXDCAN} = 0V V_{CANH} = -5V	$I_{SC\_OUT\_CANH}$	-100		-40	mA
12	Recessive bus current	V_{TXDCAN} = V_{VDD1} -27V < $V_{CANH/L}$ < 32V	I_{REC_OUT}	-5		5	mA
13	Input leakage current on **CANL** and **CANH**	VDD connected to GND with R = 0Ω and R = 47kΩ V_{CANH} = V_{CANL} = 5V	I_{LEAK_IN}	-10		10	µA
14	Common mode input resistance		R_{I_COM}	15		35	kΩ
15	Differential input resistance		R_{I_DIF}	30		70	kΩ
15a	Common mode input capacitance not production tested	V_{TXDCAN} = VDD1	C_{I_COM}		20		pF
15b	Differential input capacitance not production tested	V_{TXDCAN} = VDD1	C_{I_DIF}		10		pF
15c	Internal R_{in} resistor matching of **CANH** and **CANL**		$R_{in\_matching}$	-3		3	%

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
16	Differential bus recessive output voltages (V_{CANH} - V_{CANL})	V_{TXDCAN} = VDD1	$V_{DIFF\_OUT\_REC\_LOAD}$	-5		5	mV
17	**VDDCAN** monitor threshold	HS-CAN enabled	$V_{VDDCAN,UV}$	4.2		4.6	V
18	**VDDCAN** monitor threshold hysteresis	HS-CAN enabled	$V_{VDDCAN,UV,HYST}$		100		mV
19	CANH / CANL common mode voltage range		V_{CAN}	-12		12	V

Table 22: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Data rate range to be transmitted and received	CAN NORMAL or LISTEN mode	DR_{CAN}	40		1000	kBit/s
2	Delay **TXDCAN** to bus dominant not production tested	CAN NORMAL mode	$t_{CAN,D\_TXD\_BUS(dom)}$	25		110	ns
3	Delay **TXDCAN** to bus recessive not production tested	CAN NORMAL mode	$t_{CAN,D\_TXD\_BUS(rec)}$	10		95	ns
4	Delay bus to **RXDCAN** dominant not production tested	CAN NORMAL or LISTEN mode	$t_{CAN,D\_BUS\_RXD(dom)}$	15		115	ns
5	Delay bus to **RXDCAN** recessive not production tested	CAN NORMAL or LISTEN mode	$t_{CAN,D\_BUS\_RXD(rec)}$	35		160	ns
6	Propagation delay **TXDCAN** to **RXDCAN**	CAN NORMAL mode	t_{CAN,PD_TXD_RXD}	40		255	ns
7	Dominant time for wake up via bus	CAN off, wake up capability enabled, VS = 12V	$t_{CAN,WAKE\_BUS\_DOM}$	0.75		5	µs
8	Recessive time for wake up via bus	CAN off, wake up capability enabled, VS = 12V	$t_{CAN,WAKE\_BUS\_REC}$	0.75		5	µs
9	wake up time out	CAN_CFG.RC = 0, CAN_CFG.WU = 1	$t_{CAN,WAKE2}$	0.5		2	ms
10	CAN activation time	CAN_CFG.RC = 1	$t_{CAN,ACTIVE}$			50	µs

Table 23: AC Characteristics

4.5.4 TXDCAN and RXDCAN

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	output low level range	I_{RXDCAN} = 1mA	$V_{RXD,CAN,OUTL}$	-	-	0.4	V
2	output high level range	I_{RXDCAN} = -1mA	$V_{RXD,CAN,OUTH}$	V_{VDD1}-0.4	-	-	V
3	input low voltage range		$V_{TXD,CAN,INL}$	-	-	0.3	VDD1
4	input high voltage range		$V_{TXD,CAN,INH}$	0.7	-	-	VDD1
5	Internal **TXDCAN** pull up resistor	V_{TXDCAN} = 0V	$R_{TXD,CAN,PU}$	80	110	150	kΩ

Table 24: DC Characteristics

4.5.5 CAN Failure detection and recovery

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	time out for TXD dominant clamping failure		$t_{CAN,TXD,DOM}$	1.4		1.9	ms
2	time out for BUS dominant clamping failure		$t_{CAN,BUS,DOM}$	1.4		1.9	ms
3	duration of bus dominant or recessive time for CAN bus failure detection		$t_{BUS,FAIL}$		6		µs

Table 25: AC Characteristics

4.6 Limp Home support; pin FSON

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	output low level	I_{FSON} = 1mA $V_{VS} > V_{VS,PD}$	$V_{FSON,OUTL}$			0.4	V

Table 26: DC characteristics

4.7 Interrupt; pin INTN

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	output low level	I_{INTN} = 1mA $V_{VDD1} > 3V$	$V_{INTN,OUTL}$			0.4	V
2	pull up resistor	V_{INTN} = 0V	$R_{INTN,PU}$	80	105	150	kΩ

Table 27: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Calculation time for interrupt related state change condition detected	Interrupt state change condition detected	$t_{INTN,SETUP}$		8		t_{OSC}

Table 28: AC Characteristics

4.8 DCDC Buck converter; pins VIN, VDD1, VDD1SENSE, LXT, PGND

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	**VDD1** output voltage if enabled, E521.02..04, E521.12..14	I_{VDD1} = -500mA, C_{VDD1} > 22µF, ESR < 120mΩ, V_{VIN} > 5.5V	$V_{VDD1,5V}$	4.9		5.1	V
2	Quiescent current consumption of DCDC buck converter in case of switched off, e.g. in SBC mode SLEEP	V_{VIN} = 13.5V DCDC off	$I_{VIN,DCDC\_OFF}$		9	20	µA
3	Quiescent current consumption of DCDC buck converter in case of switched on, e.g. in SBC mode NORMAL	V_{VIN} = 13.5V DCDC on Duty cycle = 0%	$I_{VIN,DCDC\_ON}$		160		µA
4	reset threshold 1 for VDD1 E521.02..04, E521.12..14 [1)]	VDD1_CFG.THR_1:THR_0 = 0h, VDD1 falling	$V_{TH1,VDD1,RSTN}$	4.4		4.6	V
5	reset release threshold 1 for VDD1 E521.02..04, E521.12..14 [1)]	VDD1_CFG.THR_1:THR_0 = 0h, VDD1 rising	$V_{TH1,VDD1\_r,RSTN}$	4.6		4.9	V
6	reset threshold 2 for VDD1 E521.02..04, E521.12..14 [1)]	VDD1_CFG.THR_1:THR_0 = 1h, VDD1 falling	$V_{TH2,VDD1,RSTN}$	3.8		4	V
7	reset release threshold 2 for VDD1 E521.02..04, E521.12..14 [1)]	VDD1_CFG.THR_1:THR_0 = 1h, VDD1 rising	$V_{TH2,VDD1\_r,RSTN}$	4.0		4.25	V
8	reset threshold 3 for VDD1 E521.02..04, E521.12..14 [1)]	VDD1_CFG.THR_1:THR_0 = 2h, VDD1 falling	$V_{TH3,VDD1,RSTN}$	3.4		3.6	V
9	reset release threshold 3 for VDD1 E521.02..04, E521.12..14 [1)]	VDD1_CFG.THR_1:THR_0 = 2h, VDD1 rising	$V_{TH3,VDD1\_r,RSTN}$	3.6		3.85	V
10	reset threshold 4 for VDD1 E521.02..04, E521.12..14 [1)]	VDD1_CFG.THR_1:THR_0 = 3h, VDD1 falling, default selection	$V_{TH4,VDD1,RSTN}$	3		3.2	V
11	reset release threshold 4 for VDD1 E521.02..04, E521.12..14 [1)]	VDD1_CFG.THR_1:THR_0 = 3h, VDD1 rising	$V_{TH4,VDD1\_r,RSTN}$	3.2		3.45	V
12	LXT internal over current protection limit	V_{VIN} > 5.5V	I_{LXT}	650	800	1100	mA

[1)] Hysteresis of reset thresholds is designed to > 150mV in 5V system

Table 29: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	reset delay time after release of VDD1 reset		$t_{RSTN,VDD1}$	4.5		6.5	ms
2	VDD1 under voltage debounce time		$t_{DEB,VDD1}$		10	50	µs
3	reset reaction time in case of under voltage condition		$t_{RR,VDD1,RSTN}$		14	20	µs

Table 30: AC Characteristics

4.8.1 Pulse Frequency Modulated (PFM) Converter

PFM Control Logic

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Switch Minimum ON Time	No over current detected	$T_{ON,MIN}$		260		ns
2	Minimum ON Time	Over current detected	$T_{ON,OC}$		100		ns
3	Minimum OFF time without over current		$T_{OFF,MIN,NOM}$		520		ns
4	Nominal minimum OFF time after over current detection		$T_{OFF,OC,NOM}$		1330		ns
5	Extended minimum OFF time after over currrent detection		$T_{OFF,OC,EXT}$		2450		ns
6	Operation frequency	depending on ratio V_{VIN}/V_{DD1} and load conditions	F_{OP}	0		1.7	MHz
7	Peak Operation Frequency		$F_{OP,MAX}$	0.9	1.3	1.7	MHz

Table 31: AC characteristics

Low drop regulator; pins VDD2, ENVDD2

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Parameter removed						
2	output voltage range	VDD2 enabled, $6V < V_{VS} < 28V$, $I_{VDD2} > -100mA$	$V_{VDD2,100mA}$	4.9	5.0	5.1	V
3	output current limitation	$V_{VDD2} = 0V$, $V_{VS} = 28V$	$I_{VDD2,LIM}$	-220		-110	mA
4	information only, RDS of regulator for $V_{VS} = 5.5V$	VDD2 enabled, Determined for $V_{VS} = 5.5V$ Not production tested	$RDS_{VDD2,VS=5.5V}$			12	Ω
5	information only, RDS of regulator for $V_{VS} = 5.0V$	VDD2 enabled, Determined for $V_{VS} = 5.0V$ Not production tested	$RDS_{VDD2,VS=5.0V}$			13	Ω
6	information only, RDS of regulator for $V_{VS} = 4.5V$	VDD2 enabled, Determined for $V_{VS} = 4.5V$ Not production tested	$RDS_{VDD2,VS=4.5V}$			15	Ω
7	information only, RDS of regulator for $V_{VS} = 4.0V$	VDD2 enabled, Determined for $V_{VS} = 4.0V$ Not production tested	$RDS_{VDD2,VS=4.0V}$			17	Ω
8	information only, RDS of regulator for $V_{VS} = 3.5V$	VDD2 enabled, Determined for $V_{VS} = 3.5V$ Not production tested	$RDS_{VDD2,VS=3.5V}$			21	Ω
9	under voltage threshold falling	VDD2 enabled	$V_{UV,THR}$	4.5		4.8	V
10	under voltage hysteresis	VDD2 enabled	$V_{UV,HYS}$		100		mV
11	threshold of **ENVDD2** rising	V_{ENVDD2} rising	$V_{ENVDD2,LH}$	0.6		0.8	VS
12	threshold of **ENVDD2** falling	V_{ENVDD2} falling	$V_{ENVDD2,HL}$	0.5		0.7	VS

Table 32: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	under voltage debounce time		$t_{DEB,UV}$	150		280	µs

Table 33: AC Characteristics

4.9 DCDC Boost converter; pins MDRV, ISEN, PGND2

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	VS activation and output voltage E521.12, .13, .14 only	V_{VDD1} > tbd.	V_{BOOST}	6.0	6.5	7.0	V
2	Current sense threshold E521.12, .13, .14 only		V_{ISEN}	85	100	110	mV
3	Current sense input current E521.12, .13, .14 only	Booster disabled	I_{ISEN}	-1		1	µA
4	Minimum Booster input voltage to guarantee defined booster output voltage E521.12, .13, .14 only	I_{load_VS} < 600mA	$V_{Booster\_input\_min}$	3.25			V
5	Minimum Booster input voltage to guarantee defined booster output voltage, current limited to lower value of than defined for V_{BAT_min} E521.12, .13, .14 only	I_{load_VS} < tbd.	$V_{Booster\_input\_min\_2}$	2.5			V
6	Internal parasitic Resistance of the Booster-inductance E521.12, .13, .14 only		RDC_L_{BOOST}			30	mΩ
7	Pullup current at ISENSE-Pin during booster is on E521.12, .13, .14 only	Booster enabled	R_{ISENSE}		2	5	µA

Table 34: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Minimum switch off-time		$T_{OFFMIN4}$		0.47		µs
2	Maximum switch on-time		T_{ONMAX4}		8.4		µs
3	Minimum switch on-time		T_{ONMIN4}		150		ns

Table 35: AC Characteristics

5 Functional Description

5.1 Power Supply and References; pins VS, GND

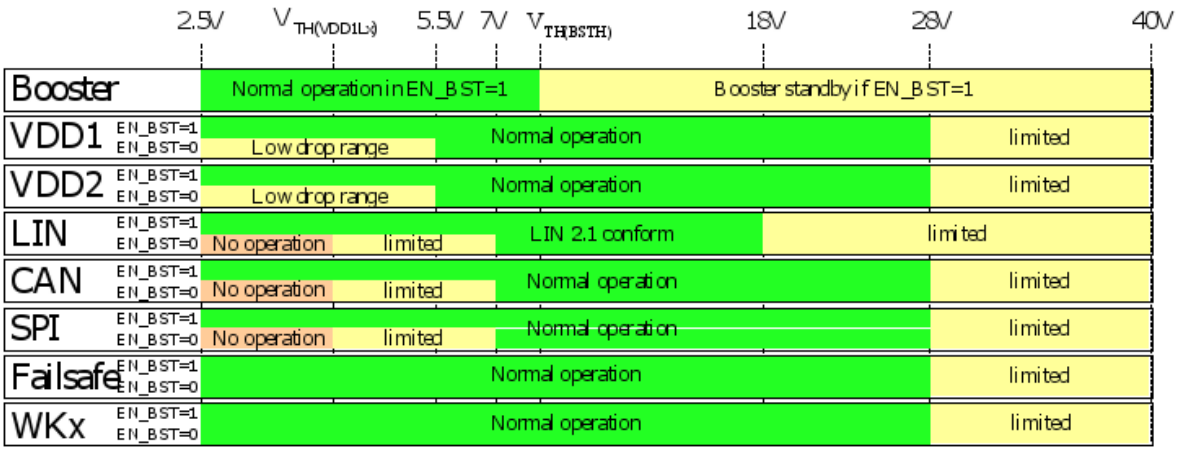


Fig. 1: Operating Range Limitations

5.1.1 Internal Time Base

Most times specified are derived from internal 1µs time base e.g. directly or by using prescalers based on this time base.

5.2 SBC Operating Modes

The device provides the following states:

- OFF
- INIT
- NORMAL
- STOP
- SLEEP
- RESTART
- FAILSAFE

Transition between states is performed at the latest t_{STATE_CHANGE} after valid condition detected.

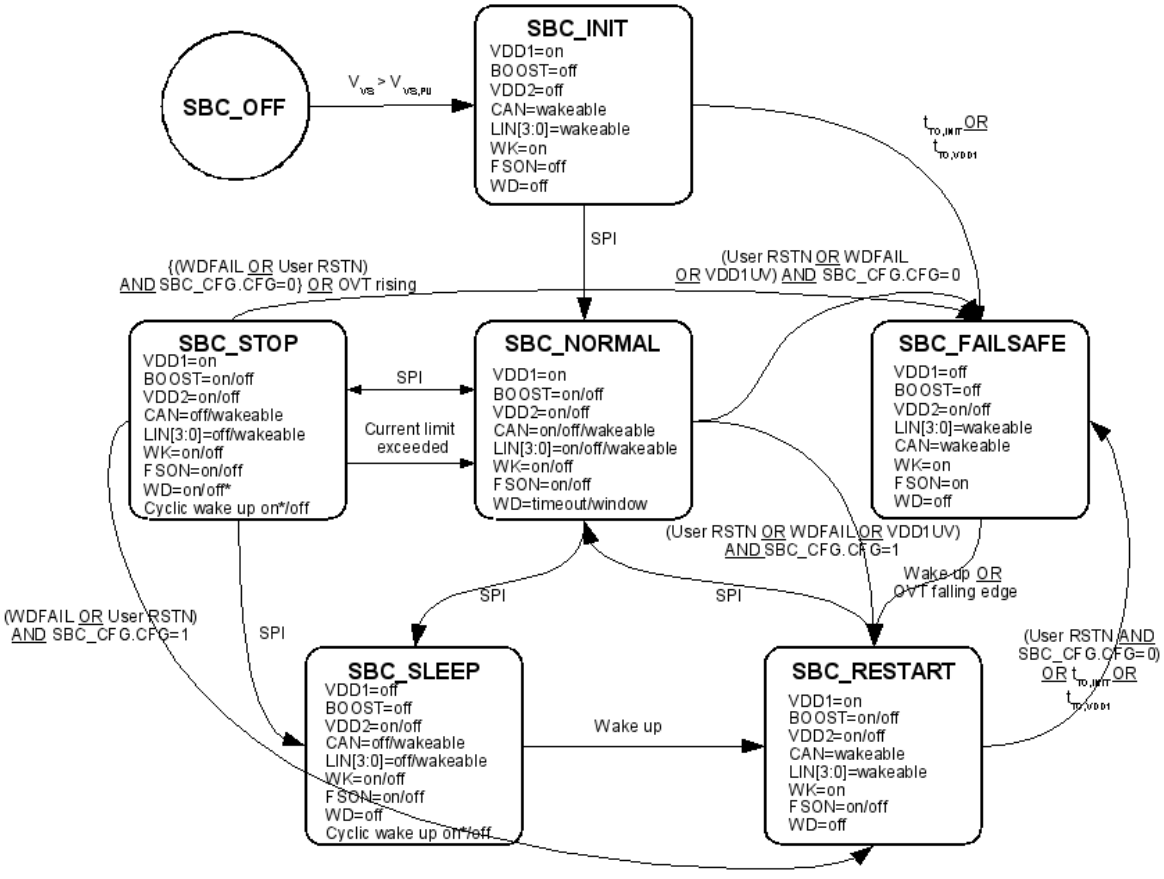


Fig. 2: SBC State Diagram

*) Watchdog and cyclic wake up use one timer. It is possible to use one at the same time only. A change between cyclic wake up and watchdog does not reset timer.

Register Name	Address	Description
SBC_CFG	0x01	SBC configuration register.
WU_SRC	0x04	Wake up source register. Wake up source is cleared if register is read via SPI.
SPI_FAIL	0x05	SPI programming failure register. Register is cleared by reading via SPI.
VDD_STAT	0x1A	VDD1, VDD2 and VDDCAN status information.

Table 36: RegisterTable

Register **SBC_CFG** (0x01)

	MSB							LSB
Content	CLAMP	-	BOOST	FSON	CFG	STATE2	STATE1	STATE0
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R/W	R	R/W	R/W	R/W	R/W
Bit Description	**CLAMP** : 1.. External reset shorter than $t_{WDRSTN,TO,GND}$ will not lead to **FSON** set 0.. External reset leads to **FSON** set immediately Info: Bit can be written in register FSON_CFGx. **BOOST** : 1.. Enable booster for low voltage at pin **VS** 0.. Do not enable booster for low voltage at pin **VS** **FSON** : 1.. **FSON** is active 0.. **FSON** is not active **CFG** : SBC state transition in case of watchdog failure 0.. FAILSAFE 1.. RESTART **STATE2 ... STATE0** 000.. OFF 001.. INIT (cannot be set by SPI) 010.. NORMAL 011.. STOP 100.. RESTART 101.. FAILSAFE 110.. SLEEP 111.. reserved							

Table 37: SBC configuration register.

Register **WU_SRC** (0x04)

	MSB							LSB
Content	LIN4	LIN3	LIN2	LIN1	CAN	VDD1	WD	WK
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**LIN4** : 1... wake up from LIN4 detected **LIN3** : 1... wake up from LIN3 detected **LIN2** : 1... wake up from LIN2 detected **LIN1** : 1... wake up from LIN1 detected **CAN** : 1... wake up from CAN detected **VDD1** : 1... wake up in STOP mode due to VDD1 current limitation exceeded **WD** : 1... cyclic wake up in STOP mode **WK** : 1... wake up from local wake up pin WK detected							

Table 38: Wake up source register. Wake up source is cleared if register is read.

Register **SPI_FAIL** (0x05)

	MSB							LSB
Content	LIN4	LIN3	LIN2	LIN1	CAN	-	WD	FSM
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**Register is cleared by reading via SPI** **LIN4** : 1.. LIN4 is reason for interrupt, e.g. configuration of LIN4 in case of not beeing in SBC state NORMAL 0.. LIN4 is not reason for interrupt **LIN3** : 1.. LIN3 is reason for interrupt, e.g. configuration of LIN3 in case of not beeing in SBC state NORMAL 0.. LIN3 is not reason for interrupt **LIN2** : 1.. LIN2 is reason for interrupt, e.g. configuration of LIN2 in case of not beeing in SBC state NORMAL 0.. LIN2 is not reason for interrupt **LIN1** : 1.. LIN1 is reason for interrupt, e.g. configuration of LIN1 in case of not beeing in SBC state NORMAL 0.. LIN1 is not reason for interrupt **CAN** : 1.. CAN is reason for interrupt, e.g. configuration of CAN in case of not beeing in SBC state NORMAL 0.. CAN is not reason for interrupt **WD** : 1.. Watchdog is reason for interrupt, e.g. configuration of WD in case of not beeing in SBC state NORMAL 0.. Watchdog is not reason for interrupt **FSM** : 1.. State machine is reason for interrupt, e.g. trying to change into SBC state SLEEP with pending wake up 0.. State machine is not reason for interrupt							

Table 39: SPI programming failure register.

Register **VDD_STAT** (0x1A)

	MSB							LSB
Content	VDD2 ON	VDD2_EN PIN	VDD2OC	VDD2 UV	-	VDDCAN UV	VDD1 UV	-
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**VDD2 ON** : 1.. Linear voltage regulator **VDD2** enabled 0.. Linear voltage regulator **VDD2** disabled **VDD2_EN PIN** : 1.. **ENVDD2** set to logic level 1 0.. **ENVDD2** set to logic level 0 **VDD2OC** : 1.. **VDD2** over current detected 0.. **VDD2** over current not detected **VDD2 UV** : 1.. **VDD2** under voltage detected 0.. **VDD2** under voltage not detected **VDDCAN UV** : 1.. **VDDCAN** under voltage detected 0.. **VDDCAN** under voltage not detected **VDD1 UV** : 1.. **VDD1** under voltage detected 0.. **VDD1** under voltage not detected							

Table 40: VDD1, VDD2 and VDDCAN status information.

5.2.1 OFF state

The OFF mode is the unsupplied state. This mode is left automatically if $V_{VS} > V_{S,PU}$.
It is entered automatically if $V_{VS} < V_{S,PD}$.

5.2.2 INIT state

The SBC is set to state INIT after $V_{VS,PU}$ is exceeded. The DCDC buck converter VDD1 is switched on. The default reset threshold $V_{TH4,VDD1,RSTN}$ is active. Pin **RSTN** is set to L. After reaching reset threshold reset delay time $t_{RSTN,VDD1}$ is applied. Then pin **RSTN** is set to H.

In case of **VDD1** does not start up beyond its reset level state transition to state FAILSAFE is performed after $t_{TO,VDD1}$. This function helps to prevent higher or even short currents to **VDD1** for longer times.

Transition from SBC state INIT to SBC state NORMAL must be initiated by SPI within $t_{TO,INIT}$. $t_{TO,INIT}$ starts with rising edge of **RSTN**.

The reset output pin **RSTN** is bidirectional and can be overwritten by the external µC. In case of an internal reset extended by an external reset the timeout $t_{WDRSTN,TO,GND}$ becomes active at the end of the internal reset duration. If the timeout is exceeded SBC changes to state FAILSAFE and **FSON** is set.

5.2.3 NORMAL state

State NORMAL is expected to be the main state. All configuration registers are accessable and watchdog is running.

Watchdog, CAN, VDD2, WK, FSON and LINs can be configured.

Low power state STOP and very low power state SLEEP can be entered via SPI.

If a watchdog trigger failure occurs or **RSTN** is overwritten externally or **VDD1** drops below the configurable reset threshold state is changed to FAILSAFE or RESTART depending on configuration of bit SBC_CFG.CFG.

5.2.4 STOP state

LIN and CAN transceivers are off but can be wakeable.

Watchdog cyclic wake up timer can be active. Configuration must be performed in state NORMAL in registers WD_CFG1 and WD_CFG2 prior entering state STOP as described for watchdog configuration change. Occurence of cyclic wake up generates an interrupt.

VDD2 regulator can be active depending on pin **ENVDD2** or bit VDD2_CFG.ON.

If **RSTN** is overwritten externally the state changed to FAILSAFE or RESTART mode depending on configuration of bit SBC_CFG.CFG. Hence the regulator is enabled every $t1_n$ an external reset is detectable only after that time only.

5.2.5 VDD1 current observation in SBC state STOP

A low current consumption is expected in SBC state STOP. To save current DCDC is switched off after an initial time $t_{TRAN,STOP}$. DCDC is enabled periodically for regular recharge phase $t_{ON\_REG,STOP}$ every reload time $t1_n$.

Reload time can be configured in register VDD1_CFG. The undervoltage detection remains active.

In case of current consumption is too high voltage drops below undervoltage threshold $k1_{VDD1}$ and regulator is enabled for $t_{TRAN,STOP}$. If this happens more than once within $t1_n$ state is changed to SBC state NORMAL and an interrupt is generated. Otherwise SBC remains in state STOP.

System behaviour concerning V_{VDD1} strongly depends on value of external capacitor. It is recommended to calculate value of external capacitor with knowledge of overall system STOP state current consumption and adding a safety margin in order to ensure SBC state STOP can be reached and kept.

Accessing register VDD1_CFG is not allowed in SBC state FAILSAFE.

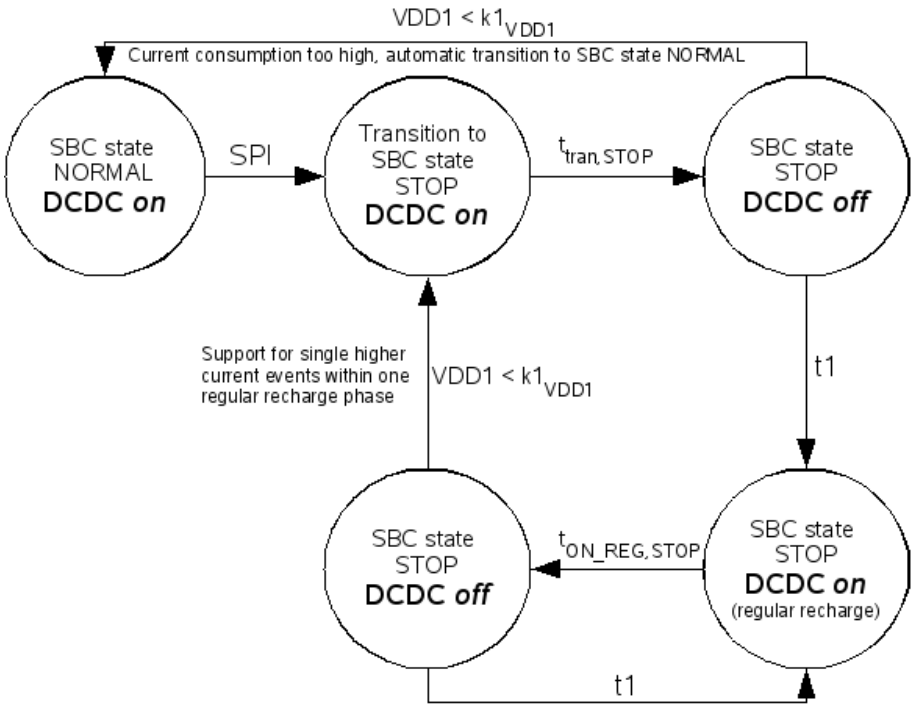


Fig. 3: Transition to and from SBC state STOP with current observation on VDD1

5.2.6 SLEEP state

LIN and CAN transceivers are off but can be wakeable. VDD1 voltage regulator is off and reset signal at **RSTN** is generated.

VDD2 regulator can be active depending on pin **ENVDD2** or bit VDD2_CFG.ON.

A transition to state SLEEP with all wake up sources disabled is prohibited. The transistion is ignored, SPI failure bit is set and an interrupt is generated.

Wake up event causes a transition to state RESTART.

Watchdog can be configured to wake up device in state SLEEP.

5.2.7 RESTART state

State RESTART is an intermediate state being reached in case of failure conditions or wake up from states SLEEP or FAILSAFE.

State can be left to NORMAL using SPI command within limited amount of time $t_{TO,INIT}$. Otherwise state FAILSAFE is entered automatically.

5.2.8 FAILSAFE state

State FAILSAFE is entered in case of failure condition present only. Pin **FSON** is activated automatically. VDD1 regulator is switched off. Pin **RSTN** is set to low.

VDD2 regulator can be active depending on pin **ENVDD2**.

With entering state FAILSAFE all wake up capabilities are enabled. In case of a wake up condition state RESTART is entered.

In case of an overtemperature failure state RESTART is entered when overtemperature condition vanishes.

5.2.9 Configuration for transition behaviour to modes FAILSAFE or RESTART

Transition behaviour in case of failure either to SBC state FAILSAFE or to SBC state RESTART can be setup using external circuitry connected to pin **INTN**.

Setup of behaviour is performed in state INIT at the end of SBC active RSTN time $t_{RSTN,VDD1}$. At this particular point voltage at **INTN** is sensed back. Desired behaviour is stored in register SBC_CFG.CFG.

For setup purposes during time of determination neither internal normal pull up resistor nor internal low side driver are active in **INTN** stage. Instead of an internal pull down resistor is active. There are two possible cases:

1. *External* pull up present: Detect logic level high
2. No *external* pull up present: Detect logic level low
   Diagram Fig. 4 shows principal implementation of **INTN** stage. T_{1N} and T_{1P} are used for normal operation. For setup phase both T_{1N} and T_{1P} are switched off and pull down controlled by T_{2N} is enabled.

Recommendation for selection of external pull up resistance towards VDD1

System with V_{VDD1}=5V: Select value of ≦ 85kΩ, e.g. 68kΩ

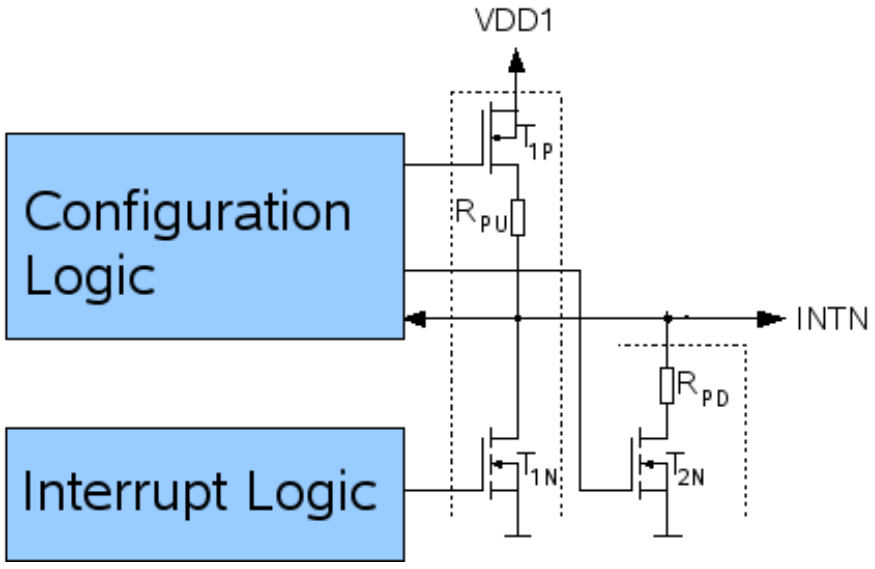


Fig. 4: INTN internal structure with support for setup SBC_CFG.CFG

Implementation of INTN stage for normal operation and setup of SBC_CFG.CFG.

An alternative way to change RESTART/FAILSAFE behaviour in case of a failure is setting bit SBC_CFG.CFG via SPI. But there are some limitations:

1. Bit SBC_CFG.CFG can not be set to L via SPI if an external pull up exists at pin **INTN**.
2. Bit SBC_CFG.CFG can be written in states STOP and NORMAL only.
3. Bit SBC_CFG.CFG is cleared in states RESTART and FAILSAFE.

5.2.10 Software Development function; pin SWDM

High active pin **SWDM** determines activation of software development function. The only way to enable software development function is a high level of pin **SWDM** with internal release of pin **RSTN** in SBC states INIT or RESTART.

In final application pin **SWDM** must be connected to electrical ground.

With software development function enabled following changes apply to system behaviour:

1. no watchdog related reset at pin **RSTN** is generated
2. automatic watchdog related transitions to states FAILSAFE or RESTART are not performed
3. external events at **RSTN** are ignored
4. exceeding of timeout $t_{TO,INIT}$ is ignored

All failures are signaled as usual in SPI status register. All other functional blocks behave as described.

Setting pin **SWDM** to low logic level disables software development function.

5.2.11 Over temperature behaviour

IC implements 8 independent temperature sensors:

1. LIN1
2. LIN2
3. LIN3
4. LIN4
5. HS-CAN
6. VDD2 voltage regulator
7. VDD1 DCDC buck converter
8. Internal aux. structures

In case of over temperature detected in LIN or CAN transceivers corresponding interface is switched off and an interrupt is set.

VDD2 voltage regulator features both warning and over temperature shutdown functionality including interrupt generation.

VDD1 over temperature detection results in an external reset at **RSTN**.

In case of internal auxiliary structures report an over temperature situation system changes to SBC state FAILSAFE. If overtemperature vanishes device will enter SBC state RESTART.

Register Name	Address	Description
OT_STAT	0x1F	Over temperature detection status register.

Table 41: RegisterTable

Register **OT_STAT** (0x1F)

	MSB							LSB
Content	LIN4	LIN3	LIN2	LIN1	CAN	VDD2	VDD1	AUX
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**LIN4** : 1.. LIN4 over temperature detected 0.. LIN4 over temperature not detected **LIN3** : 1.. LIN3 over temperature detected 0.. LIN3 over temperature not detected **LIN2** : 1.. LIN2 over temperature detected 0.. LIN2 over temperature not detected **LIN1** : 1.. LIN1 over temperature detected 0.. LIN1 over temperature not detected **CAN** : 1.. CAN over temperature detected 0.. CAN over temperature not detected **VDD2** : 1.. VDD2 over temperature detected 0.. VDD2 over temperature not detected **VDD1** : 1.. VDD1 over temperature detected 0.. VDD1 over temperature not detected **AUX** : 1.. Over temperature in other internal aux. structures detected 0.. Over temperature in other internal aux. structures not detected							

Table 42: Over temperature detection status register.

5.3 SPI communication; pins SCK, SDI, SDO, CSN

The SPI interface is used for:

- storing-/and reading CAN data-/timing and system configurations
- reading diagnosis register

By setting CSN to low level, the communication can be achieved and by setting to high level leads to disabling the communication (in this case, pin SDO is high impedance). During the transmission data shifts are controlled by the serial clock signal (SCK) according to the following rules:

- data is shifted MSB first, LSB last
- data is shifted out on the rising edge of SCK and is sampled on the falling edge of SCK
- data transmission length is always 16 Bit

SPI write is performed setting MSB Bit A7 of address value to 1. During read Bit A7 needs to be 0.

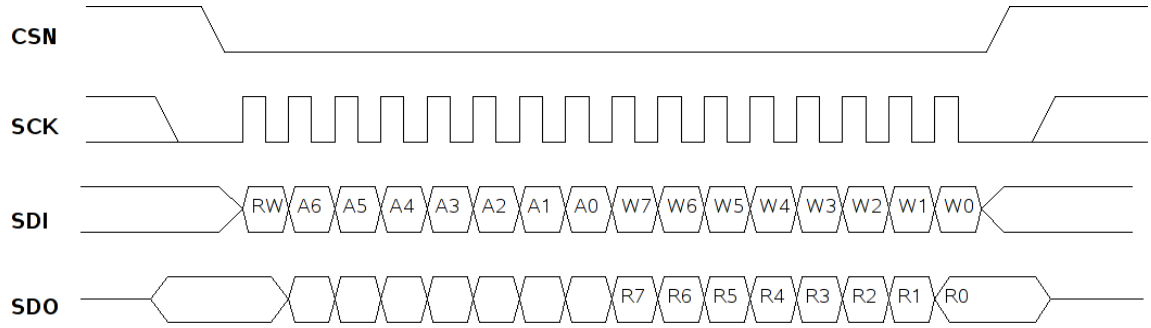


Fig. 5: SPI access

Bit RW

- **1**: write access
- **0**: read access

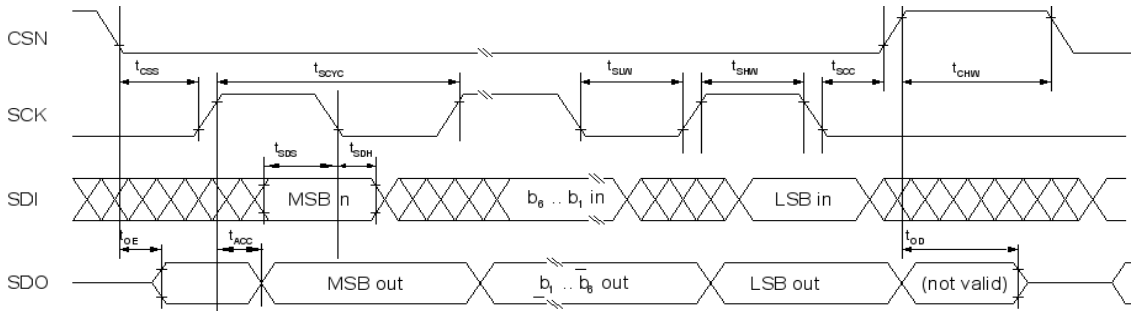


Fig. 6: SPI Timing diagram

SPI timing diagram. For configuration of write and read access check corresponding diagrams.

5.4 Watchdog; pin RSTN

Design implements watchdog functionality that can be used in window or timeout mode. Watchdog mode depends on system state.

5.4.1 Time out mode

The time out mode is an easier and less secure type of the watchdog modes. A closed window does not exist. The watchdog trigger can be applied at any time within the watchdog cycle. A watchdog trigger is detected as a write access to the register WD_TRIG. The bit TRIG_BIT must toggle. A correct watchdog trigger starts a new window period.

The period can be configured in registers WD_CFG1 and WD_CFG2 in the range from 4ms up to 1024ms using formula 4ms*(1+PER[7:0]).

In case of an incorrect watchdog trigger the SBC will enter states RESTART or FAILSAFE depending on configuration in SBC_CFG. A watchdog failure generates a reset setting the pin **RSTN** to L for $t_{WD,RSTN}$.

The first period always starts with 256ms. The first TRIG_BIT must be H.

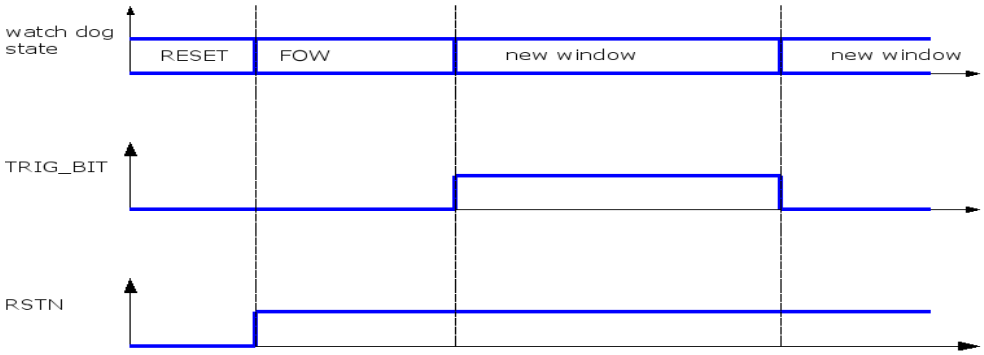


Fig. 7: watchdog time out mode

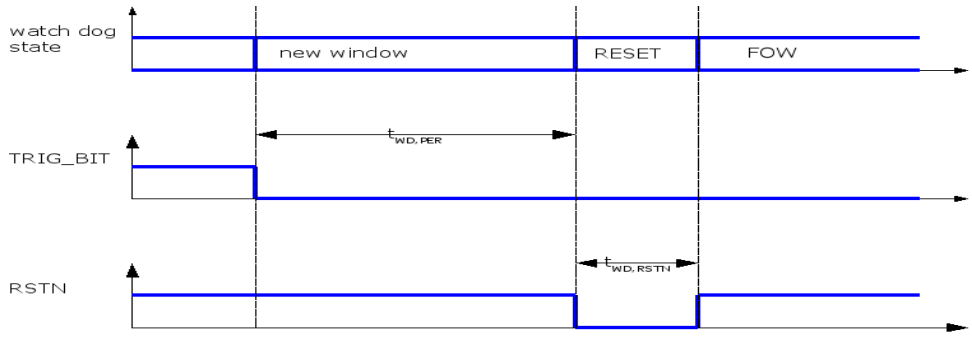


Fig. 8: watchdog time out mode without trigger

5.4.2 Window mode

The window mode is the secure type of the watchdog modes. It consists of a closed and an open window. A closed window is 50% of the configured watchdog period.

A triggering of the watchdog is only allowed in the open window. A watchdog trigger is detected as a write access to register WD_TRIG. The bit TRIG_BIT must toggle. A correct watchdog trigger starts a new window period.

The period can be configured in registers WD_CFG1 and WD_CFG2 in the range from 4ms up to 1024ms using formula 4ms*(1+PER[7:0]).

In case of an incorrect watchdog trigger the SBC will enter SBC state RESTART or FAILSAFE depending on configuration in register SBC_CFG. A watchdog generates a reset setting the pin **RSTN** to low for $t_{WD,RSTN}$.

The first period always starts with 256ms. The first TRIG_BIT must be high.

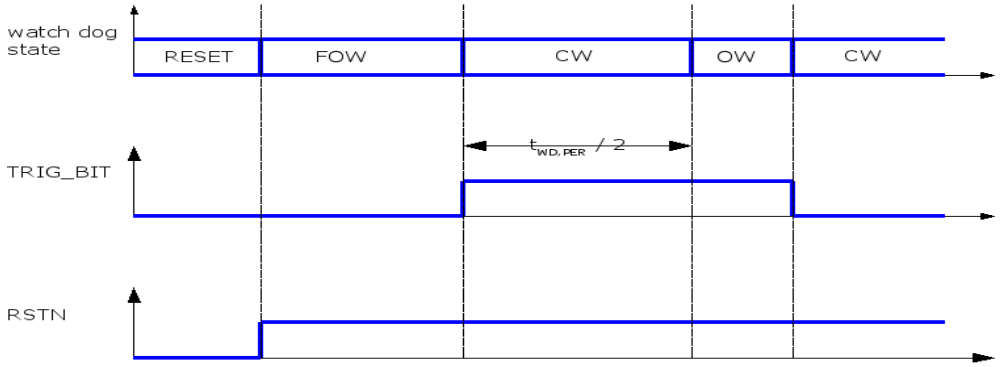


Fig. 9: watchdog window mode

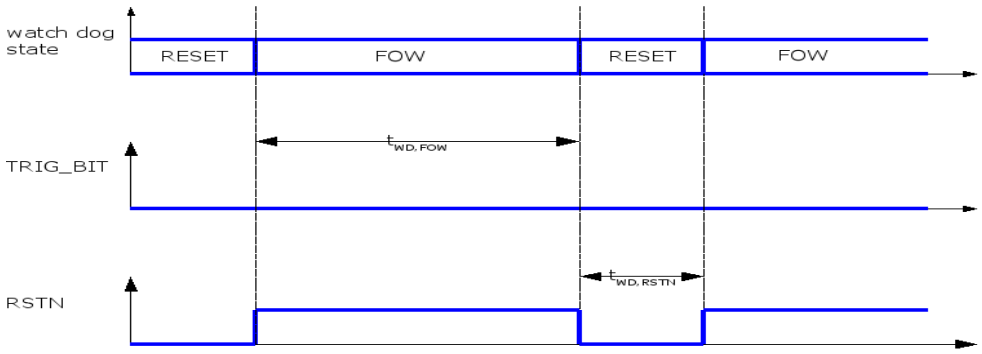


Fig. 10: watchdog window mode no trigger in FOW

Behaviour of watchdog in case of missing trigger in open window.

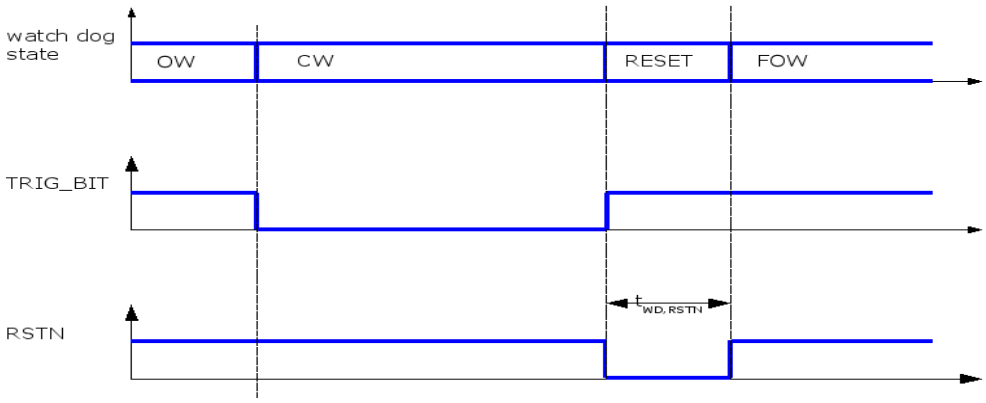


Fig. 11: watchdog window mode trigger in closed window

Behaviour of watchdog in case of trigger in closed window.

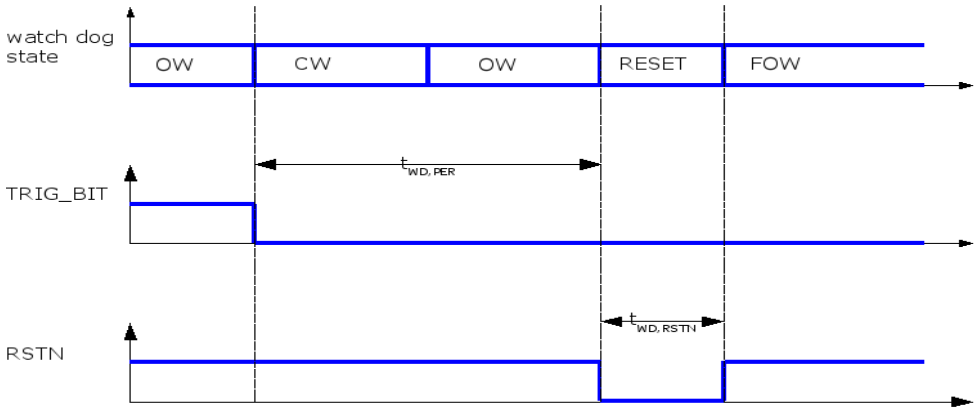


Fig. 12: watchdog window mode no trigger in open window

Behaviour of watchdog in case of missing trigger in open window.

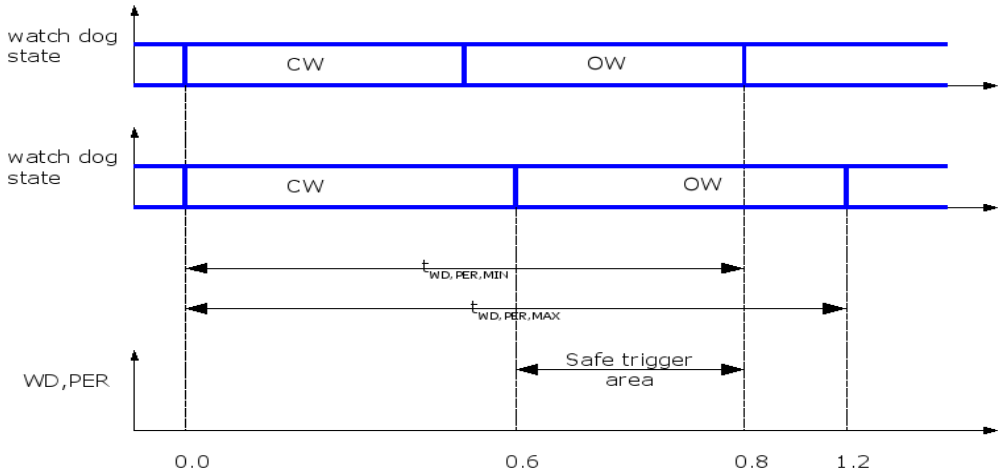


Fig. 13: safe trigger area

5.4.3 Configuration

The configuration of watchdog is allowed in SBC state NORMAL only. Registers WD_CFG1 and WD_CFG2 must be written within one watchdog cycle. The corresponding bits of WD_CFG1 and WD_CFG2 as well as WD_PER1 and WD_PER2 must be equal. Only in this case the configuration is valid. The configuration currently used can be read in registers WD_CFG and WD_PER.

Register Name	Address	Description
WD_CFG	0x08	Current watchdog configuration. Change of configuration has to be performed using WD_CFG1 and WD_CFG2 including correct watchdog trigger afterwards within one watchdog cycle in SBC state NORMAL
WD_CFG1	0x09	Watchdog configuration register 1
WD_CFG2	0x0A	Watchdog configuration register 2
WD_STAT	0x0B	Watchdog status register
WD_PER	0x0C	Current watchdog period. Change of period has to be performed using WD_PER1 and WD_PER2 including correct watchdog trigger afterwards within one watchdog cycle.
WD_TRIG	0x0D	Watchdog trigger register
WD_PER1	0x0E	Watchdog period register 1
WD_PER2	0x0F	Watchdog period register 2

Table 43: Watchdog RegisterTable

Register **WD_CFG** (0x08)

	MSB							LSB
Content	TBASE	WD	CWK1	CWK0	MODE	-	-	-
Reset value	0	0	0	0	1	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**TBASE** : In SBC state NORMAL: 1.. Output time base at **RXDLIN1** on 0.. Output time base at **RXDLIN1** off **WD** : In SBC state STOP, overwrites CWK1: 1.. Watchdog on 0.. Watchdog off **CWK1** : In SBC states STOP: 1.. Cyclic wake up on 0.. Cyclic wake up off **CWK0** : In SBC state SLEEP: 1.. Cyclic wake up on 0.. Cyclic wake up off **MODE** : → 1.. Time out mode 0.. Window mode							

Table 44: Current watchdog configuration. Change of configuration has to be performed using WD_CFG1 and WD_CFG2 including correct watchdog trigger afterwards within one watchdog cycle in SBC mode NORMAL

Register **WD_CFG1** (0x09)

	MSB							LSB
Content	TBASE	WD	CWK1	CWK0	MODE	-	-	-
Reset value	0	0	0	0	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R	R	R
Bit Description	**TBASE** : In SBC state NORMAL: 1.. Output time base at **RXDLIN1** on 0.. Output time base at **RXDLIN1** off **WD** : In SBC state STOP, overwrites CWK1: 1.. Watchdog on, 0.. Watchdog off **CWK1** : In SBC states STOP: 1.. Cyclic wake up on 0.. Cyclic wake up off **CWK0** : In SBC state SLEEP: 1.. Cyclic wake up on 0.. Cyclic wake up off **MODE** : 1.. Time out mode 0.. Window mode							

Table 45: Watchdog configuration register 1

Register **WD_CFG2** (0x0A)

	MSB							LSB
Content	-	-	-	MODE	CWK0	CWK1	WD	TBASE
Reset value	0	0	0	1	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit Description	**MODE** : 1.. Time out mode 0.. Window mode **CWK0** : In SBC state SLEEP: 1.. Cyclic wake up on 0.. Cyclic wake up off **CWK1** : In SBC states STOP: 1.. Cyclic wake up on 0.. Cyclic wake up off **WD** : In SBC state STOP, overwrites CWK1: 1.. Watchdog on 0.. Watchdog off **TBASE** : In SBC state NORMAL: 1.. Output time base at **RXDLIN1** on 0.. Output time base at **RXDLIN1** off							

Table 46: Watchdog configuration register 2

Register **WD_STAT** (0x0B)

	MSB							LSB
Content	-	-	-	-	-	-	SWDM	WDRSTN
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**SWDM** : 1.. Software development function enabled 0.. Software development function disabled **WDRSTN** : 1.. Watchdog failure event occurred 0.. No watchdog failure event occured							

Table 47: watchdog status register

Register **WD_TRIG** (0x0D)

	MSB							LSB
Content	-	-	-	-	-	-	-	TRIG
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	W
Bit Description	**TRIG** : Watchdog trigger, expects alternating content After watchdog enable first bit TRIG must be 1							

Table 48: watchdog trigger register

Register **WD_PER** (0x0C)

	MSB							LSB
Content	PER[7]	PER[6]	PER[5]	PER[4]	PER[3]	PER[2]	PER[1]	PER[0]
Reset value	0	0	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R
Bit Description	**PER[7]** : Current watchdog period setup **PER[6]** : Current watchdog period setup **PER[5]** : Current watchdog period setup **PER[4]** : Current watchdog period setup **PER[3]** : Current watchdog period setup **PER[2]** : Current watchdog period setup **PER[1]** : Current watchdog period setup **PER[0]** : Current watchdog period setup							

Table 49: Current watchdog period. Change of period has to be performed using WD_PER1 and WD_PER2 including correct watchdog trigger afterwards within one watchdog cycle.

Register **WD_PER1** (0x0E)

	MSB							LSB
Content	PER[7]	PER[6]	PER[5]	PER[4]	PER[3]	PER[2]	PER[1]	PER[0]
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**PER[7]** : Watchdog period setup **PER[6]** : Watchdog period setup **PER[5]** : Watchdog period setup **PER[4]** : Watchdog period setup **PER[3]** : Watchdog period setup **PER[2]** : Watchdog period setup **PER[1]** : Watchdog period setup **PER[0]** : Watchdog period setup							

Table 50: Watchdog period register 1

Register **WD_PER2** (0x0F)

	MSB							LSB
Content	PER[0]	PER[1]	PER[2]	PER[3]	PER[4]	PER[5]	PER[6]	PER[7]
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**PER[0]** : Watchdog period setup **PER[1]** : Watchdog period setup **PER[2]** : Watchdog period setup **PER[3]** : Watchdog period setup **PER[4]** : Watchdog period setup **PER[5]** : Watchdog period setup **PER[6]** : Watchdog period setup **PER[7]** : Watchdog period setup							

Table 51: Watchdog period register 2.

5.4.4 Watchdog timing adjustment

For very exact watchdog trigger requirements an internal time base with target frequency of 7.8125 kHz can be connected to pin **RXDLIN1**.

This function can be enabled accessing register WD_CFG.TBASE with correct access valid for watchdog configuration. Function needs to disabled via SPI again in order to receive messages using **LIN1** again.

period	minimum period	maximum period
4096 us * (WD_PER + 1)	(period - 256 us) /1.1	(period + 256 us) /0.88

Table 52: Watchdog period and accuracy

5.4.5 External Reset / Reset clamping

If RSTN is overwritten externally seven cases have to be distinguished. Please also check figure Fig. 14 for details.

1. The SBC wants to give a reset and an external source pulls the RSTN line down. After the time the SBC want to release the RSTN a timeout $t_{WDRSTN,TO,GND}$ starts. If no timeout occurs (first section in figure Fig. 14) SBC state and FSON remain unchanged.
2. If the timeout occurs and the SBC detects a RSTN clamp to GND the SBC switches to either state FAILSAFE or to state RESTART depending on configuration of bit SBC_CFG.CFG and the FSON pin is set (second section in figure Fig. 14).
3. The SBC wants to give a reset and an external source pulls the RSTN line up dominantly. At the time SBC usually releases the reset a clamp to VDD1 is detected. So SBC holds down the reset and starts timeout $t_{WDRSTN,TO,VDD1}$. If the dominant pull up releases while the timeout runs the SBC gives a regular reset and FSON remains unchanged (third section in figure Fig. 14).
4. If the dominant pull up does not release while the timeout runs SBC switches to either state FAILSAFE or to state RESTART depending on configuration of bit SBC_CFG.CFG and FSON is set (fourth section in figure Fig. 14).
5. The SBC does not want to give a reset and an external source pulls down pin **RSTN**. There are two configurations. Configuration one is SBC_CFG.CLAMP is set to one. This causes timeout $t_{WDRSTN,TO,GND}$ starting. If no timeout occurs (**fifth** section in figure Fig. 14) the state is changed to RESTART and FSON is unchanged.
6. If the timeout occurs and the SBC detects a RSTN clamp to GND the SBC switches either to mode FAILSAFE or to mode RESTART depending on configuration of bit SBC_CFG.CFG and pin FSON is set (Sixth section in figure Fig. 14).
7. Configuration two is SBC_CFG.CLAMP is set to zero. No timeout starts and the SBC detects a RSTN clamp to GND as soon as an external clamp to GND occurs. In case of this the SBC switches to either mode FAILSAFE or to mode RESTART depending on configuration of bit SBC_CFG.CFG and pin FSON is set (Seventh section in figure Fig. 14).

Fig. 14: Different RSTN behaviour

Behaviour of **RSTN** and configuration options

5.5 Local wake up; pin WK

The device can be woken up from states SLEEP and FAILSAFE via pin WK with either a rising or a falling edge. The edge sensitivity can be configured in register WK_CFG. To suppress glitches the input pin is debounced with tWK,DEB.

The wake up event is signaled at pin INTN if it is configured in register WK_CFG.

If the local wake up is not used in application, the pin WK has to be connected to pin VS.

A transition into state SLEEP is prohibited with a pending wake up request. The request must be cleared via SPI reading register WU_SRC.

Register Name	Address	Description
WK_CFG	0x10	configuration register of pin **WK.** Register is writeable in SBC state NORMAL only. In SBC states INIT, RESTART or FAILSAFE all bits are set to H.

*Table 53: **WK** RegisterTable*

Register **WK_CFG** (0x10)

	MSB							LSB
Content	-	-	-	-	-	-	FALL	RISE
Reset value	0	0	0	0	0	0	1	1
Access	R	R	R	R	R	R	R/W	R/W
Bit Description	**FALL** : A falling edge at pin **WK** leads to a wake up event. [1)] **RISE** : A rising edge at pin **WK** leads to a wake up event. [1)]							

*Table 54: configuration register of pin **WK***

1) In SBC states INIT, RESTART or FAILSAFE all bits are set to H.

5.6 LIN Transceiver; pins LIN1 to LIN4, TXDLIN1 to TXDLIN4, RXDLIN1 to RXDLIN4, GND-LIN

5.6.1 Characteristics

The LIN BUS physical interface is implemented as a LIN 2.1 standard high-voltage single wire interface (ISO 9141) for baud rates from 2.4kBds to 20.4kBds. The LIN bus has two logical values; the dominant state (BUS voltage near GND) represents logical LOW level and the recessive state (BUS voltage near VS) represents logical HIGH level. In the recessive state the BUS is pulled high by an internal pull-up resistor (typ. 30 kΩ) and a diode in series, so no external pull-up components are required for slave applications. Master applications require an additional external pull-up resistor and a series diode. The LIN protocol output data stream on the TXD signal is converted into the LIN bus signal through a current limited, wave-shaping low-side driver with control as outlined by the LIN Physical Layer Specification Revision 2.1. The receiver converts the data stream from the bus and outputs it to RXD.

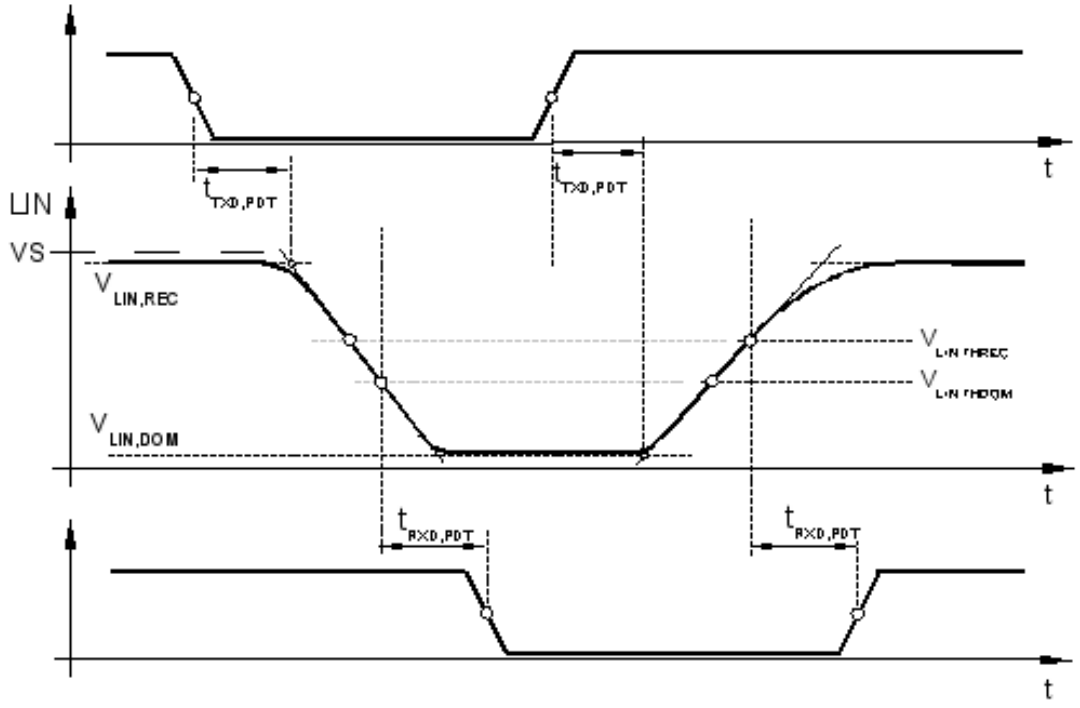


Fig. 15: LIN transceiver physical layer timing

The LIN transceiver can handle a bus voltage swing from +40V down to ground and survives -27V. The device also prevents back feed current through the LIN pin to the supply pin in case of a ground shift / loss or supply voltage disconnection.

In sleep mode the LIN block requires a very low quiescent current by using a special wake up comparator allowing the remote wakeup via the LIN bus. The sleep mode can be activated during recessive or dominant level of LIN bus line.

5.6.2 LIN Flash Mode

A Flash mode allows an increasing of the transmit baud rate up to 115kBds and the receiver baud rate up to 250kBds. The feature is configured in register LINx_CFG.

5.6.3 LIN Wake Up

The device can be woken up remotely using corresponding pin **LINx**. The wake up capability can be switched on in corresponding register LINx_CFG. In state FAILSAFE this feature is enabled regardless of configuration.

When a wake up is recognized, the corresponding flag in register WU_SRC is set.

The device supports two different behaviours.

1. A falling edge at pin **LIN** followed by a dominant bus level $V_{LIN,DOM}$ maintained for a time period $t_{LIN,WU}$ results in a remote wake up request.
2. A falling edge at pin **LIN** followed by a dominant bus level $V_{LIN,DOM}$ maintained for a time period $t_{LIN,WU}$, followed by a rising edge results in a remote wake up request.

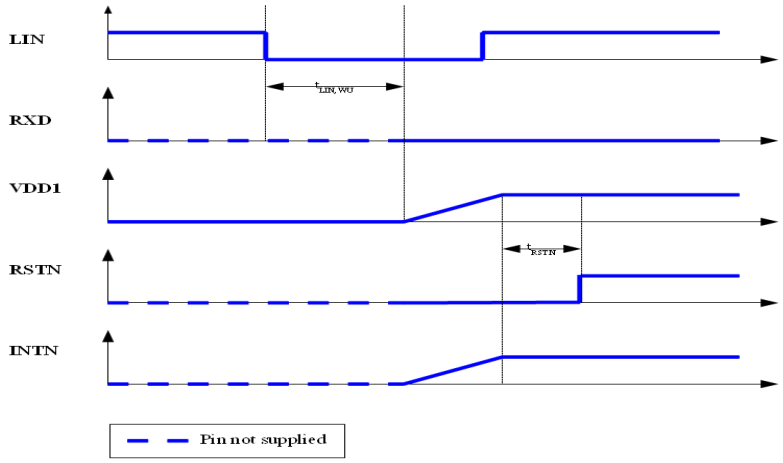


Fig. 16: LIN wake up in mode SLEEP

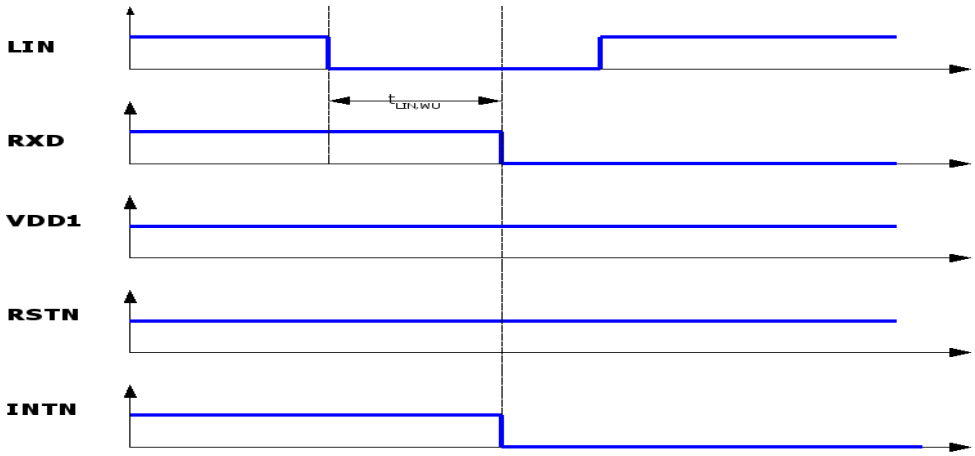


Fig. 17: LIN wake up in mode INIT

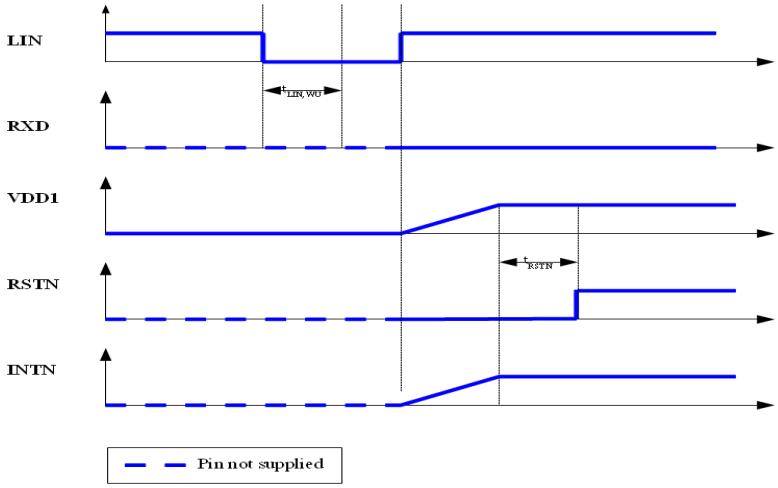


Fig. 18: LIN wake up at rising edge in mode SLEEP

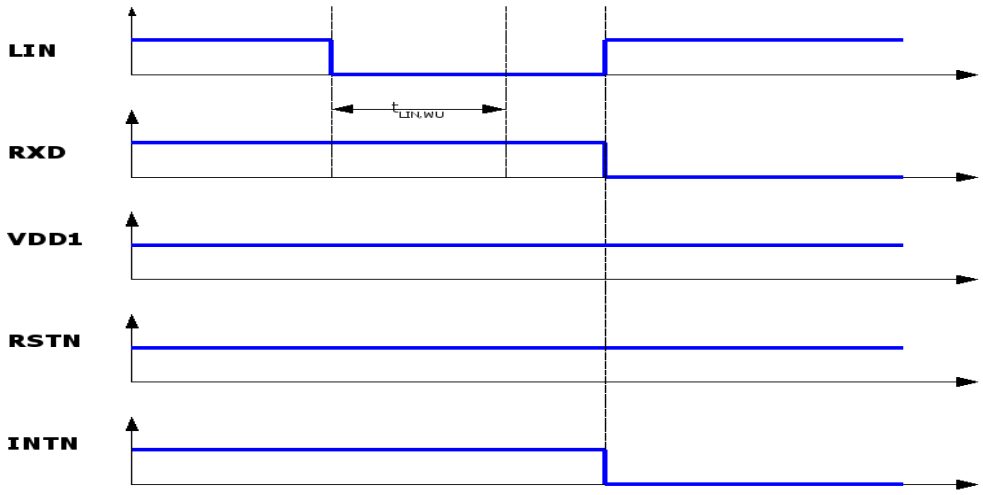


Fig. 19: LIN wake up at rising edge in mode INIT

5.6.4 LIN Failure detection and recovery

All local or bus failures are signaled in register LINx_STAT.

There are two possibilities to recover the normal operation after a failure:

- Sending two SPI commands for LIN Normal Mode, first disable receiver, second enable receiver
- If RXD is dominant while TXD is recessive since LIN receives dominant bus levels again without driving the bus dominant by itself

TXD Dominant clamping failure

This failure can only be detected if the LINx transmitter is enabled, e.g. if bit TR in register LINx_CFG is set to high. If **TXDx** is clamped dominant for longer than $t_{LIN,TXD,DOM}$ the transmitter is disabled and a failure flag is set.

RXD dominant clamping failure

This failure can be detected if the receiver is enabled, e.g. if bit TR in register LINx_CFG is set. If **RXDx** is clamped to dominant level for 4 consecutive LINx cycles the transmitter is disabled and a failure flag is set.

RXD recessive clamping failure

This failure can be detected if the receiver is enabled, e.g. bit TR in register LINx_CFG is set. If **RXDx** is clamped to recessive level for 4 consecutive **LINx** cycles the transmitter is disabled and a failure flag is set.

BUS dominant clamping failure

This failure can be detected if the receiver is enabled, e.g. if bit TR in register LINx_CFG is set. If **LINx** is clamped to low for longer than $t_{LIN,BUS,DOM}$ a failure flag is set. The transmitter is not disabled.

OT failure

If OT occurs transmitter is disabled and a failure flag is set. The transmitter is enabled if the temperature falls below its threshold and if the conditions for the failure recovery are present.

TXD to RXD clamping failure

This failure can only be detected if the transmitter is enabled. Pin **TXDLINx** is set to low that LINx becomes dominant. Afterwards pin **RXDLINx** is set to low too controlled by the receiver. In case of error c52ondition present pin **TXDLINx** can not be released to high because the driver of **RXDLINx** is much stronger. If **TXDLINx** is clamped dominant for longer than $t_{LIN,TXD,DOM}$ the transmitter is disabled and a failure flag is set.

5.6.5 LIN Configuration

All configuration registers are writeable in state NORMAL only .

Register Name	Address	Description
LIN_CFG	0x06	Shortcut to LIN1-4 TR and RC configuration bits
LIN1_CFG	0x20	Configuration register for LIN1
LIN_INT	0x21	LIN interrupt register
LIN1_STAT	0x22	Status register for LIN1
LIN2_CFG	0x24	Configuration register for LIN2
LIN2_STAT	0x26	Status register for LIN2
LIN3_CFG	0x28	Configuration register for LIN3
LIN3_STAT	0x2A	Status register for LIN3
LIN4_CFG	0x2C	Configuration register for LIN4
LIN4_STAT	0x2E	Status register for LIN4

Table 55: LIN RegisterTable

Register **LIN_INT** (0x21)

	MSB							LSB
Content	LIN4	LIN3	LIN2	LIN1	-	-	-	-
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**LIN4** : 1.. LIN4 is reason for interrupt 0.. LIN4 is not reason for interrupt **LIN3** : 1.. LIN3 is reason for interrupt 0.. LIN3 is not reason for interrupt **LIN2** : 1.. LIN2 is reason for interrupt 0.. LIN2 is not reason for interrupt **LIN1** : 1.. LIN1 is reason for interrupt 0.. LIN1 is not reason for interrupt							

Table 56: LIN interrupt register

Register **LIN1_CFG** (0x20)

	MSB							LSB
Content	-	FAILINT	FLASH	WUINT	WUCFG	WU	TR	RC
Reset value	0	0	0	0	1	1	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**FAILINT** : 1...Interrupt enabled for LIN failures, could only be set if RC is set. This is locked by hardware. 0...Interrupt disabled for LIN failures **FLASH** : The FLASH mode deactivates filtering and provides a baud rate of up to 125kBaud for transmitting and 250kBaud for receiving. 1...Flash mode enabled 0...Flash mode disabled **WUINT** : 1...Interrupt enabled if WU is detected 0...Interrupt disabled if WU is detected **WUCFG** : 1... Wake up is performed with next rising edge after LIN wake up debounce time 0.. Wake up is performed after LIN wake up debounce time **WU** : 1...Wake up capability enabled, could only be set if RC and TR are not set. This is locked by hardware. 0...Wake up capability disabled **TR** : 1...Transmitter enabled, RC is enabled automatically, WU is cleared 0...Transmitter disabled **RC** : 1...receiver enabled, read bus only, WU is cleared 0...receiver disabled							

Table 57: Configuration register for LIN1

Register **LIN1_STAT** (0x22)

	MSB							LSB
Content	-	Bus short	TXDDOM	BUSDOM	RXDREC	RXDDOM	-	-
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**Bus short** : 1...LIN short circuit detected 0...LIN short circuit not detected **TXDDOM** : 1...TXD permanent dominant clamping timeout exceeded 0...TXD permanent dominant clamping timeout not exceeded **BUSDOM** : 1...LIN permanent dominant clamping timeout exceeded 0...LIN permanent dominant clamping timeout not exceeded **RXDREC** : 1...RXD permanent recessive clamping timeout exceeded 0...RXD permanent recessive clamping timeout not exceeded **RXDDOM** : 1...RXD permanent dominant clamping timeout exceeded 0...RXD permanent dominant clamping timeout not exceeded							

Table 58: Status register for LIN1

Register **LIN2_CFG** (0x24)

	MSB							LSB
Content	-	FAILINT	FLASH	WUINT	WUCFG	WU	TR	RC
Reset value	0	0	0	0	1	1	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**FAILINT** : 1...Interrupt enabled for LIN failures, could only be set if RC is set. This is locked by hardware. 0...Interrupt disabled for LIN failures **FLASH** : The FLASH mode deactivates filtering and provides a baud rate of up to 125kBaud for transmitting and 250kBaud for receiving. 1...Flash mode enabled 0...Flash mode disabled **WUINT** : 1...Interrupt enabled if WU is detected 0...Interrupt disabled if WU is detected **WUCFG** : 1... Wake up is performed with next rising edge after LIN wake up debounce time 0.. Wake up is performed after LIN wake up debounce time **WU** : 1...Wake up capability enabled, could only be set if RC and TR are not set. This is locked by hardware. 0...Wake up capability disabled **TR** : 1...Transmitter enabled, RC is enabled automatically, WU is cleared 0...Transmitter disabled **RC** : 1...receiver enabled, read bus only, WU is cleared 0...receiver disabled							

Table 59: Configuration register for LIN2

Register **LIN2_STAT** (0x26)

	MSB							LSB
Content	-	Bus short	TXDDOM	BUSDOM	RXDREC	RXDDOM	-	-
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**Bus short** : 1...LIN short circuit detected 0...LIN short circuit not detected **TXDDOM** : 1...TXD permanent dominant clamping timeout exceeded 0...TXD permanent dominant clamping timeout not exceeded **BUSDOM** : 1...LIN permanent dominant clamping timeout exceeded 0...LIN permanent dominant clamping timeout not exceeded **RXDREC** : 1...RXD permanent recessive clamping timeout exceeded 0...RXD permanent recessive clamping timeout not exceeded **RXDDOM** : 1...RXD permanent dominant clamping timeout exceeded 0...RXD permanent dominant clamping timeout not exceeded							

Table 60: Status register for LIN2

Register **LIN3_CFG** (0x28) - should not be used with E521.02 and E521.12

	MSB							LSB
Content	-	FAILINT	FLASH	WUINT	WUCFG	WU	TR	RC
Reset value	0	0	0	0	1	1	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**FAILINT** : 1...Interrupt enabled for LIN failures, could only be set if RC is set. This is locked by hardware. 0...Interrupt disabled for LIN failures **FLASH** : The FLASH mode deactivates filtering and provides a baud rate of up to 125kBaud for transmitting and 250kBaud for receiving. 1...Flash mode enabled 0...Flash mode disabled **WUINT** : 1...Interrupt enabled if WU is detected 0...Interrupt disabled if WU is detected **WUCFG** : 1... Wake up is performed with next rising edge after LIN wake up debounce time 0.. Wake up is performed after LIN wake up debounce time **WU** : 1...Wake up capability enabled, could only be set if RC and TR are not set. This is locked by hardware. 0...Wake up capability disabled **TR** : 1...Transmitter enabled, RC is enabled automatically, WU is cleared 0...Transmitter disabled **RC** : 1...receiver enabled, read bus only, WU is cleared 0...receiver disabled							

Table 61: Configuration register for LIN3

Register **LIN3_STAT** (0x2A) - should not be used with E521.02 and E521.12

	MSB							LSB
Content	-	Bus short	TXDDOM	BUSDOM	RXDREC	RXDDOM	-	-
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**Bus short** : 1...LIN short circuit detected 0...LIN short circuit not detected **TXDDOM** : 1...TXD permanent dominant clamping timeout exceeded 0...TXD permanent dominant clamping timeout not exceeded **BUSDOM** : 1...LIN permanent dominant clamping timeout exceeded 0...LIN permanent dominant clamping timeout not exceeded **RXDREC** : 1...RXD permanent recessive clamping timeout exceeded 0...RXD permanent recessive clamping timeout not exceeded **RXDDOM** : 1...RXD permanent dominant clamping timeout exceeded 0...RXD permanent dominant clamping timeout not exceeded							

Table 62: Status register for LIN3

Register **LIN4_CFG** (0x2C) - should not be used with E521.02, E521.03, E521.12 and E521.13

	MSB							LSB
Content	-	FAILINT	FLASH	WUINT	WUCFG	WU	TR	RC
Reset value	0	0	0	0	1	1	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**FAILINT** : 1...Interrupt enabled for LIN failures, could only be set if RC is set. This is locked by hardware. 0...Interrupt disabled for LIN failures **FLASH** : The FLASH mode deactivates filtering and provides a baud rate of up to 125kBaud for transmitting and 250kBaud for receiving. 1...Flash mode enabled 0...Flash mode disabled **WUINT** : 1...Interrupt enabled if WU is detected 0...Interrupt disabled if WU is detected **WUCFG** : 1... Wake up is performed with next rising edge after LIN wake up debounce time 0.. Wake up is performed after LIN wake up debounce time **WU** : 1...Wake up capability enabled, could only be set if RC and TR are not set. This is locked by hardware. 0...Wake up capability disabled **TR** : 1...Transmitter enabled, RC is enabled automatically, WU is cleared 0...Transmitter disabled **RC** : 1...receiver enabled, read bus only, WU is cleared 0...receiver disabled							

Table 63: Configuration register for LIN4

Register **LIN4_STAT** (0x2E) - should not be used with E521.02, E521.03, E521.12 and E521.13

	MSB							LSB
Content	-	Bus short	TXDDOM	BUSDOM	RXDREC	RXDDOM	-	-
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**Bus short** : 1...LIN short circuit detected 0...LIN short circuit not detected **TXDDOM** : 1...TXD permanent dominant clamping timeout exceeded 0...TXD permanent dominant clamping timeout not exceeded **BUSDOM** : 1...LIN permanent dominant clamping timeout exceeded 0...LIN permanent dominant clamping timeout not exceeded **RXDREC** : 1...RXD permanent recessive clamping timeout exceeded 0...RXD permanent recessive clamping timeout not exceeded **RXDDOM** : 1...RXD permanent dominant clamping timeout exceeded 0...RXD permanent dominant clamping timeout not exceeded							

Table 64: Status register for LIN4

Register **LIN_CFG** (0x06)

	MSB							LSB
Content	TR4	RC4	TR3	RC3	TR2	RC2	TR1	RC1
Reset value	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**TR4** : Same as LIN4_CFG.TR. Should set to 0 with E521.02, E521.03, E521.12 and E521.13 **RC4** : Same as LIN4_CFG.RC. Should set to 0 with E521.02, E521.03, E521.12 and E521.13 **TR3** : Same as LIN3_CFG.TR. Should set to 0 with E521.02 and E521.12 **RC3** : Same as LIN3_CFG.RC. Should set to 0 with E521.02 and E521.12 **TR2** : Same as LIN2_CFG.TR **RC2** : Same as LIN2_CFG.RC **TR1** : Same as LIN1_CFG.TR **RC1** : Same as LIN1_CFG.RC							

Table 65: Shortcut to LIN1-4 TR and RC configuration bits

5.7 HS-CAN Transceiver; pins CANH, CANL, RXDCAN, TXDCAN, VDDCAN

The HS-CAN transceiver is compatible to ISO 11898-5.

CANH and CANL interface the CAN protocol controller to HS-CAN physical layer wires. Data rate can be selected up to 1MegBaud.

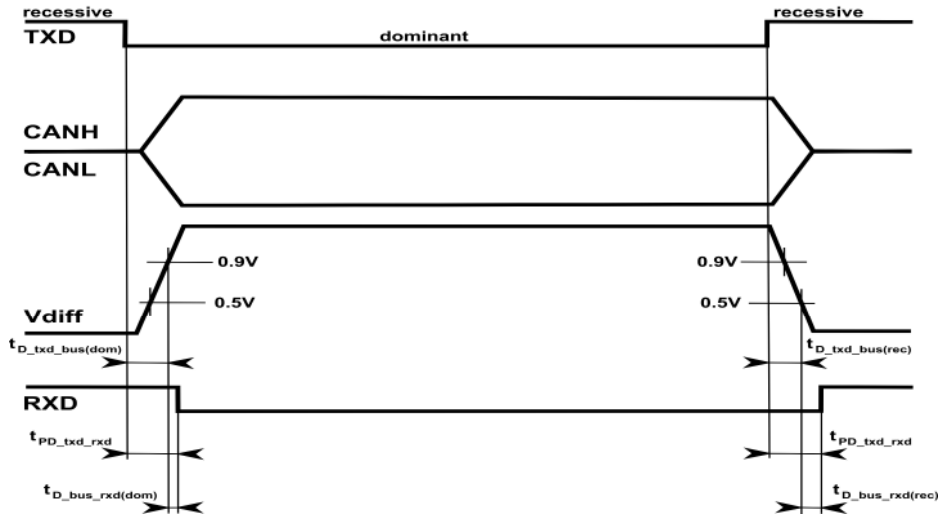


Fig. 20: HS-CAN Bus timing

5.7.1 CAN Wake up

The device is capable detecting wake up pattern at the CAN bus if configured. A wake up pattern ideally consists of four consecutive symbols dominant, recessive, dominant and recessive. The dominant bus states have to be longer than $t_{CAN,WAKE\_BUS\_DOM}$ and the recessive bus states have to be longer than $t_{CAN,WAKE\_BUS\_REC}$. The pattern must be applied within t_{WAKE2}.

When the wake up pattern is recognized, the corresponding flag in register WU_SRC is set.Pin **INTN** is set low if bit CAN_CFG.WUINT was set high. Pin **RXDCAN** is set to low until bit CAN_CFG.RC is set high or register WU_SRC is read.

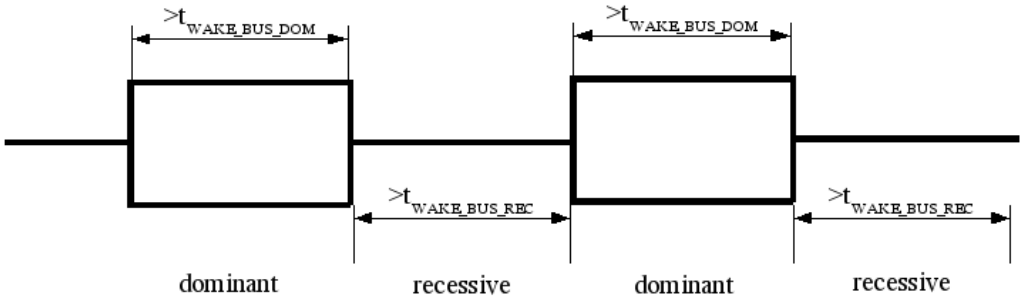


Fig. 21: Remote Wakeup Pattern

5.7.2 CAN Failure detection and recovery

All CAN related local or bus failures are signaled in register CAN_STAT.

There are two possibilities to recover the normal operation after a failure:

- Sending the SPI command for CAN Normal Operation Mode
- If RXD is dominant while TXD is recessive

TXD Dominant clamping failure

This failure can only be detected if the transmitter is enabled, e.g. bit TR in register CAN_CFG is set to high. If **TXDCAN** is clamped dominant for longer than $t_{CAN,TXD,DOM}$ the transmitter is disabled and a failure flag is set.

RXD dominant clamping failure

This failure can be detected if the receiver is enabled, e.g. bit RC or TR in register CAN_CFG is set. If **RXDCAN** is clamped low for 4 consecutive **CAN** cycles the transmitter is disabled and a failure flag is set.

RXD recessive clamping failure

This failure can be detected if the receiver is enabled, e.g. bit RC or TR in register CAN_CFG is set. If **RXDCAN** is clamped recessive level for 4 consecutive **CAN** cycles the transmitter is disabled and a failure flag is set.

BUS dominant clamping failure

This failure can be detected if the receiver is enabled, e.g. bit RC or TR in register CAN_CFG is set. If CAN is clamped dominant for longer than $t_{CAN,BUS,DOM}$ a failure flag is set. The transmitter is not disabled.

TXD to RXD clamping failure

This failure can only be detected if the transmitter is enabled. Pin **TXDCAN** is set to low that CAN becomes dominant. Afterwards pin **RXDCAN** is set to low too controlled by the receiver. In case of error condition present pin **TXDCAN** can not be released to high because the driver of **RXDCAN** is much stronger. If **TXDCAN** is clamped dominant for longer than $t_{CAN,TXD,DOM}$ the transmitter is disabled and a failure flag is set.

OT failure

If OT occurs the transmitter is disabled and a failure flag is set. The transmitter is enabled again if the temperature falls below its threshold and the conditions for the failure recovery are present.

CANH to GND clamping failure

This failure can be detected if the transmitter is enabled, e.g. bit TR in register CAN_CFG is set. If the short is present for 4 consecutive **CAN** cycles of at least $t_{BUS,FAIL}$ a failure flag is set. The transmitter is not disabled. The failure is cleared if CANH is not clamped to GND anymore.

CANL to GND clamping failure

This failure can be detected if the transmitter is enabled, e.g. bit TR in register CAN_CFG is set. If the short is present for 4 consecutive **CAN** cycles of at least $t_{BUS,FAIL}$ a failure flag is set. The transmitter is not disabled. The failure is cleared if CANH is not clamped to GND anymore.

CANH to VDDCAN/VS clamping failure

This failure can be detected if the transmitter is enabled, e.g. bit TR in register CAN_CFG is set. If the short is present for 4 consecutive **CAN** cycles of at least $t_{BUS,FAIL}$ a failure flag is set. The transmitter is not disabled. The failure is cleared if CANH is not clamped to **VDDCAN/VS** anymore.

CANL to VCC/VS clamping failure

This failure can be detected if the transmitter is enabled, e.g. bit RC or TR in register CAN_CFG is set. If the short is present for 4 consecutive **CAN** cycles of at least $t_{BUS,FAIL}$ a failure flag is set. The transmitter is not disabled. The failure is cleared if CANH is not clamped to **VDDCAN/VS** anymore.

5.7.3 CAN Configuration

Register Name	Address	Description
CAN_CFG	0x30	Configuration register for CAN
CAN_STAT	0x32	Status register for CAN

Table 66: CAN RegisterTable

Register **CAN_CFG** (0x30)

	MSB							LSB
Content	-	FAILINT	-	WUINT	BF	WU	TR	RC
Reset value	0	0	0	1	0	1	0	0
Access	R	R/W	R	R/W	R/W	R/W	R/W	R/W
Bit Description	**FAILINTEN** : 1...interrupt enabled for CAN failures 0...interrupt disabled for CAN failures **WUINT** : 1...interrupt enabled if WU is detected 0...interrupt disabled if WU is detected **BF :** 1.. CAN bus short failure detection enabled 0.. CAN bus short failure detection disabled **WU** : 1...wake up capability enabled, only valid if RC and TR are 0 0...wake up capability disabled **TR** : 1...transmitter enabled, RC is enabled automatically, WU is masked 0...transmitter disabled **RC** : 1...receiver enabled, listen only, WU is masked 0...receiver disabled							

Table 67: Configuration register for CAN

Register **CAN_STAT** (0x32)

	MSB							LSB
Content	CHVCC	CHGND	CLVCC	CLGND	RXDREC	RXDDOM	BUSDOM	TXDDOM
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**CHVCC** : 1.. CANH to VCC or VS clamping detected 0.. CANH to VCC or VS clamping not detected **CHGND** : 1.. CANH to GND clamping detected 0.. CANH to GND clamping not detected **CLVCC** : 1.. CANL to VCC or VS clamping detected 0.. CANL to VCC or VS clamping not detected **CLGND** : 1.. CANL to GND clamping detected 0.. CANL to GND clamping not detected **RXDREC** : 1.. RXD permanent recessive clamping timeout exceeded 0.. RXD permanent recessive clamping timeout not exceeded **RXDDOM** : 1.. RXD permanent dominant clamping timeout exceeded 0.. RXD permanent dominant clamping timeout not exceeded **BUSDOM** : 1.. CAN permanent dominant clamping timeout exceeded 0.. CAN permanent dominant clamping timeout not exceeded **TXDDOM** : 1.. TXD permanent dominant clamping timeout exceeded 0.. TXD permanent dominant clamping timeout not exceeded							

Table 68: Status register for CAN

5.8 Limp Home support; pin FSON

SBC features limp home support using pin **FSON**.

Activation of **FSON** is not linked to SBC mode FAILSAFE only. Please check sections 5.8.1 and 5.2 for details.

In order to activate output pin **FSON** using SPI command. Both registers FSON_CFG1 and FSON_CFG2 need to be accessed within one watchdog period for system safety reasons. If contents of registers is equal pin FSON is activated when watchdog is triggered. Otherwise no change is made.

Register Name	Address	Description
FSON_STAT	0x02	FSON status register.
FSON_CFG1	0x1B	FSON configuration register 1
FSON_CFG2	0x1C	FSON configuration register 2

Table 69: FSON RegisterTable

Register **FSON_CFG1** (0x1B)

	MSB							LSB
Content	CLAMP	-	-	SPI	-	-	-	-
Reset value	1	0	0	0	0	0	0	0
Access	R/W	R	R	R/W	R	R	R	R
Bit Description	**CLAMP** : 1.. External reset shorter than $t_{WDRSTN,TO,GND}$ will not lead to **FSON** set 0.. External reset leads to **FSON** set immediately **SPI** : 1.. Activate FSON 0.. Deactivate FSON							

Table 70: FSON configuration register 1

Register **FSON_CFG2** (0x1C)

	MSB							LSB
Content	-	-	-	-	SPI	-	-	CLAMP
Reset value	0	0	0	0	0	0	0	1
Access	R	R	R	R	R/W	R	R	R/W
Bit Description	**SPI** : 1.. Activate FSON 0.. Deactivate FSON **CLAMP** : 1.. External reset shorter than $t_{WDRSTN,TO,GND}$ will not lead to **FSON** set 0.. External reset leads to **FSON** set immediately							

Table 71: FSON configuration register 2

Register **FSON_STAT** (0x02)

	MSB							LSB
Content	-	VDD1UV	WD	OT	INITTO	RSTNSC	FSON_SPI	FSON_INT
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**VDD1UV** : 1..**VDD1** under voltage detected 0..**VDD1** under voltage not detected **WD** : 1..Watchdog trigger failure detected 0..Watchdog trigger failure not detected **OT** : 1..Over temperature detected 0..Over temperature not detected **INITTO** : 1..Timeout in mode INIT detected 0..Timeout in mode INIT not detected **RSTNSC** : 1..**RSTN** clamped low externally 0..**RSTN** not clamped low externally **FSON_SPI** : 1..**FSON** activated via SPI 0..**FSON** not activated via SPI **FSON_INT** : 1..**FSON** activated due to FAILSAFE condition detected 0..**FSON** not activated due to no FAILSAFE condition detected							

Table 72: FSON status register.

5.8.1 Activation of FSON

FSON is activated in following cases:

1. SBC init mode not left within time $t_{TO,INIT}$
2. VDD1 time out $t_{TO,VDD1}$
3. Activated by SPI command accessing FSON_CFG1.FSON_SPI and FSON_CFG2.FSON_SPI within one watchdog cycle
4. Permanent clamping of **RSTN** to **GND**
5. Permanent clamping of **RSTN** to **VDD1**
6. External Reset on RSTN (partly configurable withSBC_CFG.CLAMP)
7. Over temperature
8. Watchdog failure

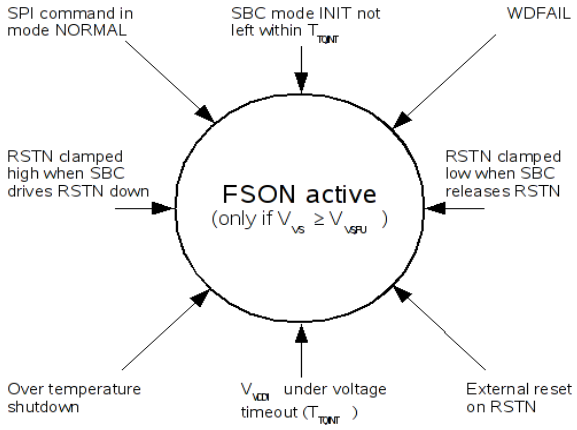


Fig. 22: Activation of FSON

Activation sources for limp home output **FSON**

5.8.2 Deactivation of FSON

FSON is deactivated in following cases:

1. µC sent deactivation command via SPI AND SBC is in state NORMAL AND µC sent correct watchdog trigger
2. VS falls below $VS_{VS,PD}$

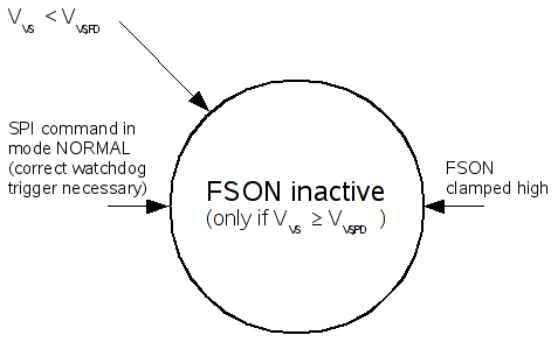


Fig. 23: Deactivation of FSON

Deactivation sources for limp home output **FSON**

5.9 Interrupt; pin INTN

The interrupt pin is driven low if the following interrupt sources/conditions occur:

- wake up event at CAN, LIN or WK, cyclic wake up
- over temperature warning
- over temperature shut down
- under voltage at **VDD1** or **VDD2**
- communication failures at CAN or LIN

Interrupts can be enabled in configuration registers of the corresponding modules.

For over temperature and under voltage the appearance and disappearance is signaled via an interrupt. Therefore after SPI reading of interrupt source pin **INTN** is not blocked if the interrupt condition is still active.

In order to evaluate detailed reason for interrupt read corresponding status registers.

Register Name	Address	Description
INT	0x03	Interrupt status register
VDD_STAT	0x1A	VDD1, VDD2 and VDDCAN status information.

Table 73: INTN RegisterTable

Register **INT** (0x03)

	MSB							LSB
Content	CAN	LIN	WAKE	VDDx	OTWARN	OT	FSM/SPI	-
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**CAN** : 1... HS-CAN interface is reason for interrupt **LIN** : 1... At least one of the LIN interfaces is reason for interrupt **WAKE** : 1... Wake up event is reason for interrupt **VDDx** : 1... Under voltage condition is reason for interrupt **OTWARN** : 1... Over temperature warning level crossing is reason for interrupt **OT** : 1... Over temperature shutdown level crossing is reason for interrupt **FSM/SPI** : 1... FSM or SPI are reasons for interrupt							

Table 74: Interrupt status register

Register **VDD_STAT** (0x1A)

	MSB							LSB
Content	VDD2 ON	VDD2 ENA PAD	VDD2OC	VDD2 UV	-	VDDCAN UV	VDD1 UV	-
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit Description	**VDD2 ON** : 1..Linear voltage regulator **VDD2** enabled 0..Linear voltage regulator **VDD2** disabled **VDD2 ENA PAD** : 1..**ENVDD2** set to logic level 1 0..**ENVDD2** set to logic level 0 **VDD2OC** : 1..**VDD2** over current detected 0..**VDD2** over current not detected **VDD2 UV** : 1.. **VDD2** under voltage detected 0.. **VDD2** under voltage not detected **VDDCAN UV** : 1.. **VDDCAN** under voltage detected. If CAN is not activated, this bit is high without generating a interrupt in this case. 0.. **VDDCAN** under voltage not detected **VDD1 UV** : 1.. **VDD1** under voltage detected 0.. **VDD1** under voltage not detected							

Table 75: VDD1, VDD2 and VDDCAN status information.

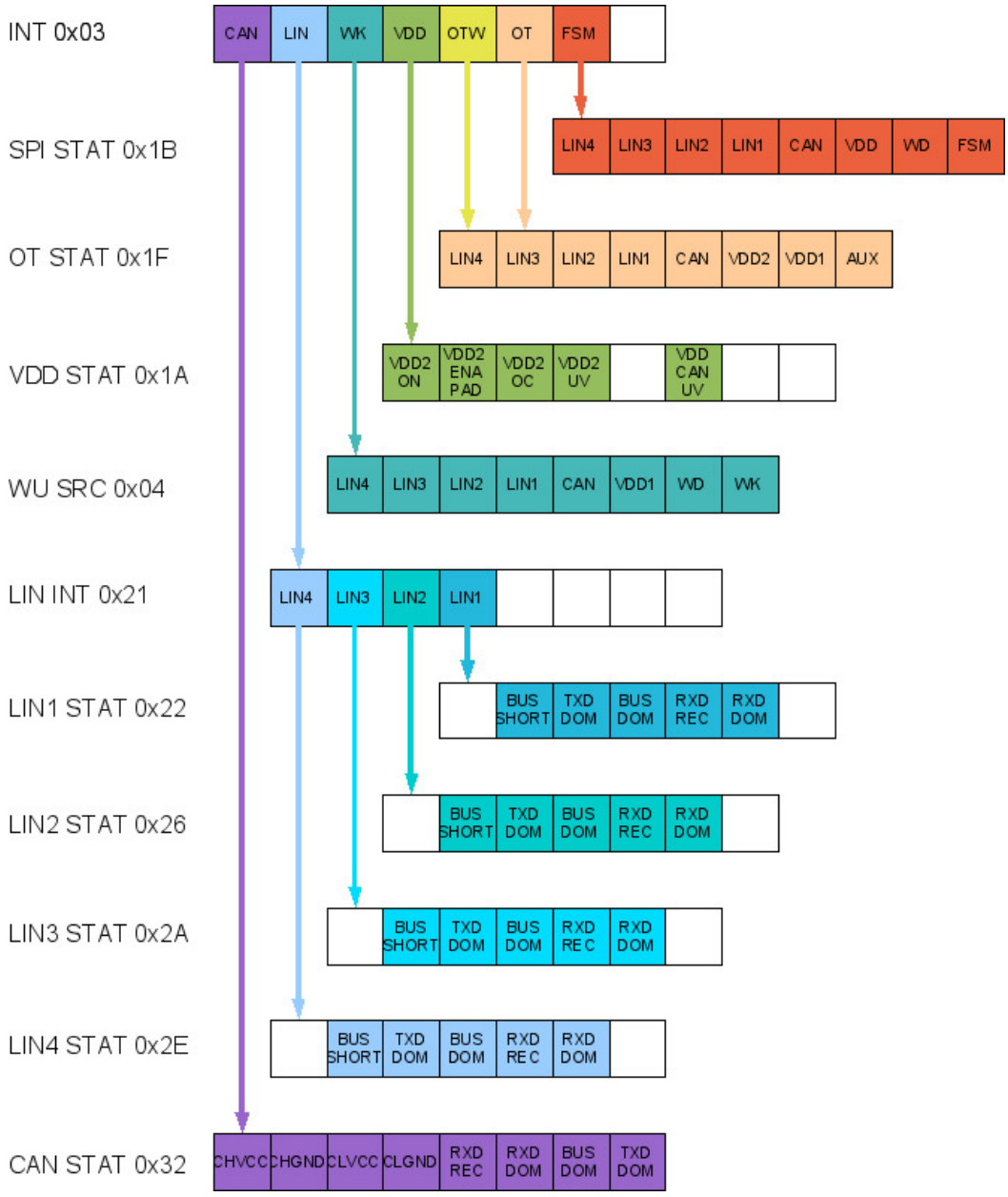


Fig. 24: Interrupt and status register dependency

In case of interrupt detailed information can be read from device in order to evaluate reason for interrupt.

5.10 DCDC Buck converter; pins VIN, VDD1, VDD1SENSE, LXT, PGND

Register Name	Address	Description
VDD1_CFG	0x14	VDD1 configuration register Writing register in SBC state FAILSAFE is not allowed

Table 76: VDD1 RegisterTable

Register **VDD1_CFG** (0x14)

	MSB							LSB
Content	t1_1	t1_0	IDLE	-	-	STOP	THR_1	THR_0
Reset value	0	1	1	0	0	0	0	0
Access	R/W	R/W	R/W	R	R	R	R/W	R/W
Bit Description	**t1_1** : configuration of time t1 for SBC mode STOP observation **t1_0** : configuration of time t1 for SBC mode STOP observation 00...5ms 01...10ms 10...20ms 11...40ms **IDLE :** 1.. activate IDLE prevention 0.. deactivate IDLE prevention IDLE detected: • DCDC on • DCDC reports IDLE • V(VDD1) < typ. 0.98*$VDD1_{nom}$ **STOP : selection of behaviour in state stop** 1..in case of high current consumption state remains in STOP 0..in case of high current consumption state is changed to NORMAL **THR_1** : selection of reset threshold **THR_0** : selection of reset threshold 00...$V_{TH1,VDD1,RSTN}$ 01...$V_{TH2,VDD1,RSTN}$ 10...$V_{TH3,VDD1,RSTN}$ 11...$V_{TH4,VDD1,RSTN}$							

Table 77: VDD1 configuration register

Remark: Register Writing register in SBC state FAILSAFE is not allowed

5.10.1 General Description

The DCDC buck converter is a fixed output voltage step-down converter intended for automotive and general battery driven applications, featuring open loop stability and short current limitation for the integrated driver transistor.

The device is offered in a 5V output voltage version providing up to 500mA output current.

The modulation scheme is based on **P**ulse **F**requency **M**odulation. For operation a clock signal is not needed, providing minimum ON/OFF time regulation for the internal switch. Internal current measurement allows to reduce the ON time below the given nominal ON time to prevent excessive current flow in the inductor.

5.10.2 Pulse Frequency Modulated Converter

The following sub chapters provide descriptions of the blocks implemented to control the output voltage. The regulation principle provides an adaptive operation frequency of typ. up to 1.3MHz, depending on V_{VIN} / V_{VDD1} voltage ratio and load conditions.

PFM Control Logic

PFM control logic generates the timings necessary to control the converter based on a combination of output voltage, temperature and measured switch current. It provides adaptive frequency, depending on input voltage to output voltage ratio in the range of 0Hz up to typ. >1.3MHz.

Internal Power Switch

The internal highside power switch connects **VIN** and **LXT** controlled by PFM control logic.

The highside power switch current is limited providing saturation protection to the inductor and to prevent over current damage to the application. It allows startup of the converter without soft-start measures.

5.10.3 Application / Implementation Hints

Output voltage ripple is strongly dependent on peripheral elements chosen (L_{LXT} and $C_{VDD1SENSE}$) and their parasitic behavior. ESR of output capacitance $C_{VDD1SENSE}$ must be suitable to ensure a small ripple for proper regulation (see recommended operating conditions). The ripple voltage can be calculated by

$V_{RIPPLE,VDD1SENSE} = R_{ESR,COUT} * I_{RIPPLE,L\_LXT}$

The DC resistance of L_{LXT} reduces the efficiency but does not affect the output voltage ripple. (Though a high resistance can generate a significant thermal power within the inductor). Furthermore higher DC resistance will also increase the minimum input voltage requirements for nominal output voltage.

The free-wheeling diode must have a low forward voltage as well as a low reverse recovery time. Parasitic capacitance of this diode decreases the overall efficiency and causes current spikes when the driver turns on (consider this behaviour for EMI).

For low power requirements on VDD1 consider the leakage of the freewheeling diode at nominal converter output voltage. Leakage current will contribute to the overall output current of the converter.

A reverse polarity diode for VIN is recommended. In EMC sensitive environments additional decoupling measures at VIN are recommended.

5.10.4 VDD1 under-voltage monitor

If **VDD1** < $V_{THx,VDD1\_f,RSTN}$ a reset is generated and pin **RSTN** is set to L. SBC enters state RESTART or FAILSAFE depending on SBC_CFG.CFG. If **VDD1** > $V_{THx,VDD1,RSTN}$ reset will be enlarged and **RSTN** will be held L for $t_{RSTN,VDD1}$. After that **RSTN** is set to H.
To prevent high or short current events **VDD1** is monitored. If **VDD1** < $V_{THx,VDD1,RSTN}$ timeout $t_{TO,VDD1}$ is started. If timeout exceeds SBC is set to state FAILSAFE and regulator is switched off.
If **VDD1** > $V_{THx,VDD1,RSTN}$ timeout is reset.
Timeout is enabled only if **VS** > $V_{ON-OFF,VS}$. Otherwise **VDD1** will not reach its output value.

5.11 Low drop regulator; pins VDD2, ENVDD2

The on chip low drop voltage regulator (LDO) provides a voltage of typically 5.0V at pin **VDD2**. LDO can be active in SBC operating states NORMAL, STOP, SLEEP, RESTART or FAILSAFE. It can be activated via SPI or via pin **ENVDD2**. **VS** related pin **ENVDD2** has higher priority. In order to save system current **ENVDD2** does not implement pull down functionality.

If the external pin **ENVDD2** is low the SPI register determines status of LDO. Otherwise if the pin **ENVDD2** is high the LDO is activated independently of the contents of the register VDD2_CFG.ON. In case of external deactivation of **VDD2** using pin **ENVDD2** LDO is switched off as well as SPI register is reset to off state. Register VDD2_CFG can be written in state NORMAL only. It is cleared in state FAILSAFE. The LDO is limited in output current. Current limitation is always activated. Over voltage protection against VS and reverse polarity protection are implemented. An over temperature protection using both warning and shutdown levels is implemented. In case of over temperature detection an interrupt is generated. Voltage supervision including interrupt generation is implemented.

Register Name	Address	Description
VDD2_CFG	0x18	VDD2 configuration register

Table 78: VDD2 RegisterTable

Register **VDD2_CFG** (0x18)

	MSB							LSB
Content	-	-	-	-	-	-	-	ON
Reset value	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W
Bit Description	**ON** : 1... enables regulator							

Table 79: VDD2 configuration register

5.12 DCDC Boost converter; pins MDRV, ISEN, PGND2

For applications relevant during startup, an optional input voltage boost converter can be added. The boost converter activates if the supply voltage at pin VS falls below the V_{BOOST} level. Then the gate driver sets active level on pin MDRV driving the gate of external power-MOS-switch for either maximum ON-time T_{ONMAX4} or till the current reaches the threshold V_{ISEN} sensing on shunt at pin ISEN. After switching off at pin MDRV the next switch on will be only after expiration minimum OFF-time $T_{OFFMIN4}$. Each switch on event holds the pin MDRV active at least for the minimum ON-time T_{ONMIN4} regardless of current sense level at pin ISEN. So the boost converter is self oscillating. It can also be deactivated if pin ISEN is not connected to external Rsense and externally pulled up between 2V and VDD1 level.

Booster activation is controlled using SBC_CFG.BOOST. In default setup booster set to off.

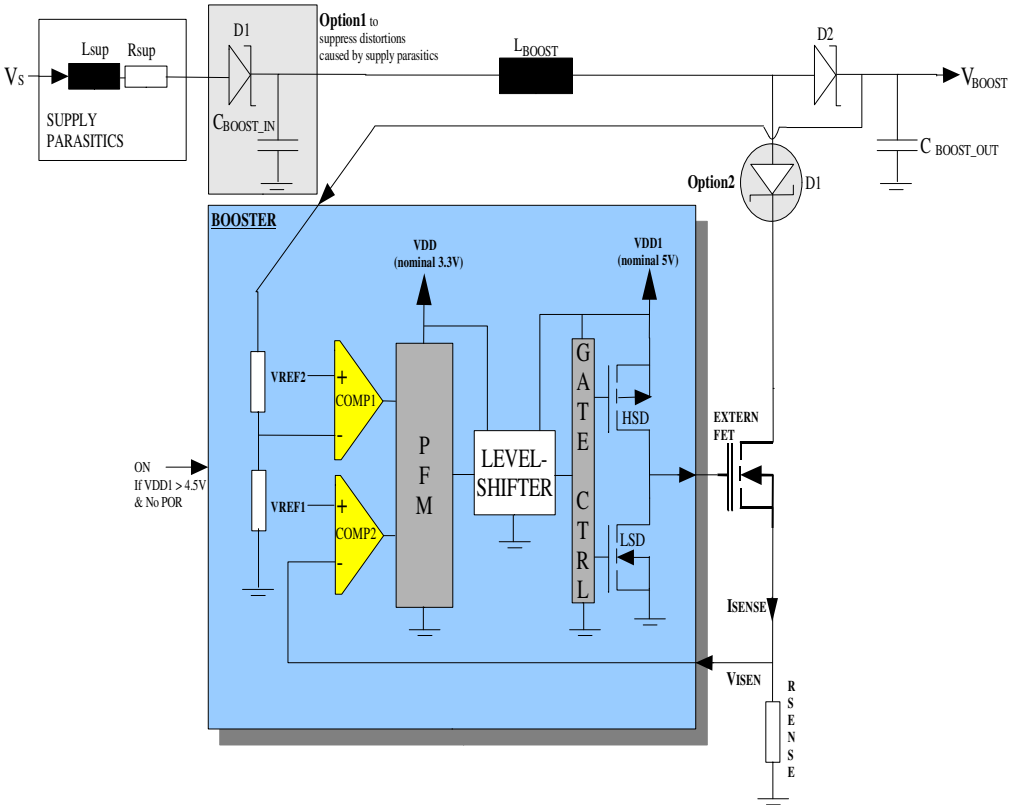


Fig. 25: Functional diagram Booster

6 Register Table

Register Name	Address	Description
SBC_CFG	0x01	SBC configuration register.
FSON_STAT	0x02	FSON status register.
INT	0x03	Interrupt status register
WU_SRC	0x04	Wake up source register. Wake up source is cleared if register is read.
SPI_FAIL	0x05	SPI programming failure register. Register is cleared by reading via SPI.
LIN_CFG	0x06	Shortcut to LIN1-4 TR and RC configuration bits
WD_CFG	0x08	Current watchdog configuration. Change of configuration has to be performed using WD_CFG1 and WD_CFG2 including correct watchdog trigger afterwards within one watchdog cycle in SBC mode NORMAL
WD_CFG1	0x09	Watchdog configuration register 1
WD_CFG2	0x0A	Watchdog configuration register 2
WD_STAT	0x0B	watchdog status register
WD_PER	0x0C	Current watchdog period. Change of period has to be performed using WD_PER1 and WD_PER2 including correct watchdog trigger afterwards within one watchdog cycle.
WD_TRIG	0x0D	watchdog trigger register
WD_PER1	0x0E	Watchdog period register 1
WD_PER2	0x0F	Watchdog period register 2.
WK_CFG	0x10	configuration register of pin **WK.** Register is writeable in SBC state NORMAL only. In SBC states INIT, RESTART or FAILSAFE all bits are set to H.
VDD1_CFG	0x14	VDD1 configuration register. Writing register in SBC state FAILSAFE is not allowed
VDD2_CFG	0x18	VDD2 configuration register
VDD_STAT	0x1A	VDD1, VDD2 and VDDCAN status information.
SPI_STAT	0x1B	Status register with respect to FSM.
OT_STAT	0x1F	Over temperature detection status register.
LIN1_CFG	0x20	Configuration register for LIN1
LIN_INT	0x21	LIN interrupt register
LIN1_STAT	0x22	Status register for LIN1
LIN2_CFG	0x24	Configuration register for LIN2
LIN2_STAT	0x26	Status register for LIN2
LIN3_CFG	0x28	Configuration register for LIN3
LIN3_STAT	0x2A	Status register for LIN3
LIN4_CFG	0x2C	Configuration register for LIN4
LIN4_STAT	0x2E	Status register for LIN4
CAN_CFG	0x30	Configuration register for CAN
CAN_STAT	0x32	Status register for CAN

Table 80: Register Table

7 Applications Information

7.1 Overview

The device E521.02 .. E521.04 is used in application without pre-booster, while E521.12 .. E521.14 supports pre-boost functionality. The following chapters show typical operating circuits of these two use cases.

7.2 Typical Operating Circuit with booster

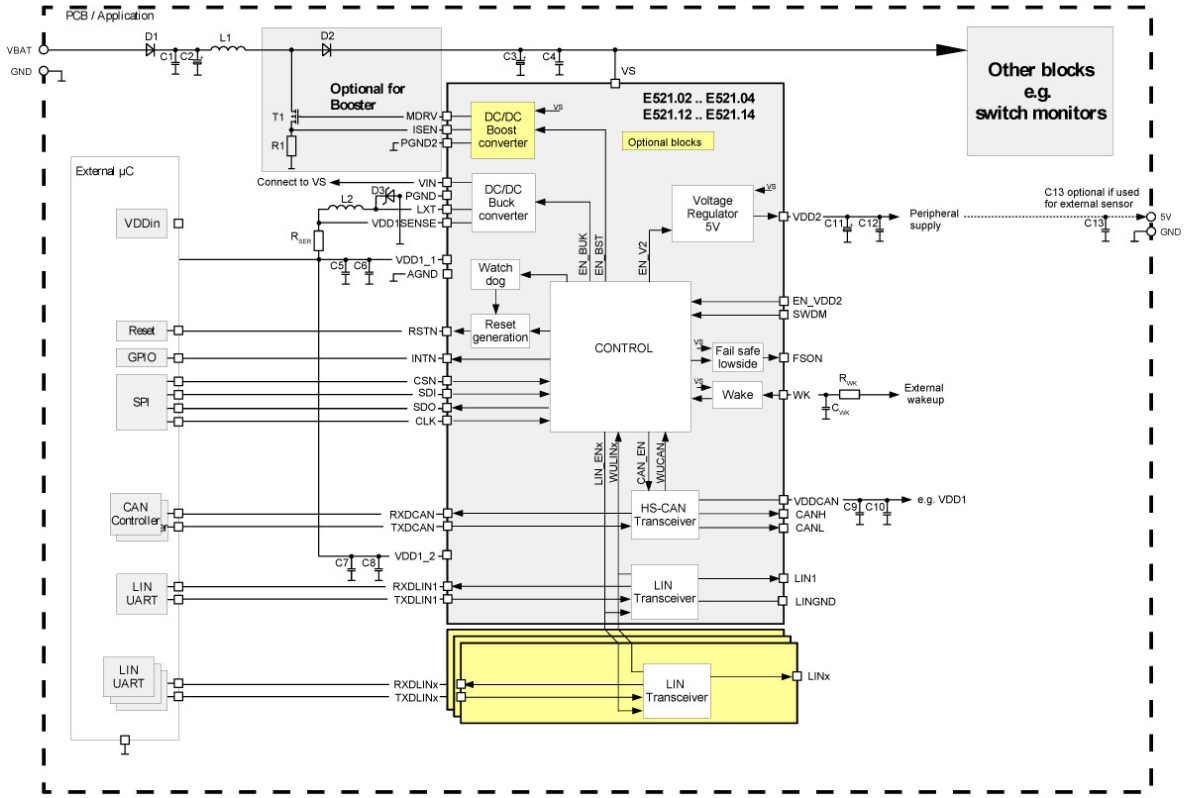


Table 81. External Components

Description	Condition	Symbol	Min	Typ	Max	Unit
Battery supply input pins						
Battery filter capacitor to ground		C_1		100		nF
Battery buffer capacitor to ground		C_2		47		µF
EMC filter inductor	Saturation current relative to maximum application current I_{VDD1}	L_1		2.2		µH

Description	Condition	Symbol	Min	Typ	Max	Unit
VS, VIN buffer capacitance to ground	Effective ESR of C_3, C_4 shall be < 300mΩ	C_3	10	22	-	µF
VS, VIN filter capacitance to ground	Effective ESR of C_3, C_4 shall be < 300mΩ	C_4		100		nF
WK						
Optional LP filter capacitance for WK		C_{WK}		22		nF
LP filter resistor for pin WK		R_{WK}	1	3.3	10	kΩ
VDD1						
Inductance at LXT to output voltage	I_{VDD1} < 500mA	L_2	18	33	82	µH
Serial Resistance of LXT Inductance	I_{VDD1} < 500mA	R_{L2}		0.1	0.6	Ω
Relative Saturation Current of LXT Inductor	Saturation current relative to maximum application current I_{VDD1}	$I_{L2,SAT}$	130			%
Freewheeling Diode Forward Voltage e.g. MBR	Forward current 1.3 x I(VDD1) T_{AMB} = 25°C	V_{D2}		0.6	1	V
Reverse Recovery Time of Freewheeling Diode	Forward current 1.3 x I(VDD1) T_{AMB} = 25°C	$t_{D2,rec}$		10	25	ns
Peak to peak voltage ripple at VDD1SENSE for regulation, regulation ripple included in 2% tolerance window for VDD1		$V_{VDD1SENSE,RIPPLE}$	10		100	mV
VDD1SENSE Decoupling resistor		R_{SER}	50	60	140	mΩ
VDD1_1 external buffer capacitor	Effective ESR of C_5, C_6, C_7, C_8 shall be < 10mΩ	C_5		10		µF
VDD1_1 external filter capacitor	Effective ESR of C_5, C_6, C_7, C_8 shall be < 10mΩ	C_6		33		nF
VDD1_2 external buffer capacitor	Effective ESR of C_5, C_6, C_7, C_8 shall be < 10mΩ	C_7		10		µF
VDD1_2 external filter capacitor	Effective ESR of C_5, C_6, C_7, C_8 shall be < 10mΩ	C_8		33		nF
VDDCAN						
VDDCAN external buffer capacitor	ESR < TBD	C_9		10		µF
VDDCAN external filter capacitor	ESR < TBD	C_{10}		33		nF

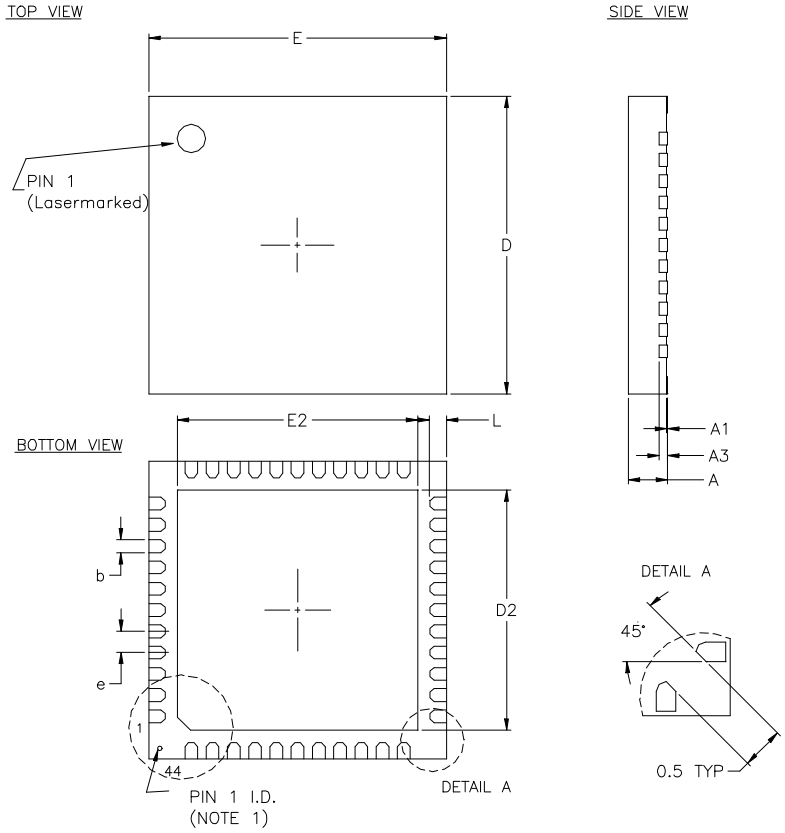
Description	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
VDD2						
External buffer capacitor for VDD2	ESR > 200mΩ	C_{11}	2.2		22	µF
External filter capacitor	close to pin VDD2	C_{12}		100		nF
External filter capacitor	close to external connector if used as external sensor supply (global pin)	C_{13}		4.7		nF
Booster (optional)						
Booster inductance	I_{sat} depends on R_{sense} selection	L_1		2.2		µH
Booster diode, e.g. SS24		D_2				
Booster input buffer capacitance		C_2	50	100	-	µF
Booster input filter capacitance		C_1		TBD		nF
Booster output buffer capacitance	I_{LOAD_VS} < 600mA ESR < 50mΩ	C_3	50		-	µF
Booster output filter capacitance		C_4		TBD		nF
Current sense resistance	I_{sat_Lboost} > 1.8A	R_{1_60}		60		mΩ
Current sense resistance	I_{sat_Lboost} > 3.6A	R_{1_30}		30		mΩ
RDSon of the external FET	V_{VDD1} > 4.5V	$R_{DSON,T1}$			30	mΩ
Total gate charge of the external FET	V_{DS} = 5V V_{GS} = 5V I_D = 3.6A V_{th} < 3V	$Qb_{BOOST\_ext\_FET}$			10	nC
Maximal forward current of the external Booster diode D1, D2		$I_{AV(SKD\_BOOST)}$	3.6			A
Maximal forward voltage of the external Booster diode D1, D2 @ 3.6A		$V_{F(SKD\_BOOST)}$			500	mV

8 Package Information

The E521.14 device family is available in a Pb free, RoHs compliant, QFN44L7 plastic package according to JEDEC MO-220 K.01 VKKD-3.

The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020C with a soldering peak temperature of (260+5)°C.

Note: Thermal resistance junction to ambient $R_{th,ja}$ is typ. 24 °C/W, based on JEDEC standard JESD-51-2, JESD-51-5 and JESD-51-7.



Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand off	A1	0.00	0.02	0.05	0.000	0.00079	0.002
Thickness of terminal leads, including lead finish	A3	--	0.20 REF	--	--	0.0079 REF	--
Width of terminal leads	b	0.18	0.25	0.30	0.007	0.010	0.012
Package length / width	D / E	--	7.00 BSC	--	--	0.276 BSC	--
Length / width of exposed pad	D2 / E2	5.50	5.65	5.80	0.217	0.223	0.229
Lead pitch	e	--	0.5 BSC	--	--	0.020 BSC	--
Length of terminal for soldering to substrate	L	0.35	0.40	0.45	0.014	0.016	0.018
Number of terminal positions	N		44			44	

Note: the mm values are valid, the inch values contains rounding errors

WARNING – Life Support Applications Policy

Elmos Semiconductor AG is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing Elmos Semiconductor AG products, to observe standards of safety, and to avoid situations in which malfunction or failure of an Elmos Semiconductor AG Product could cause loss of human life, body injury or damage to property. In development your designs, please ensure that Elmos Semiconductor AG products are used within specified operating ranges as set forth in the most recent product specifications.

General Disclaimer

Information furnished by Elmos Semiconductor AG is believed to be accurate and reliable. However, no responsibility is assumed by Elmos Semiconductor AG for its use, nor for any infringements of patents or other rights of third parties, which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Elmos Semiconductor AG. Elmos Semiconductor AG reserves the right to make changes to this document or the products contained therein without prior notice, to improve performance, reliability, or manufacturability .

Application Disclaimer

Circuit diagrams may contain components not manufactured by Elmos Semiconductor AG, which are included as means of illustrating typical applications. Consequently, complete information sufficient for construction purposes is not necessarily given. The information in the application examples has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of Elmos Semiconductor AG or others.

Contact Information

Headquarters
Elmos Semiconductor AG
Heinrich-Hertz-Str. 1 • D-44227 Dortmund (Germany) ☏: +492317549100 ✉: sales-germany@elmos.com : www.elmos.com

Sales and Application Support Office North America
Elmos NA. Inc.
32255 Northwestern Highway • Suite 220 Farmington Hills
MI 48334 (USA) ☏: +12488653200 ✉: sales-usa@elmos.com

Sales and Application Support Office China
Elmos Semiconductor Technology (Shanghai) Co., Ltd.
Unit 16B, 16F Zhao Feng World Trade Building,
No. 369 Jiang Su Road, Chang Ning District,
Shanghai, PR China, 200050 ☏: +86216210 0908 ✉: sales-china@elmos.com

Sales and Application Support Office Korea
Elmos Korea
B-1007, U-Space 2, #670 Daewangpangyo-ro,
Sampyoung-dong, Bunddang-gu, Sungnam-si
Kyounggi-do 463-400 Korea ☏: +82317141131 ✉: sales-korea@elmos.com

Sales and Application Support Office Japan
Elmos Japan K.K.
BR Shibaura N Bldg. 7F
3-20-9 Shibaura, Minato-ku,
Tokyo 108-0023 Japan ☏: +81334517101 ✉: sales-japan@elmos.com

Sales and Application Support Office Singapore
Elmos Semiconductor Singapore Pte Ltd.
3A International Business Park
#09-13 ICON@IBP • 609935 Singapore ☏: +65 6908 1261 ✉: sales-singapore@elmos.com