

PRELIMINARY - July 26, 2000

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

## DESCRIPTION

The SC1534 is designed to maintain a glitch-free 3.3V output when at least one of two inputs, 5V (VIN) and 3.3V (VAUX), is present.

Whenever VIN exceeds a predetermined threshold value, the internal 3.3V linear regulator is enabled, and DR is pulled high.

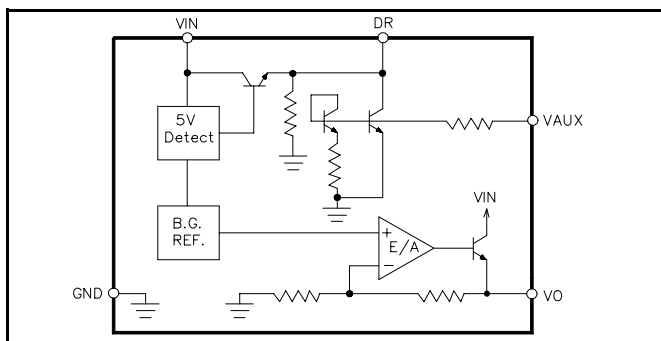
When VIN falls below a lower threshold value, DR is pulled low and the internal linear regulator is turned off. DR has been designed to drive the gate of an external low threshold P-channel MOSFET, which can be used to connect the 3.3V supply directly to the regulator output. This ensures an uninterrupted 3.3V output even if VIN falls out of specification. A maximum  $R_{DS(ON)}$  of 200mΩ is recommended.

When both supplies are simultaneously available, the drive pin (DR) will be pulled High, turning off the external PMOS switch.

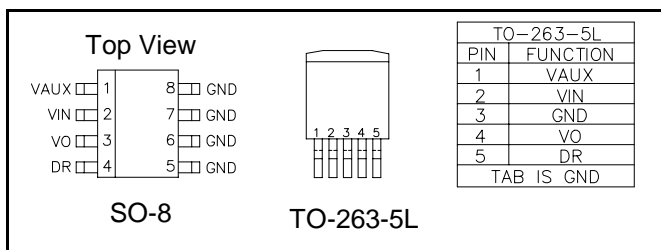
The internal 5V detector has its upper threshold (for VIN rising) set to 4.22V (typical) while the lower threshold (for VIN falling) is at 4.05V (typical) giving a hysteresis of approximately 170mV.

The SC1534 is available in the popular SO-8 and 5-lead TO-263 surface mount packages.

## BLOCK DIAGRAM



## PIN CONFIGURATION



## FEATURES

- Glitch-free transition between input sources
- Internal logic selects input source
- Gate drive for external PMOS bypass switch
- 5V detector with hysteresis
- 1% regulated output voltage accuracy
- 400mA load current capability
- SO-8 and TO-263 packages

## APPLICATIONS

- Desktop Computers
- Network Interface Cards (NICs)
- PCMCIA/PCI Interface Cards
- Cardbus™ Technology
- Power supplies with multiple input sources

## ORDERING INFORMATION

Part Number <sup>(1)</sup>	Package
SC1534CM.TR	TO-263-5L
SC1534CS.TR	SO-8

Note:

(1) Only available in tape and reel packaging.

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Maximum	Units
Input Supply Voltage	VIN	-0.5 to +7	V
Auxiliary Supply Voltage	VAUX	-0.5 to +7	V
LDO Output Current	$I_O$	10 to 400	mA
Operating Ambient Temperature Range	$T_A$	-5 to +70	°C
Operating Junction Temperature Range	$T_J$	-5 to +125	°C
Storage Temperature Range	$T_{STG}$	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec	$T_{LEAD}$	300	°C
Thermal Impedance Junction to Ambient SO-8 <sup>(1)</sup>	$\theta_{JA}$	65	°C/W
TO-263		60	
Thermal Impedance Junction to Case SO-8	$\theta_{JC}$	39	°C/W
TO-263		3	
ESD Rating	ESD	2	kV

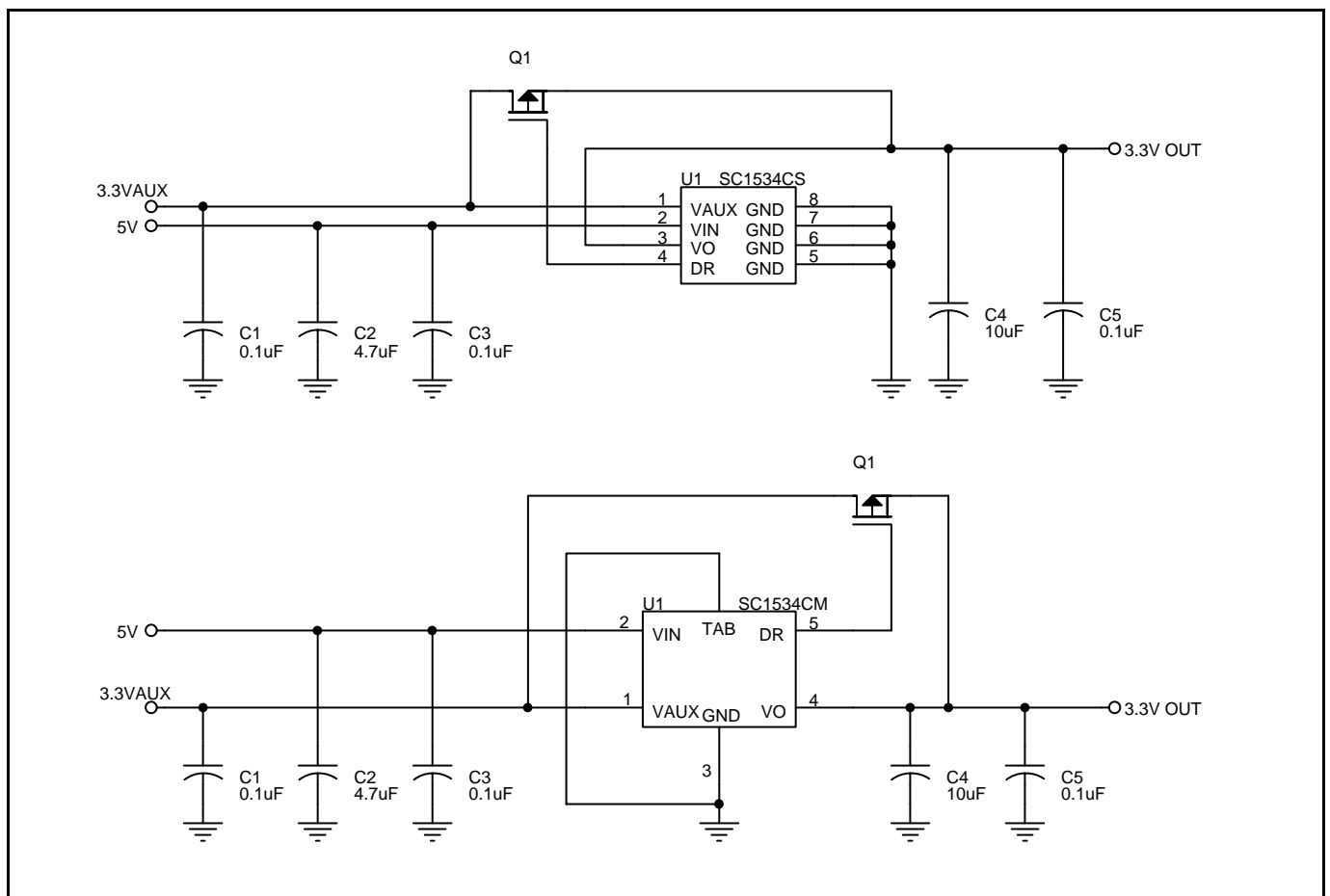
Note:

(1) 1 inch square of 1/16" FR-4, double sided, 1 oz. minimum copper weight.

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**PIN DESCRIPTION**

Pin Name	SO-8 Pin #	TO-263-5L Pin #	Pin Function
DR	4	5	Driver output for external P-channel MOSFET pass element.
GND	5,6,7,8	3/TAB	Logic and power ground.
VAUX	1	1	This is the auxiliary input supply, nominally 3.3V.
VIN	2	2	This is the main input supply for the IC, nominally 5V.
VO	3	4	LDO 3.3V output.

**APPLICATION CIRCUIT**

**NOTE:**

(1) External switch (Q1): use a low threshold P-channel MOSFET such as Fairchild FDN338P or International Rectifier IRF7604, or equivalent. (PMOS, typical gate threshold voltage  $\approx 1V$ ,  $R_{DS(ON)} < 200m\Omega$  at  $V_{GS} = 2.7V$ ).

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**ELECTRICAL CHARACTERISTICS**

 Unless specified,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $V_{AUX} = 3.3\text{V}$ ,  $I_O = 400\text{mA}$ ,  $C_O = 10\mu\text{F}$ . Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
<b>VIN</b>						
Supply Voltage	VIN	VAUX = 0V	<b>4.35</b>	<b>5.00</b>	<b>5.50</b>	V
Quiescent Current	IQ	VIN = 5V, VAUX = 0V, IO = 0mA		8.0	11.0	mA
				<b>13.0</b>		
Reverse Leakage From VAUX	IVIN	VIN = 5V, VAUX = 3.3V, IO = 0mA		10.0	14.0	mA
				<b>15.0</b>		
Reverse Leakage From VAUX	IVIN	VAUX = 3.6V, VIN = 0V, IO = 0mA		-1.5	-3.0	mA
				<b>-4.0</b>		
<b>VAUX</b>						
Supply Voltage	VAUX		<b>3.0</b>	<b>3.3</b>	<b>3.6</b>	V
Quiescent Current	IQ(AUX)	VAUX = 3.3V, VIN = 0V, IO = 0mA		8.0	11.0	mA
				<b>13.0</b>		
Reverse Leakage From VIN	IVAUX	VAUX = 3.3V, VIN = 5V, IO = 0mA		1.5	2.5	mA
				<b>3.0</b>		
Reverse Leakage From VIN	IVAUX	VIN = 5.5V, VAUX = 0V, IO = 0mA		-5.0	-50.0	$\mu\text{A}$
				<b>-100.0</b>		
<b>5V Detect<sup>(1)(2)(3)</sup></b>						
Low Threshold Voltage	VTH(LO)	VIN Falling, IO = 20mA	3.92	4.05	4.18	V
			<b>3.90</b>		<b>4.20</b>	
Hysteresis	VHYST		90	170		mV
			<b>80</b>			
High Threshold Voltage	VTH(HI)	VIN Rising, IO = 20mA			<b>4.35</b>	V
<b>VO</b>						
LDO Output Voltage	VO	IO = 20mA	3.267	3.300	3.333	V
		$4.35\text{V} \leq V_{IN} \leq 5.5\text{V}$ , $0\text{mA} \leq I_O \leq 400\text{mA}$	<b>3.234</b>		<b>3.366</b>	
Output Current	IO				<b>400</b>	mA
Line Regulation	REG(LINE)	VIN = 4.35V to 5.5V		0.20	0.60	%
					<b>0.80</b>	
Load Regulation	REG(LOAD)	IO = 20mA to 400mA		0.20	0.80	%
					<b>1.00</b>	

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**ELECTRICAL CHARACTERISTICS**

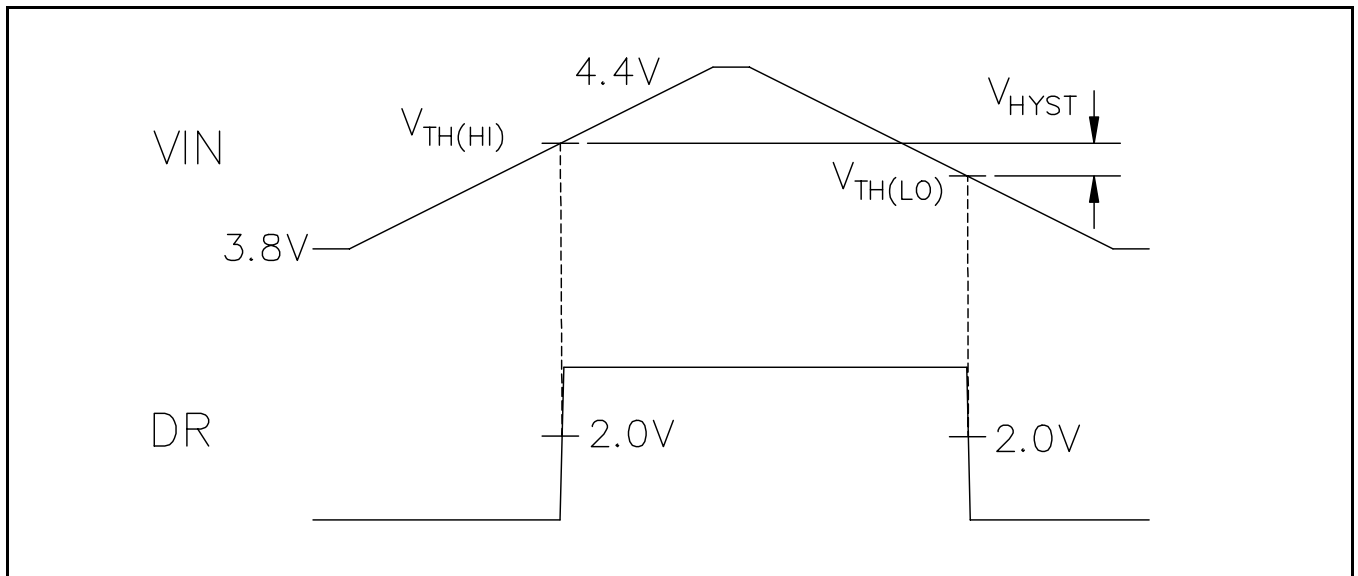
 Unless specified,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $V_{AUX} = 3.3\text{V}$ ,  $I_O = 400\text{mA}$ ,  $C_O = 10\mu\text{F}$ . Values in **bold** apply over full operating temperature range.

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Units
<b>Drive Output</b>						
Drive Voltage	$V_{DR}$	$4.35\text{V} \leq V_{IN} \leq 5.5\text{V}$ , $I_{DR} = 200\mu\text{A}$	3.4	$V_{IN} - 0.8$		V
			<b>3.3</b>			
		$V_{IN} < V_{TH(LO)}$ , $I_{DR} = -200\mu\text{A}$		35	150	mV
					<b>250</b>	
Peak Drive Current	$I_{DR(PK)}$	Sinking: $V_{IN} = 3.9\text{V}$ , $V_{DR} = 1\text{V}$ ; Sourcing: $V_{IN} = 4.35\text{V}$ , $V_{IN} - V_{DR} = 2.5\text{V}$	7			mA
			<b>6</b>			
Drive High Delay <sup>(1)(4)</sup>	$t_{DH}$	$C_{DR} = 1.2\text{nF}$ , $V_{IN}$ ramping up, measured from $V_{IN} = V_{TH(HI)}$ to $V_{DR} = 2\text{V}$		0.5	1.0	$\mu\text{s}$
					<b>2.0</b>	
Drive Low Delay <sup>(1)(4)</sup>	$t_{DL}$	$C_{DR} = 1.2\text{nF}$ , $V_{IN}$ ramping down, measured from $V_{IN} = V_{TH(LO)}$ to $V_{DR} = 2\text{V}$		0.5	1.0	$\mu\text{s}$
					<b>2.0</b>	

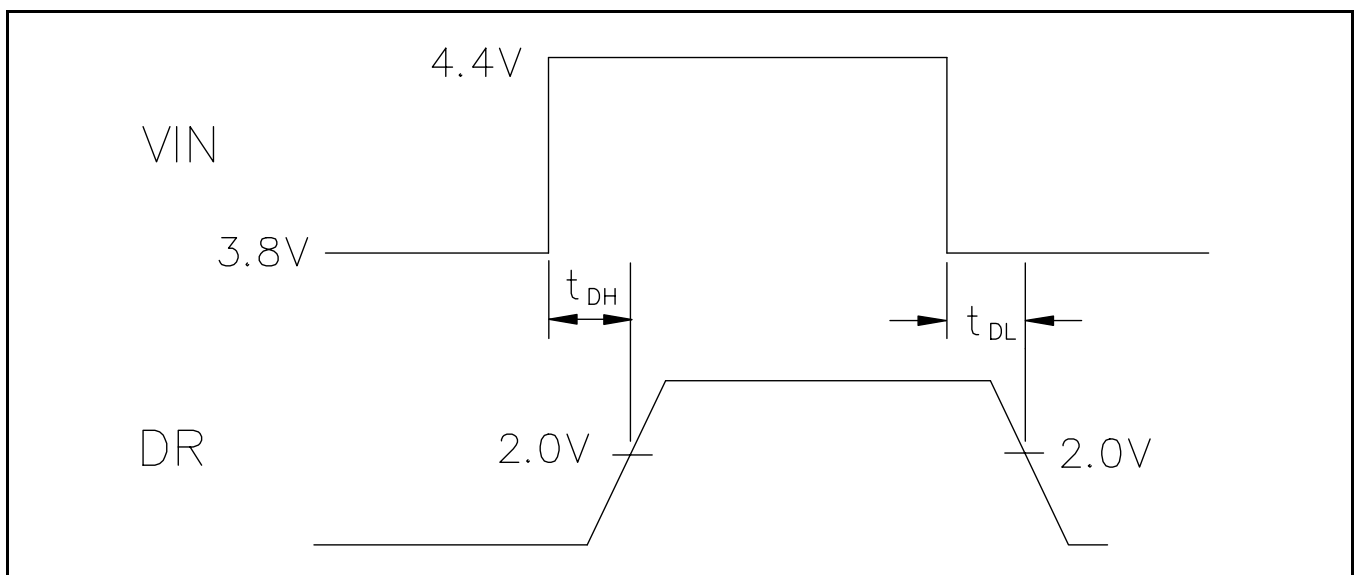
**NOTES:**

- (1) Guaranteed by design.
- (2) See 5V Detect Thresholds on page 5.
- (3) Recommended source impedance for 5V supply:  $\leq 0.125\Omega$ . This will ensure that  $I_O \times R_{SOURCE} < V_{HYST}$ , thus avoiding DR toggling during 5V detect threshold transitions.
- (4) See Timing Diagram on page 5.

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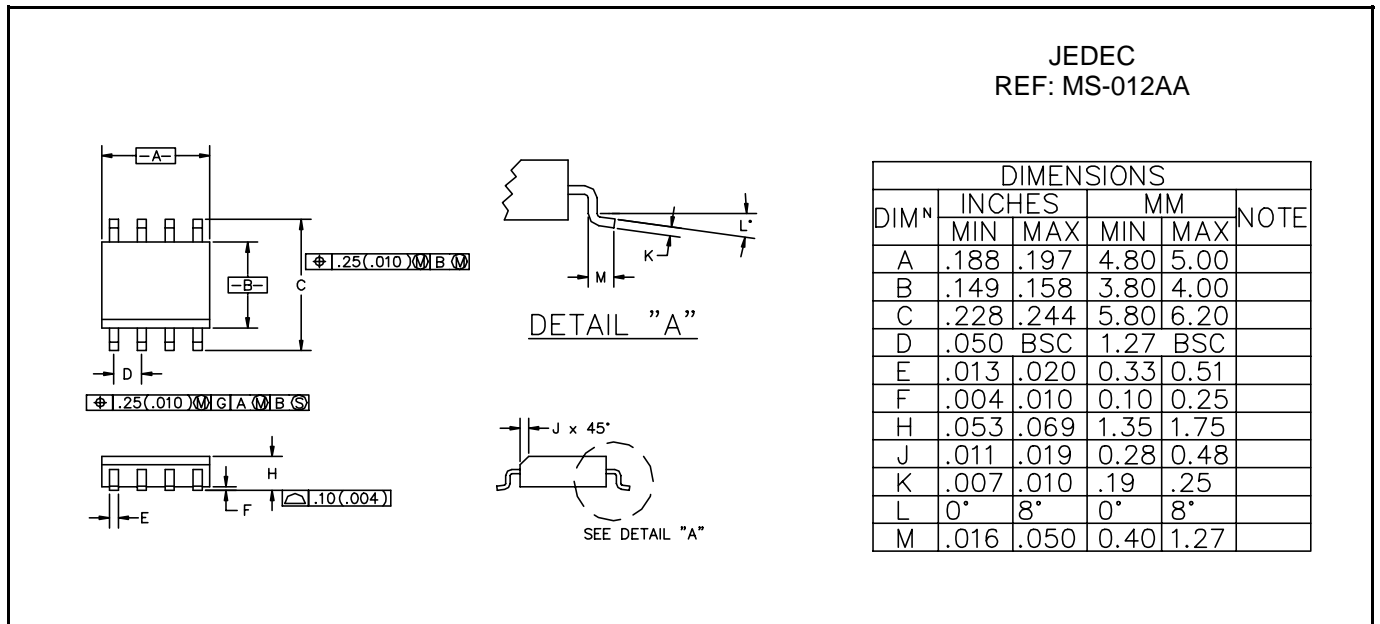
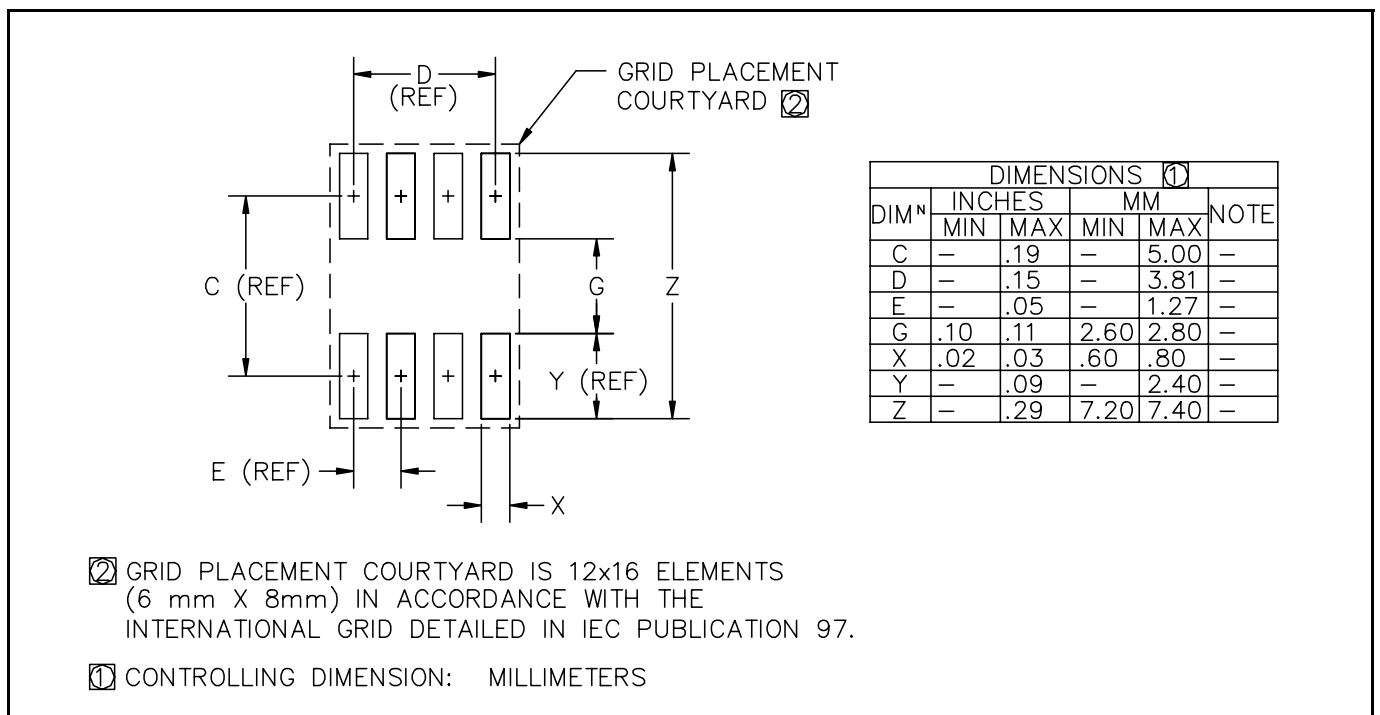
**5V DETECT THRESHOLDS**

**NOTE:**

 (1) VIN rise and fall times (10% to 90%) to be  $\geq 100\mu s$ .

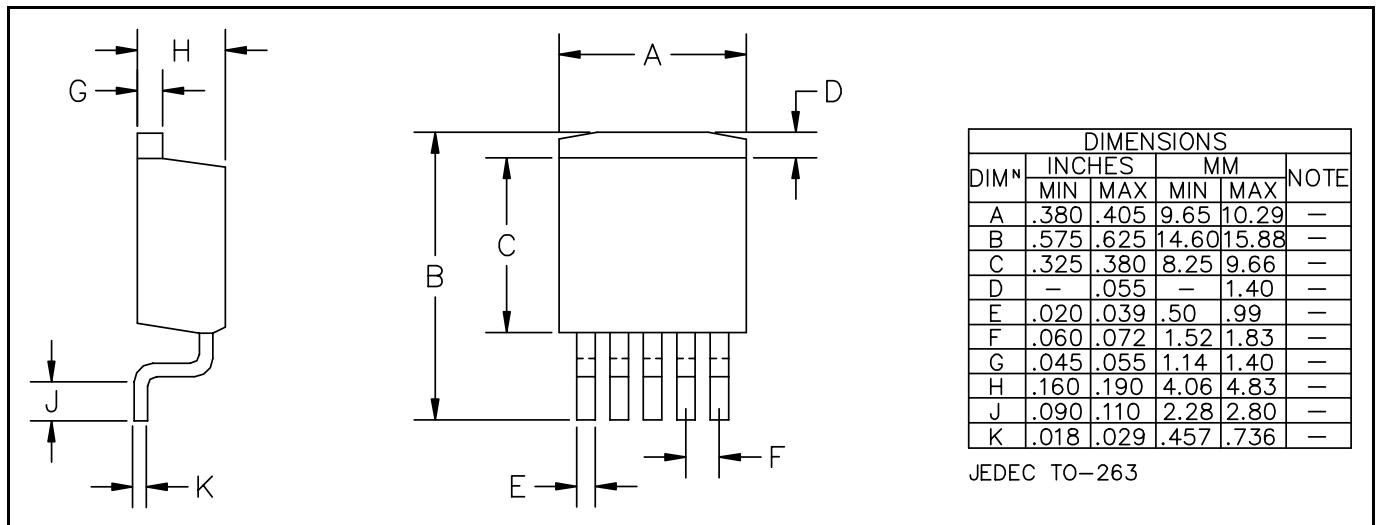
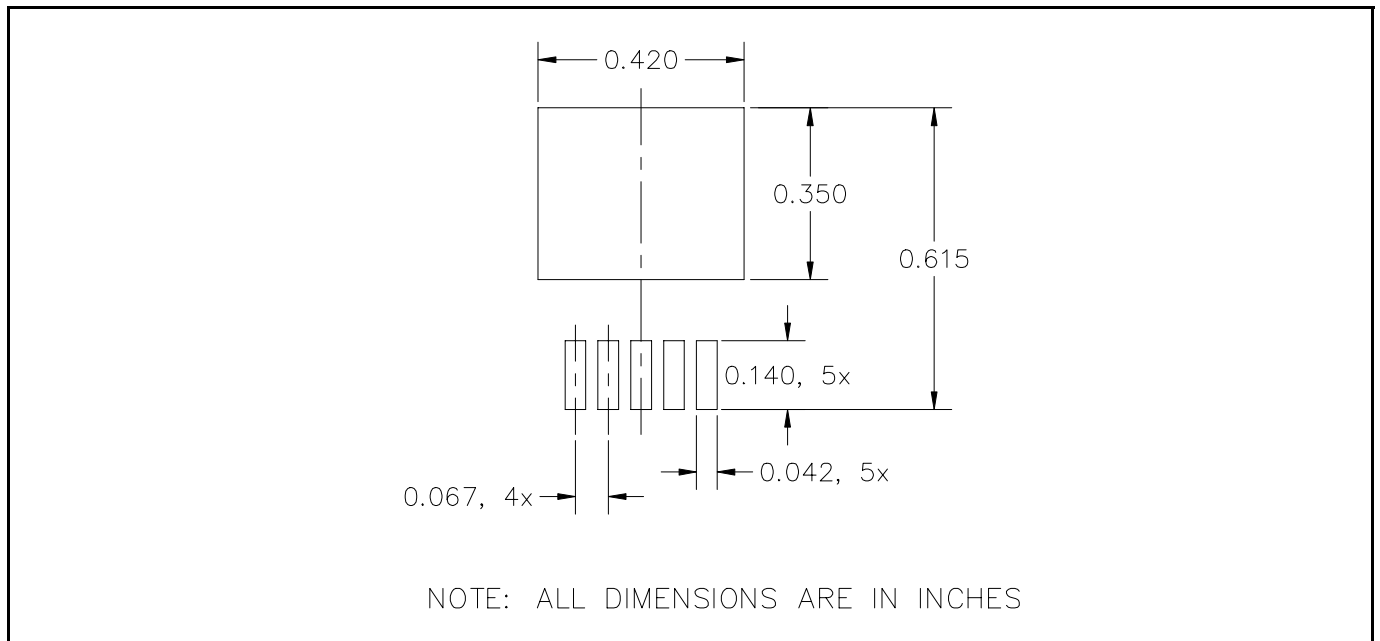
**TIMING DIAGRAM**

**NOTE:**

 (1) VIN rise and fall times (10% to 90%) to be  $\leq 100ns$ .

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**OUTLINE DRAWING - SO-8**

**MINIMUM LAND PATTERN - SO-8**


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**DEVICE OUTLINE - TO-263, 5 PIN**

**MINIMUM LAND PATTERN - TO-263, 5 PIN**


ECN00-1212