# MAX11190

# 4-Channel, Dual, Simultaneous Sampling, 2.2V to 3.6V, 12-Bit, 3Msps SAR ADC in Tiny 3mm x 3mm TQFN Package

## General Description

The MAX11190 is a 4-channel, dual, multiplexed, 12-bit, compact, high-speed, low-power, successive approximation analog-to-digital converter (ADC). This high-performance dual ADC includes high-dynamic range sample-and-holds and a high-speed serial interface. This ADC accepts a full-scale input from 0V to the reference voltage.

The device features two dual, single-ended analog inputs connected to two ADC cores using 2:1 MUXs. The device also includes a separate supply input for data interface and dedicated inputs for reference voltage.

This device operates from a 2.2V to 3.6V supply and consumes only 10.5mW at 3Msps. The device includes full power-down mode and fast wake-up for optimal power management and a high-speed 3-wire serial interface. The 3-wire serial interface directly connects to SPI, QSPI™, and MICROWIRE® devices without external logic. Each of the two internal ADCs has its own dedicated DOUTA/DOUTB for faster data communication.

Excellent dynamic performance, low voltage, low power, ease of use, and small package size make this converter ideal for simultaneous data-acquisition applications, and for other applications that demand low power consumption and minimal space.

The device is available in a 3mm x 3mm, 16-pin TQFN package and operates over the -40ºC to +125ºC temperature range.

## Applications

- Motor Control
- Simultaneous Data Acquisition
- Medical Instrumentation
- Process Control

***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX11190.related.*

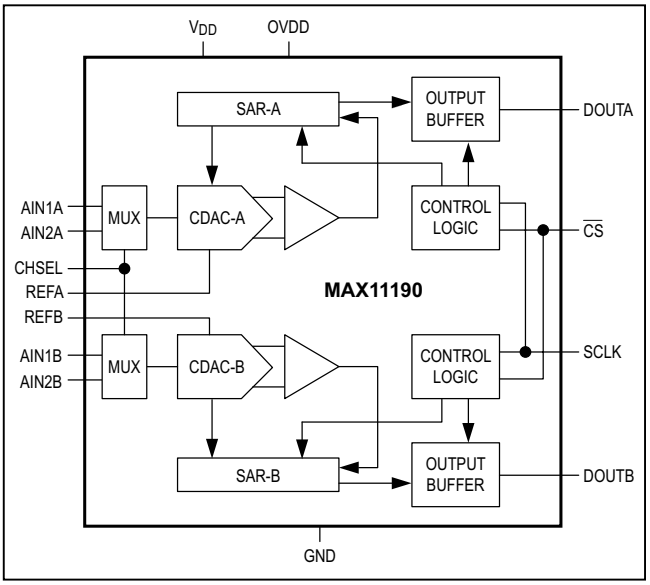
*QSPI is a trademark of Motorola, Inc.*

*MICROWIRE is a registered trademark of National Semiconductor Corporation*

## Benefits and Features

- Integration and Packaging Save Space
  - Simultaneous Sampling
  - Dual, 4-Channel, Single-Ended 12-Bit Resolution ADC (2 x 2)
  - 16-Pin, 3mm x 3mm TQFN Package
- Excellent Performance Ideal for Motor Control Applications
  - 72dB SNR
  - 3Msps Conversion Rate without Pipeline Delay
  - External Reference Inputs
  - Wide -40°C to +125°C Operation
- Low Power Design Simplifies Power-Supply Requirements
  - Very Low Power Consumption at 5µA/ksps
  - 10.5mW at 3Msps
  - 2.2V to 3.6V Supply Voltage
  - 2.6µA Power-Down Current
- Dual SPI Ports Simplifies System Design
  - SPI-/QSPI-/MICROWIRE-Compatible Serial Interface with Two DOUTA/DOUTB Pins
  - Dedicated Digital Output Supply Allows Serial Interface to Directly Connect to 1.5V, 1.8V, 2.5V, or 3V Digital Systems

## Functional Diagram




*19-6743; Rev 2; 12/14*

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## Absolute Maximum Ratings

$V_{DD}$ to GND .....-0.3V to +4V
AIN1A, AIN2A to GND....-0.3V to the lower of ($V_{DD}$ + 0.3V) and +4.0V
REFA, OVDD to GND ....-0.3V to the lower of ($V_{DD}$ + 0.3V) and +4.0V
AIN1B, AIN2B to GND....-0.3V to the lower of ($V_{DD}$ + 0.3V) and +4.0V
REFB to GND.....-0.3V to the lower of ($V_{DD}$ + 0.3V) and +4.0V
$\overline{CS}$, SCLK to GND..... -0.3V to the lower of ($V_{OVDD}$ + 0.3V) and +4.0V
CHSEL to GND ..... -0.3V to the lower of ($V_{OVDD}$ + 0.3V) and +4.0V
DOUTA to GND..... -0.3V to the lower of ($V_{OVDD}$ + 0.3V) and +4.0V
DOUTB to GND ..... -0.3V to the lower of ($V_{OVDD}$ + 0.3V) and +4.0V

Multilayer Board Max Power Dissipation ($T_A$ = +70ºC)
TQFN (derate 20.8mW/ºC above +70ºC).....1667mW
Operating Temperature Range.....-40ºC to +125ºC
Storage Temperature Range.....-65ºC to +150ºC
Lead Temperature (soldering, 10s) ..... +300ºC
Soldering Temperature (reflow) ..... +260ºC

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .....48°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$).....10°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## Electrical Characteristics

($V_{DD}$ = +2.2V to +3.6V, REFA = REFB = $V_{DD}$, OVDD = $V_{DD}$, unless otherwise noted. $f_{SCLK}$ = 48MHz, 3Msps, 50% duty cycle. Reference pins are independent, $C_{DOUTA/DOUTB}$ = 10pF. $T_A$ = -40ºC to 125ºC, unless otherwise noted. Typical values are at $T_A$ = +25ºC.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC ACCURACY** | | | | | | |
| Resolution | | 12 bit | 12 | | | Bits |
| Integral Nonlinearity | INL | | | | ±1 | LSB |
| Differential Nonlinearity | DNL | No missing codes over temperature | | | ±1 | LSB |
| Offset Error | | | | ±1 | ±4.0 | LSB |
| Gain Error | | Excluding offset and reference errors | | ±1 | ±4.0 | LSB |
| Total Unadjusted Error | TUE | | | ±1.5 | | LSB |
| Channel-to-Channel Offset Matching | | | | ±0.3 | | LSB |
| Channel-to-Channel Gain Matching | | | | ±0.3 | | LSB |
| **DYNAMIC PERFORMANCE** | | | | | | |
| Signal-to-Noise Plus Distortion (Note 3) | SINAD | $f_{IN}$ = 1MHz | 70 | 72 | | dB |
| Signal-to-Noise Ratio | SNR | $f_{IN}$ = 1MHz | 70.5 | 72 | | dB |
| Total Harmonic Distortion | THD | $f_{IN}$ = 1MHz | | -85 | -75 | dB |
| Spurious-Free Dynamic Range | SFDR | $f_{IN}$ = 1MHz | 76 | 85 | | dB |
| Intermodulation Distortion | IMD | $f_{IN1}$ = 1.0003MHz, $f_{IN2}$ = 0.99955MHz | | -84 | | dB |
| Full-Power Bandwidth | | -3dB point | | 40 | | MHz |
| Full-Linear Bandwidth | | SINAD > 68dB | | 2.5 | | MHz |
| Small-Signal Bandwidth | | | | 45 | | MHz |
| Crosstalk | | Channel to channel | | -90 | | dB |



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## Electrical Characteristics (continued)

($V_{DD}$ = +2.2V to +3.6V, REFA = REFB = $V_{DD}$, OVDD = $V_{DD}$, unless otherwise noted. $f_{SCLK}$ = 48MHz, 3Msps, 50% duty cycle. Reference pins are independent, $C_{DOUTA/DOUTB}$ = 10pF. $T_A$ = -40ºC to 125ºC, unless otherwise noted. Typical values are at $T_A$ = +25ºC.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **CONVERSION RATE** | | | | | | |
| Throughput | | 16 cycles | 0.03 | | 3 | Msps |
| Conversion Time | | 13 cycles | 260 | | | ns |
| Acquisition Time | $t_{ACQ}$ | Track time = 2.5 cycles | 52 | | | ns |
| Aperture Delay | | From $\overline{CS}$ falling edge | | 4 | | ns |
| Aperture Delay Matching | | | | 150 | | ps |
| Aperture Jitter | | | | 15 | | ps |
| Serial-Clock Frequency | $f_{CLK}$ | | 0.48 | | 48 | MHz |
| **ANALOG INPUT (AIN1A, AIN2A, AIN1B, and AIN2B)** | | | | | | |
| Input Voltage Range | $V_{INA}$ | AIN1A and AIN2A pins | 0 | | $V_{REFA}$ | V |
| | $V_{INB}$ | AIN1B and AIN2B pins | 0 | | $V_{REFB}$ | V |
| Input Leakage Current | $I_{ILA}$ | | | 0.002 | ±1 | µA |
| Input Capacitance | $C_{AIN_}$ | Track | | 20 | | pF |
| | | Hold | | 4 | | |
| **EXTERNAL REFERENCE (REFA and REFB)** | | | | | | |
| Input Voltage Range | $V_{REFA}$ $V_{REFB}$ | | 1 | | $V_{DD}$ + 0.05 | V |
| Input Leakage Current | $I_{ILR}$ | Conversion stopped | | 0.005 | ±1 | µA |
| Input Capacitance | $C_{REFA}$ $C_{REFB}$ | | | 5 | | pF |
| **DIGITAL INPUTS (SCLK, $\overline{CS}$, CHSEL)** | | | | | | |
| Input High Voltage | $V_{IH}$ | | 0.75 x $V_{OVDD}$ | | | V |
| Input Low Voltage | $V_{IL}$ | | | | 0.25 x $V_{OVDD}$ | V |
| Input Hysteresis | $V_{HYST}$ | | | 0.15 x $V_{OVDD}$ | | %OVDD/ $V_{DD}$ |
| Input Leakage Current | $I_{IL}$ | Inputs at 0V or $V_{OVDD}$ | | 0.001 | ±1 | µA |
| Input Capacitance | $C_{IN}$ | | | 2 | | pF |
| **DIGITAL OUTPUT (DOUTA and DOUTB)** | | | | | | |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$ = 1mA | 0.85 x $V_{OVDD}$ | | | V |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 5mA | | | 0.15 x $V_{OVDD}$ | V |
| Three-State Leakage Current | $I_{OL}$ | | | | ±1.0 | µA |
| Three-State Output Capacitance (Without Pad Metal) | $C_{OUT}$ | | | 5 | | pF |



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## Electrical Characteristics (continued)

($V_{DD}$ = +2.2V to +3.6V, REFA = REFB = $V_{DD}$, OVDD = $V_{DD}$, unless otherwise noted. $f_{SCLK}$ = 48MHz, 3Msps, 50% duty cycle. Reference pins are independent, $C_{DOUTA/DOUTB}$ = 10pF. $T_A$ = -40ºC to 125ºC, unless otherwise noted. Typical values are at $T_A$ = +25ºC.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| Positive Supply Voltage | $V_{DD}$ | $V_{DD}$ pin | 2.2 | | 3.6 | V |
| Digital I/O Supply Voltage | $V_{OVDD}$ | OVDD pin | 1.5 | | $V_{DD}$ | V |
| Power-Down Current | $I_{PD}$ | Leakage only, per supply pin | | 2.6 | 10 | µA |
| Positive Supply Current (Full Power Mode) | $I_{DD}$ | $f_{SAMPLE}$ = 3Msps, $V_{AIN}$ = 0V, both ADCs | | | 6.8 | mA |
| Positive Supply Current (Full Power Mode), No Clock | $I_{DD}$ | $f_{SAMPLE}$ = 3Msps, $V_{DD}$ = +3V, both ADCs | | 3.9 | | mA |
| Line Rejection | PSR | $V_{DD}$ = +2.2V to +3.6V, $V_{REF}$ = 2.2V | | 0.7 | | LSB/V |
| **TIMING CHARACTERISTICS** | | | | | | |
| Quiet Time | $t_Q$ | (Note 4) | 4 | | | ns |
| $\overline{CS}$ Pulse Width | $t_1$ | (Note 4) | 10 | | | ns |
| $\overline{CS}$ Fall to SCLK Setup | $t_2$ | (Note 4) | 5 | | | ns |
| $\overline{CS}$ Falling until DOUTA/DOUTB Three-State Disabled | $t_3$ | (Note 4) | 1 | | | ns |
| Data Access Time After SCLK Falling Edge | $t_4$ | $V_{OVDD}$ = 2.2V to 3.6V | | | 15 | ns |
| | | $V_{OVDD}$ = 1.5V to 2.2V | | | 16.5 | |
| SCLK Pulse-Width Low | $t_5$ | Percentage of clock period (Note 4) | 40 | | 60 | % |
| SCLK Pulse-Width High | $t_6$ | Percentage of clock period (Note 4) | 40 | | 60 | % |
| Data Hold Time from SCLK Falling Edge | $t_7$ | Figure 3 (Note 4) | 5 | | | ns |
| SCLK Falling until DOUTA/DOUTB Three-Stated | $t_8$ | Figure 4 (Note 4) | 2.5 | | 14 | ns |
| T-Power Up | | 1 conversion cycle (Note 4) | | | 1 | Cycle |

**Note 2:** Limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization, unless otherwise noted.
**Note 3:** All timing specifications given are with a 10pF capacitor.
**Note 4:** Guaranteed by design in characterization; not production tested.



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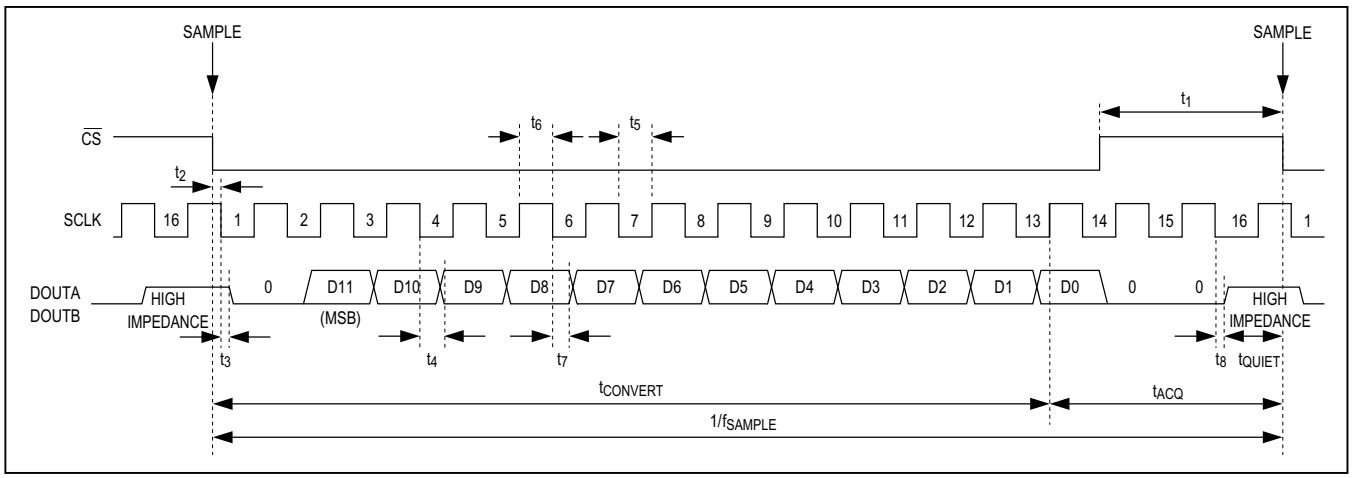


*Figure 1. Interface Signals for Maximum Throughput*

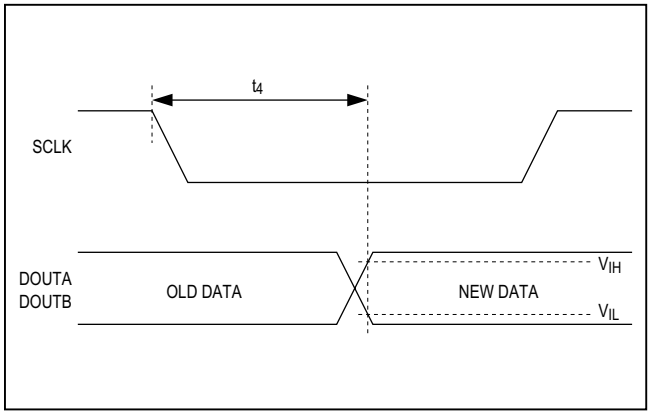


*Figure 2. Setup Time After SCLK Falling Edge*

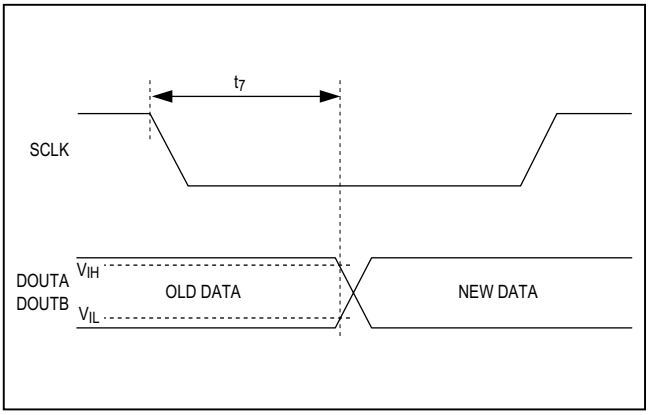


*Figure 3. Hold Time After SCLK Falling Edge*

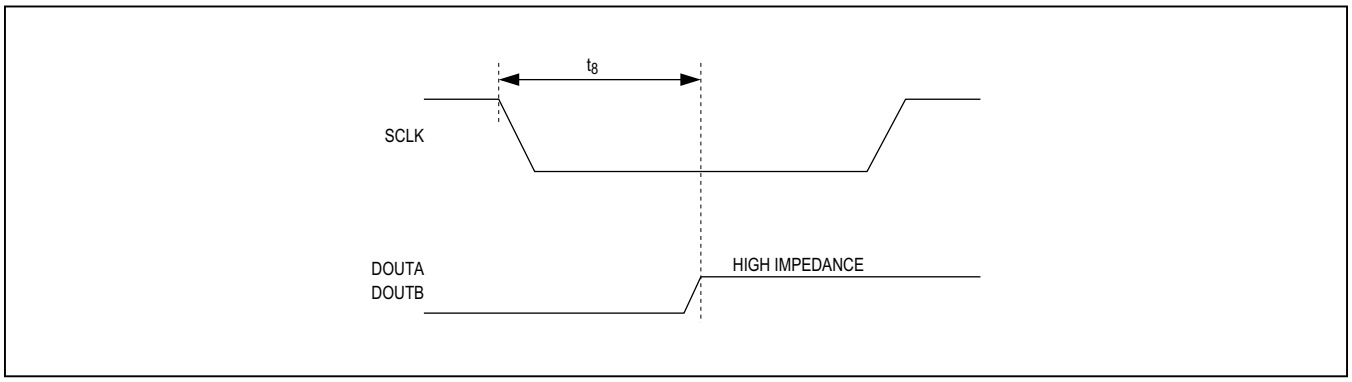


*Figure 4. SCLK Falling Edge DOUTA/DOUTB Three-State*



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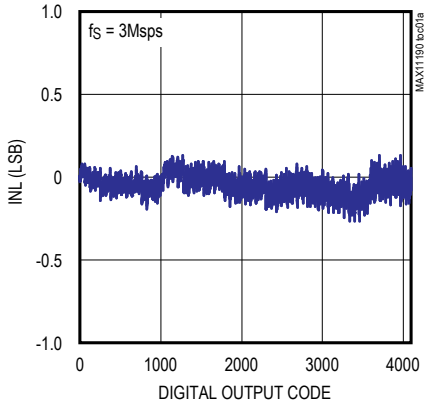
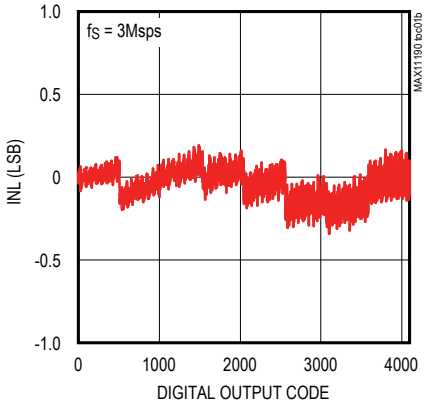
## Typical Operating Characteristics

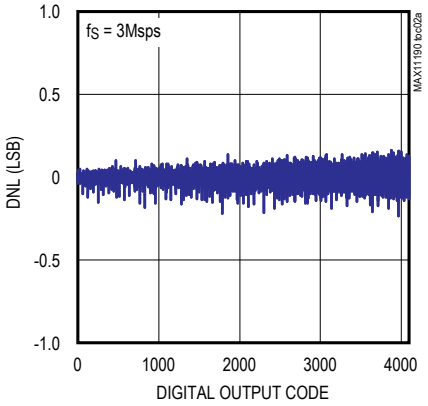
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE (A)



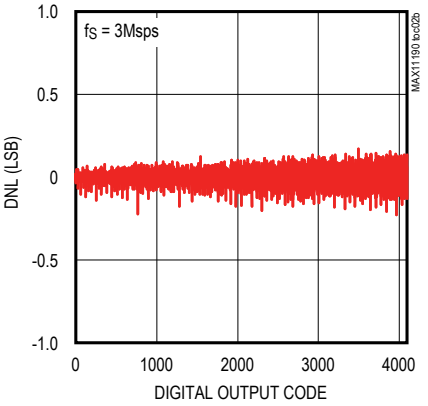

INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE (B)



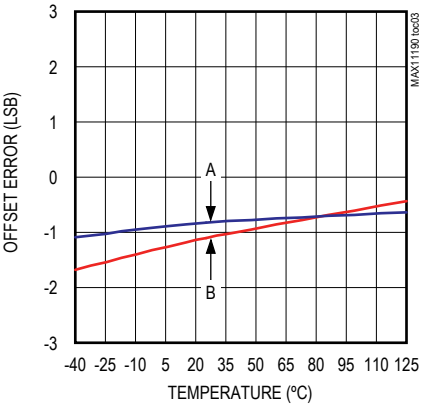

DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE (A)



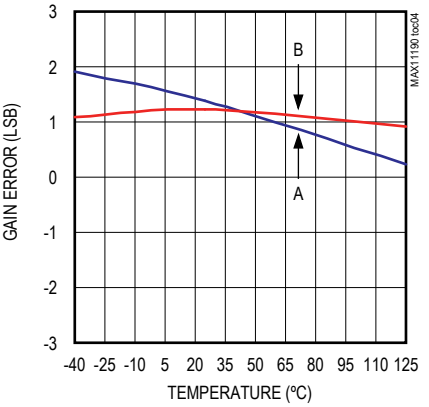

DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE (B)



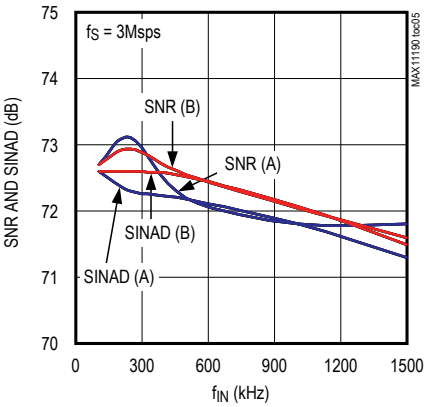

OFFSET ERROR vs. TEMPERATURE



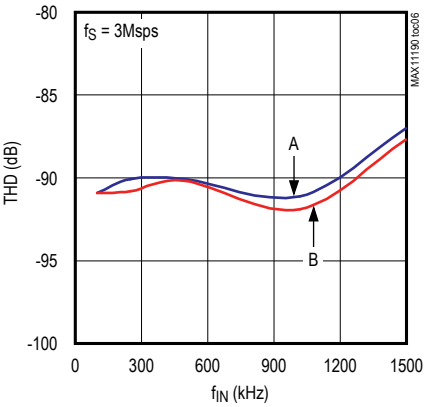

GAIN ERROR vs. TEMPERATURE



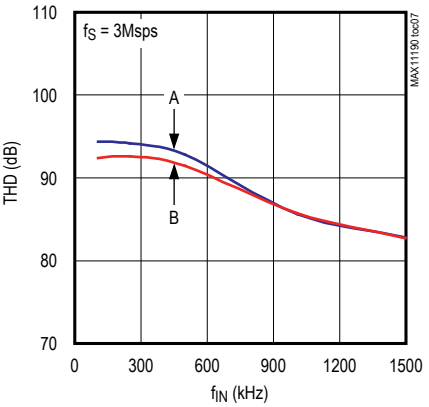

SNR AND SINAD vs. ANALOG INPUT FREQUENCY




THD vs. ANALOG INPUT FREQUENCY




SFDR vs. ANALOG INPUT FREQUENCY



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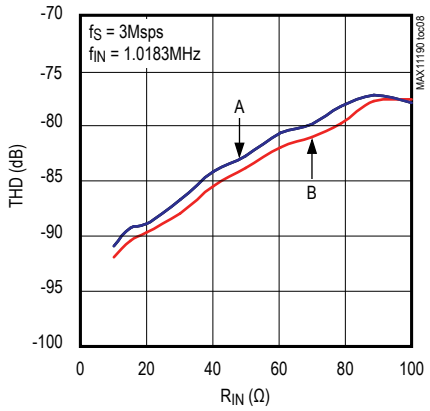
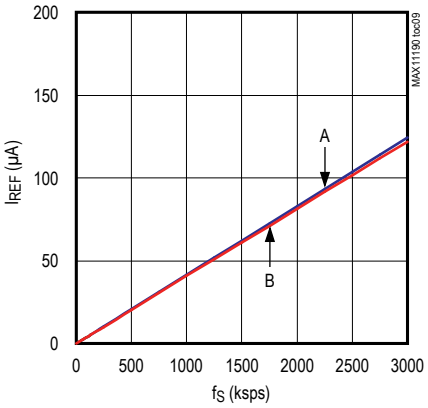
## Typical Operating Characteristics (continued)

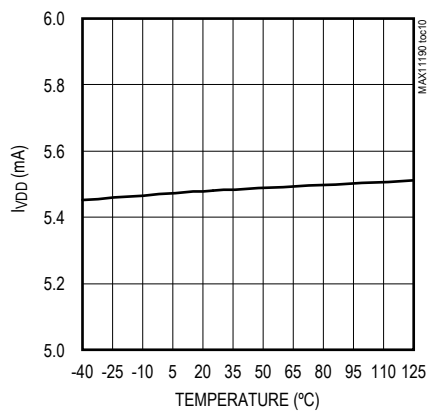
THD vs. INPUT RESISTANCE



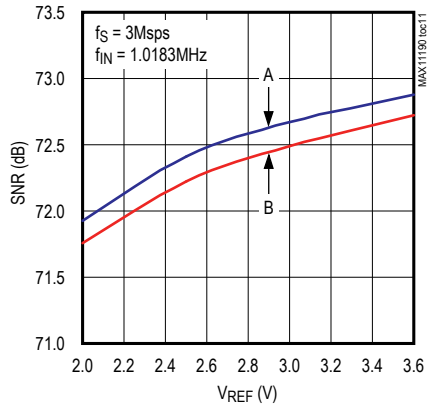

REFERENCE CURRENT vs. SAMPLING RATE



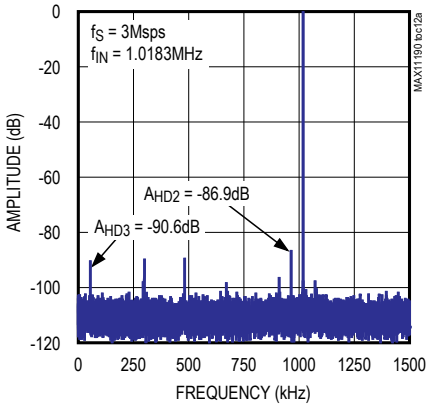

TOTAL SUPPLY CURRENT vs. TEMPERATURE



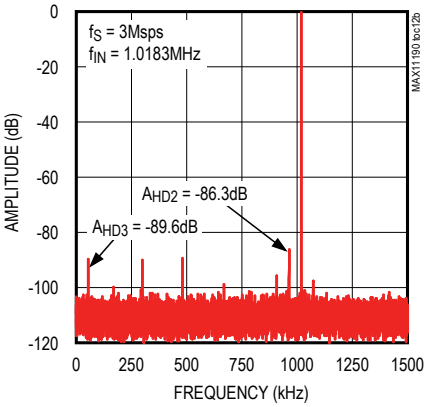

SNR vs. REFERENCE VOLTAGE




1MHz SINE WAVE INPUT (16384 POINT FFT PLOT) (A)




1MHz SINE WAVE INPUT (16384 POINT FFT PLOT) (B)



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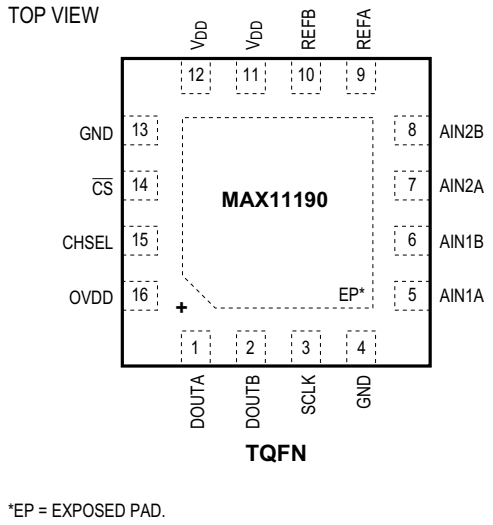
## Pin Configuration




## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | DOUTA | Serial-Data Output of ADC A. DOUTA changes state on SCLK's falling edge. |
| 2 | DOUTB | Serial-Data Output of ADC B. DOUTB changes state on SCLK's falling edge. |
| 3 | SCLK | Serial-Clock Input. SCLK drives the conversion process and clocks data out. |
| 4 | GND | Ground. This pin must connect to a solid ground plane. |
| 5 | AIN1A | Channel 1 of ADC A |
| 6 | AIN1B | Channel 1 of ADC B |
| 7 | AIN2A | Channel 2 of ADC A |
| 8 | AIN2B | Channel 2 of ADC B |
| 9 | REFA | Reference Pin for ADC A |
| 10 | REFB | Reference Pin for ADC B |
| 11, 12 | $V_{DD}$ | Positive Supply Voltage |
| 13 | GND | Ground. This pin must connect to a solid ground plane. |
| 14 | $\overline{CS}$ | Chip Select (Active-Low). Initiates power-up and acquisition on the falling edge. |
| 15 | CHSEL | Channel Select Pin Referring to AIN1A/AIN1B and AIN2A/AIN2B. Set CHSEL low to select AIN1A/AIN1B for conversion. |
| 16 | OVDD | Digital I/O Supply Voltage ($\overline{CS}$, CHSEL, DOUTA, DOUTB, SCLK). Bypass to GND with a 4.7µF ceramic capacitor. |
| — | EP | Exposed pad, internally connected to ground. Connect to a solid ground plane. |



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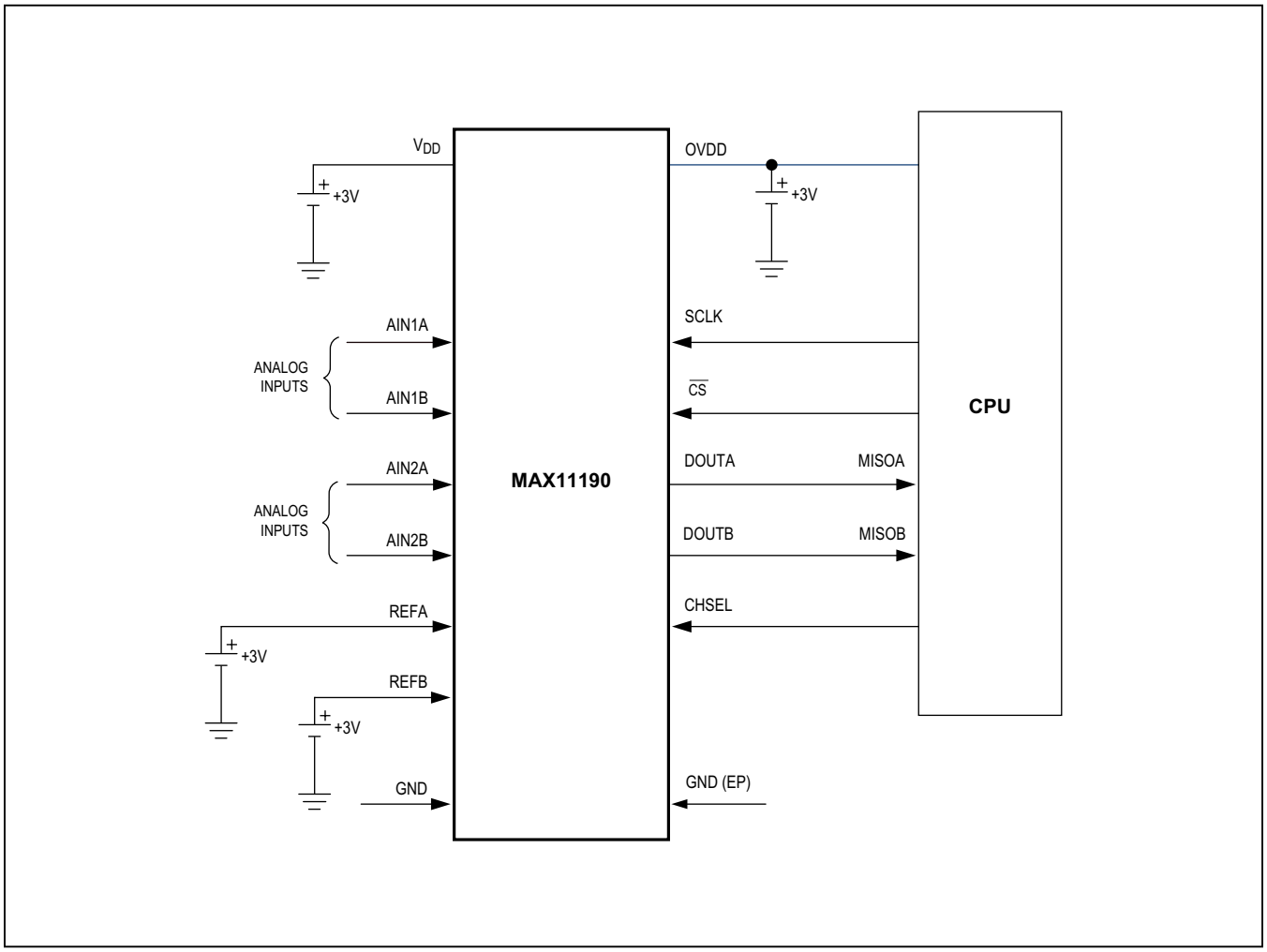
## Typical Operating Circuit



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## Detailed Description

The MAX11190 is a 3Msps, 12-bit, low-power, single-supply, dual, multiplexed simultaneous-sampling ADC. The device operates from a 2.2V to 3.6V supply and consumes only 16.4mW ($V_{DD}$ = 3V)/10.5mW ($V_{DD}$ = 2.2V) at 3Msps. This device is capable of sampling at full rate when driven by 48MHz. The MAX11190 provides a separate digital supply input (OVDD) to power the digital interface enabling communication with 1.5V, 1.8V, 2.5V, or 3V digital systems.

The conversion results for each of the two integrated ADCs appear at DOUTA and DOUTB, MSB first, with a leading zero followed by the 12-bit results followed by two trailing zeros. See Figure 1.

Each ADC core has an independent reference input. The input signal range for analog inputs is defined as 0V to $V_{REF}$ ($V_{REF}$ of respective core) with respect to GND.

This device includes a power-down feature allowing minimized power consumption at 5µA/ksps for lower throughput rates. The wake-up and power-down feature is controlled by using the SPI interface as described in the *Operation Modes* section.

### Serial Interface

The MAX11190 features a 3-wire serial interface that directly connects to SPI, QSPI, and MICROWIRE devices without external logic—DOUTA and DOUTB need to be received by the host at the same time. Figure 1 shows the interface signals for a single conversion frame to achieve maximum throughput.

The falling edge of $\overline{CS}$ defines the sampling instant. Once $\overline{CS}$ transitions low, the external clock signal (SCLK) controls the conversion.

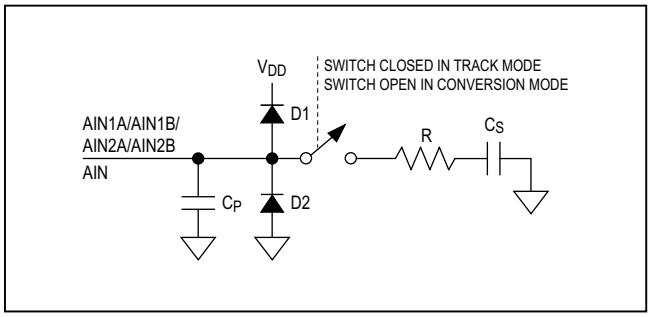


*Figure 5. Analog Input Circuit*

Each of the two SAR cores of this device successively extracts binary-weighted bits in every clock cycle. The MSB appears on the data bus during the 2nd clock cycle with a delay outlined in the timing specifications. All extracted data bits appear successively on the data bus with the LSB appearing during the 13th clock cycle for 12-bit operation. The serial data stream of conversion bits is preceded by a leading zero and succeeded by trailing zeros. The data outputs (DOUTA and DOUTB) go into high-impedance state during the 16th clock cycle.

To sustain the maximum sample rate, all devices have to be resampled immediately after the 16th clock cycle. For lower sample rates, the $\overline{CS}$ falling edge can be delayed leaving DOUTA/DOUTB in a high-impedance condition. Pull $\overline{CS}$ high after the 10th SCLK falling edge (see the *Operation Modes* section).

### Analog Input

The MAX11190 produces digital outputs that correspond to the analog input voltages within the specified operating range of 0 to $V_{REF}$.

Figure 5 shows an equivalent circuit for the analog input AIN1A/AIN1B/AIN2A/AIN2B. Internal protection diodes D1/D2 confine the analog input voltage within the power rails ($V_{DD}$, GND). The analog input voltage can swing from $V_{GND}$ - 0.3V to $V_{DD}$ + 0.3V without damaging the device.

The electric load presented to the external stage driving the analog input varies depending on which mode the ADC is in: track mode vs. conversion mode. In track mode, the internal sampling capacitor, $C_S$ (16pF), must be charged through the resistor, R (50Ω), to the input voltage. For faithful sampling of the input, the capacitor voltage on $\overline{CS}$ has to settle to the required accuracy during the track time.

The source impedance of the external driving stage in conjunction with the sampling switch resistance affects the settling performance. The THD vs. Input Resistance graph in the *Typical Operating Characteristics* shows THD sensitivity as a function of the signal source impedance. Keep the source impedance at a minimum for high-dynamic performance applications. Use a high-performance op amp, such as the MAX4430, to drive the analog input, thereby decoupling the signal source and the ADC.

While the ADC is in conversion mode, the sampling switch is open presenting a pin capacitance, $C_P$ ($C_P$ = 5pF), to the driving stage. See the *Applications Information* section for information on choosing an appropriate buffer for the ADC.



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## ADC Transfer Function

The output format is straight binary. The code transitions midway between successive integer LSB values such as 0.5 LSB, 1.5 LSB, etc. The LSB size is $V_{REF}/2^{12}$. The ideal transfer characteristic is shown in Figure 9.

## Operation Modes

The IC offers two modes of operation: normal mode and power-down mode. The logic state of the $\overline{CS}$ signal during a conversion activates these modes. The power-down mode can be used to optimize power dissipation with respect to sample rate.

### Normal Mode

In normal mode, the device is powered up at all times, thereby achieving its maximum throughput rates. Figure 6 shows the timing diagram of this device in normal mode. The falling edge of $\overline{CS}$ samples the analog input signal, starts a conversion, and frames the serial-data transfer.

To remain in normal mode, keep $\overline{CS}$ low until the falling edge of the 10th SCLK cycle. Pulling $\overline{CS}$ high after the 10th SCLK falling edge keeps the part in normal mode. However, pulling $\overline{CS}$ high before the 10th SCLK falling edge terminates the conversion, both DOUTA/DOUTBs go into high-impedance mode, and the device enters power-down mode. See Figure 7.

### Power-Down Mode

In power-down mode, all bias circuitry is shut down drawing typically only 2.6µA of leakage current. To save power, put the device in power-down mode between conversions. Using the power-down mode between conversions is ideal for saving power when sampling the analog input infrequently.

### Entering Power-Down Mode

To enter power-down mode, drive $\overline{CS}$ high between the 2nd and 10th falling edges of SCLK (see Figure 7). By pulling $\overline{CS}$ high, the current conversion terminates and both DOUTA/DOUTB enter high impedance.

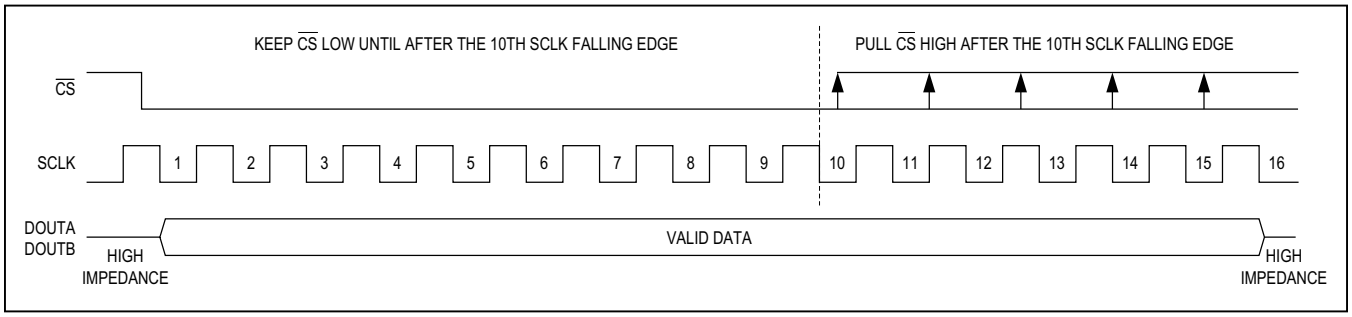


*Figure 6. Normal Mode*

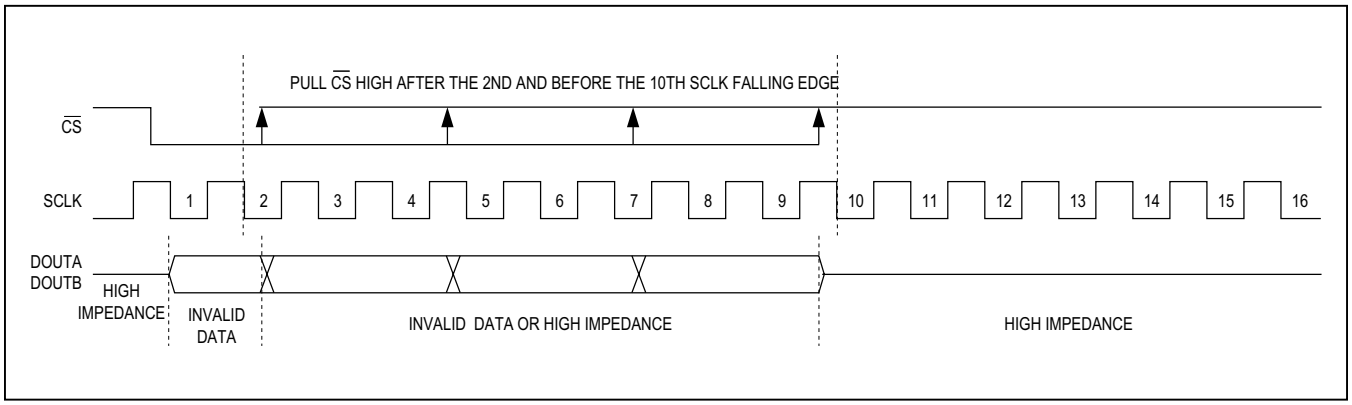


*Figure 7. Entering Power-Down Mode*



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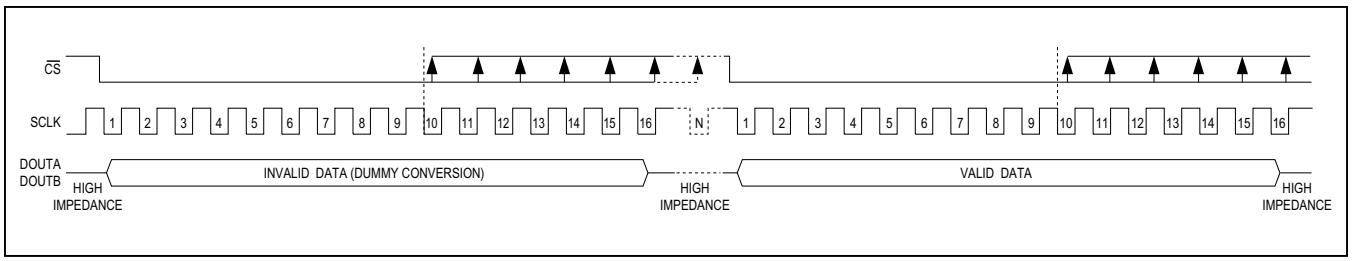


*Figure 8. Exiting Power-Down Mode*

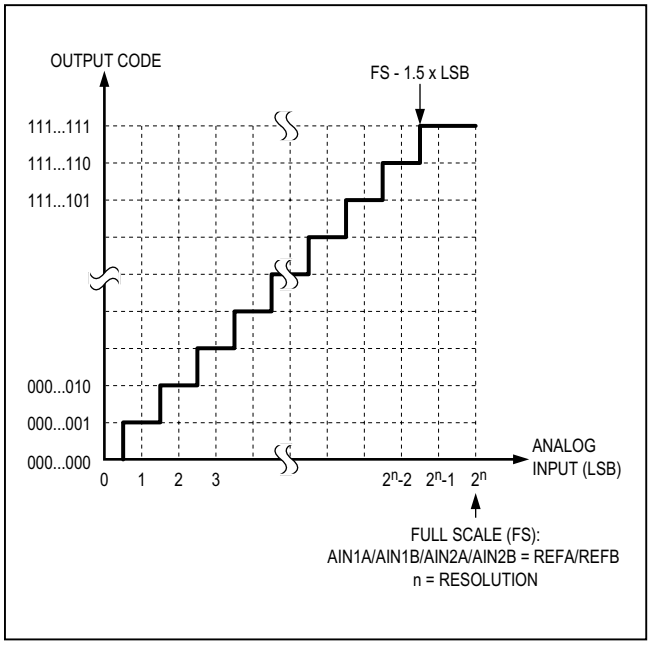


*Figure 9. ADC Transfer Function*

## Exiting Power-Down Mode

To exit power-down mode, implement one dummy conversion by driving $\overline{CS}$ low for at least 10 clock cycles (see Figure 8). The data on DOUTA/DOUTB is invalid during this dummy conversion. The first conversion following the dummy cycle contains a valid conversion result.

The power-up time equals the duration of the dummy cycle, and is dependent on the clock frequency. The power-up time for this device (48MHz SCLK) is 333ns.

## Supply Current vs. Sampling Rate

For applications requiring lower throughput rates, the user can reduce the clock frequency ($f_{SCLK}$) to lower the sample rate. Figure 10 shows the typical supply current ($I_{VDD}$) as a function of sample rate ($f_S$) for the device. The part operates in normal mode and is never powered down.

The user can also power down the ADC between conversions by using power-down mode. Figure 11 shows this device as the sample rate is reduced, the device remains in the power-down state longer and the average supply current ($I_{VDD}$) drops accordingly.

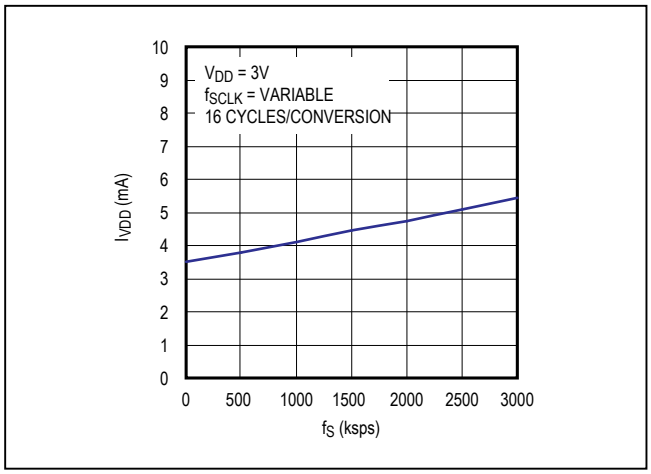


*Figure 10. Supply Current vs. Sample Rate (Normal Operating Mode)*

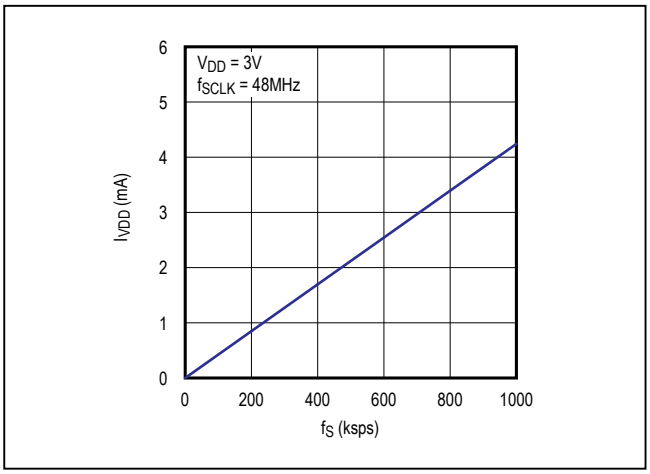


*Figure 11. Supply Current vs. Sample Rate (Device Powered Down Between Conversions)*



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### Dual-Channel Operation

The MAX11190 features dual simultaneous-sampling ADCs each with two multiplexed channels. This device uses a channel-select (CHSEL) input to select between analog input AIN1A/AIN1B (CHSEL = 0) or AIN2A/AIN2B (CHSEL = 1). As shown in Figure 12, the CHSEL signal is required to change between the 2nd and 12th clock cycle within a regular conversion to guarantee proper switching between channels.

### 14-Cycle Conversion Mode

The IC can operate with 14 cycles per conversion. Figure 13 shows the corresponding timing diagram. Observe that DOUTA/DOUTB does not go into high-impedance mode. Also, observe that $t_{ACQ}$ needs to be sufficiently long to guarantee proper settling of the analog input voltage. See the *Electrical Characteristics* table for $t_{ACQ}$ requirements and the *Analog Input* section for a description of the analog inputs.

## Applications Information

### Layout, Grounding, and Bypassing

For best performance, use PCBs with a solid ground plane. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another or digital lines underneath the ADC package. Noise in the $V_{DD}$ power supply, OVDD, and REFA/REFB affects the ADC's performance. Bypass the $V_{DD}$, OVDD, and REFA/REFB to ground with 0.1µF and 10µF bypass capacitors. Minimize capacitor lead and trace lengths for best supply-noise rejection.

### Choosing an Input Amplifier

It is important to match the settling time of the input amplifier to the acquisition time of the ADC. The conversion results are accurate when the ADC samples the input signal for an interval longer than the input signal's worst-case settling time. By definition, settling time is the interval

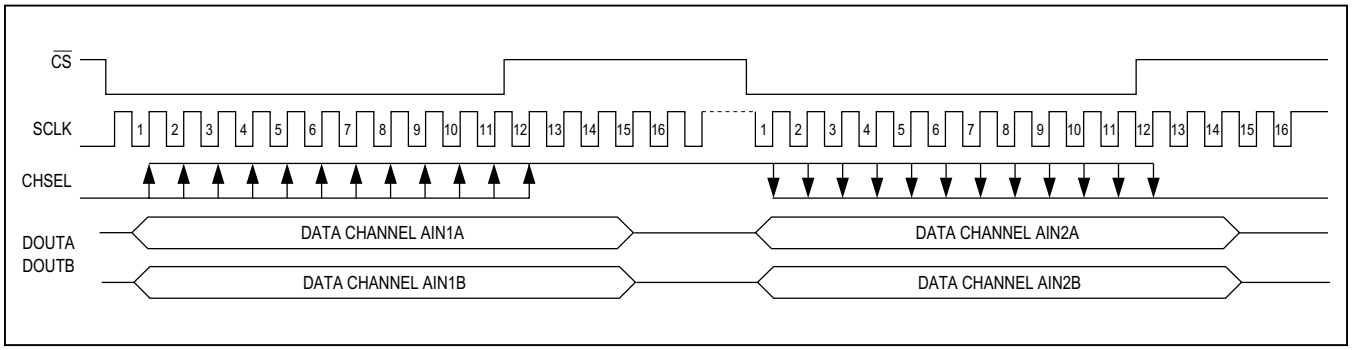


*Figure 12. Channel Select Timing Diagram*

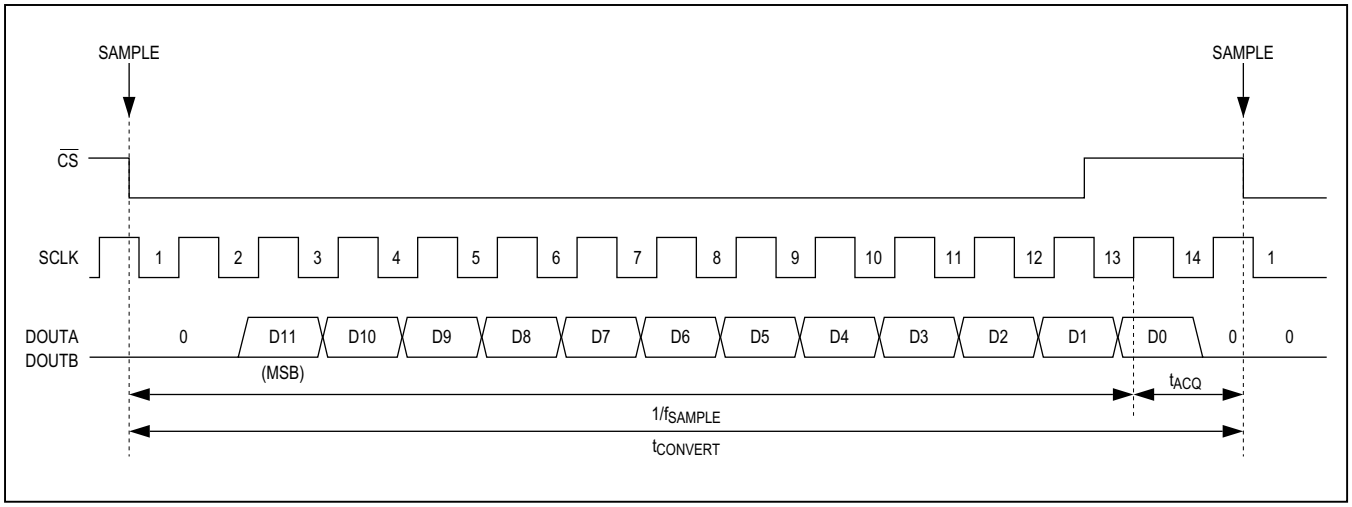


*Figure 13. 14-Clock Cycle Operation*



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between the application of an input voltage step and the point at which the output signal reaches and stays within a given error band centered on the resulting steady-state amplifier output level. The ADC input sampling capacitor charges during the sampling cycle, referred to as the acquisition period. During this acquisition period, the settling time is affected by the input resistance and the input sampling capacitance. This error can be estimated by looking at the settling of an RC time constant using the input capacitance and the source impedance over the acquisition time period.

Figure 14 shows a typical application circuit. The MAX4430, offering a settling time of 37ns at 16 bits, is an excellent choice for this application. See the THD vs. Input Resistance graph in the *Typical Operating Characteristics*.

## Choosing a Reference

For devices using an external reference, the choice of the reference determines the output accuracy of the ADC. An ideal voltage reference provides a perfect initial accuracy and maintains the reference voltage independent of changes in load current, temperature, and time. Considerations in selecting a reference include initial voltage accuracy, temperature drift, current source, sink capability, quiescent current, and noise. Figure 14 shows a typical application circuit using the MAX6126 to provide the reference voltage. The MAX6033 and MAX6043 are also excellent choices.

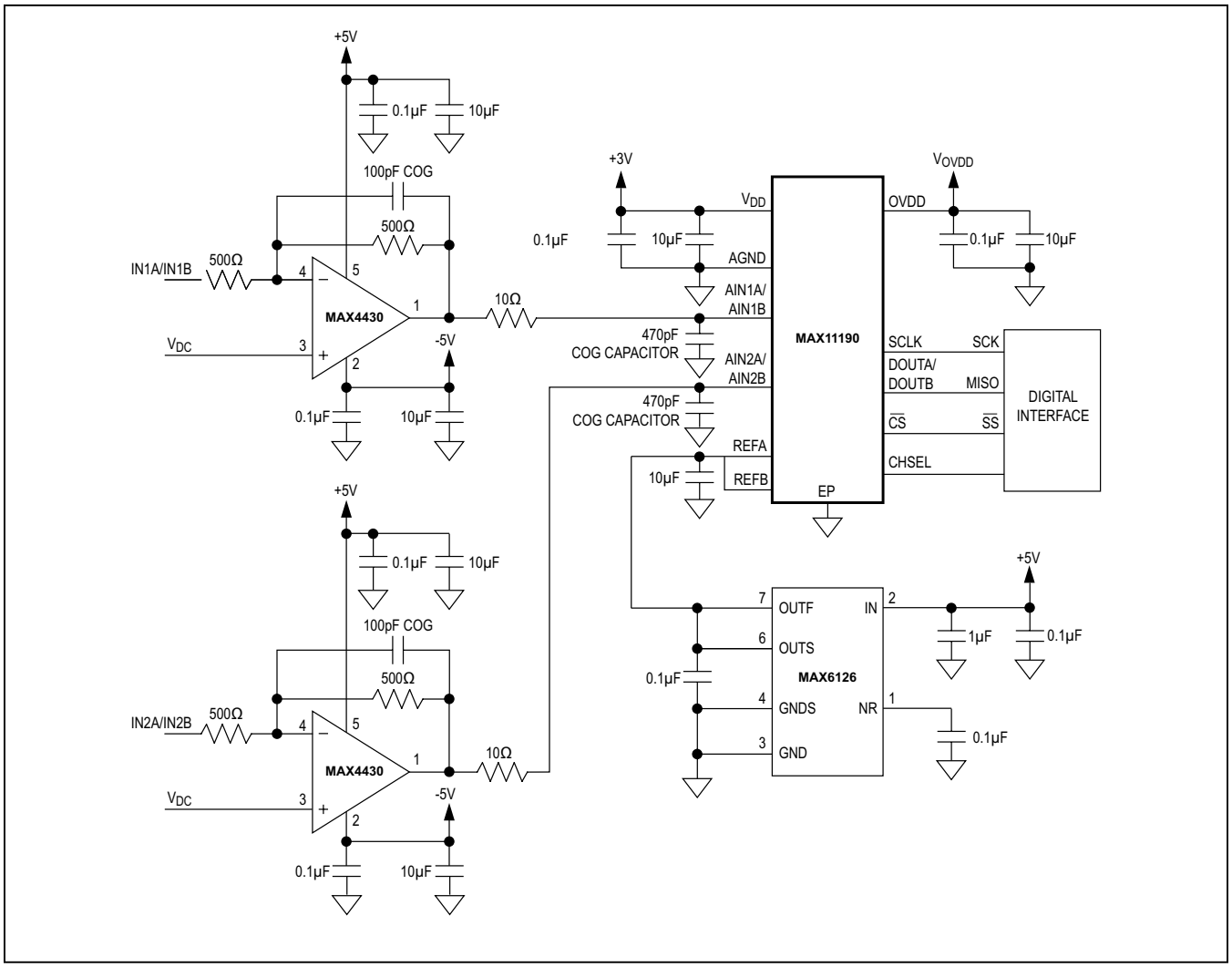


*Figure 14. Typical Application Circuit*



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## Definitions

### Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. For these devices, the straight line is a line drawn between the end points of the transfer function after offset and gain errors are nulled.

### Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of ±1 LSB or less guarantees no missing codes and a monotonic transfer function.

### Offset Error

Offset error is the deviation of the first code transition (00 . . . 000) to (00 . . . 001) from the ideal, that is, AGND + 0.5 LSB.

### Gain Error

Gain error is the deviation of the last code transition (111 . . . 110) to (111 . . . 111) from the ideal after adjusting for the offset error, that is, $V_{REF}$ - 1.5 LSB.

### Aperture Jitter

Aperture jitter ($t_{AJ}$) is the sample-to-sample variation in the time between the samples.

### Aperture Delay

Aperture delay ($t_{AD}$) is the time between the falling edge of the sampling clock and the instant when an actual sample is taken.

### Aperture Delay Matching

Aperture delay ($t_{ADM}$) is the difference between the aperture delay between channel A and B measured at the falling edge of the sampling clock for the sample taken from the identical analog input.

### Signal-To-Noise Ratio (SNR)

SNR is a dynamic figure of merit that indicates the converter's noise performance. For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

SNR (dB) (MAX) = (6.02 x N + 1.76) (dB)

In reality, there are other noise sources such as thermal noise, reference noise, and clock jitter that also degrade SNR. SNR is computed by taking the ratio of the RMS signal to the RMS noise. RMS noise includes all spectral components to the Nyquist frequency excluding the fundamental, the first five harmonics, and the DC offset.

### Signal-To-Noise Ratio and Distortion (SINAD)

SINAD is a dynamic figure of merit that indicates the converter's noise and distortion performance. SINAD is computed by taking the ratio of the RMS signal to the RMS noise plus distortion. RMS noise plus distortion includes all spectral components to the Nyquist frequency excluding the fundamental and the DC offset:

$$SINAD(dB) = 20 \times \log\left[\frac{SIGNAL_{RMS}}{(NOISE + DISTORTION)_{RMS}}\right]$$

### Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1}\right)$$

where $V_1$ is the fundamental amplitude and $V_2$–$V_5$ are the amplitudes of the 2nd- through 5th-order harmonics.

### Spurious-Free Dynamic Range (SFDR)

SFDR is a dynamic figure of merit that indicates the lowest usable input signal amplitude. SFDR is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset. SFDR is specified in decibels with respect to the carrier (dBc).

### Full-Power Bandwidth

Full-power bandwidth is the frequency at which the input signal amplitude attenuates by 3dB for a full-scale input.

### Full-Linear Bandwidth

Full-linear bandwidth is the frequency at which the SINAD is equal to a specified value.

### Intermodulation Distortion

Any device with nonlinearities creates distortion products when two sine waves at two different frequencies ($f_1$ and $f_2$) are applied into the device. Intermodulation distortion (IMD) is the total power of the IM2 to IM5 intermodulation products to the Nyquist frequency relative to the total input power of the two input tones, $f_1$ and $f_2$. The individual input tone levels are at -6dBFS.



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## Ordering Information

| PART | PIN-PACKAGE | BITS | SPEED |
|---|---|---|---|
| MAX11190ATE+ | 16 TQFN-EP* | 12 | 3Msps |

***Note:*** *All devices are specified over the -40ºC to +125ºC operating temperature range.*

*+Denotes lead(Pb)-free/RoHS-compliant package.*

**EP = Exposed pad.*

## Chip Information

PROCESS: CMOS

## Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|---|---|---|---|
| 16 TQFN-EP | T1633MK+5 | **21-0136** | **90-0032** |



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## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 6/13 | Initial release | — |
| 1 | 2/14 | Updated *Package Thermal Characteristics* and *Package Information* | 4, 18 |
| 2 | 12/14 | Updated *Benefits and Features* section | 1 |

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