12-Channel High Voltage Analog Switch

Features

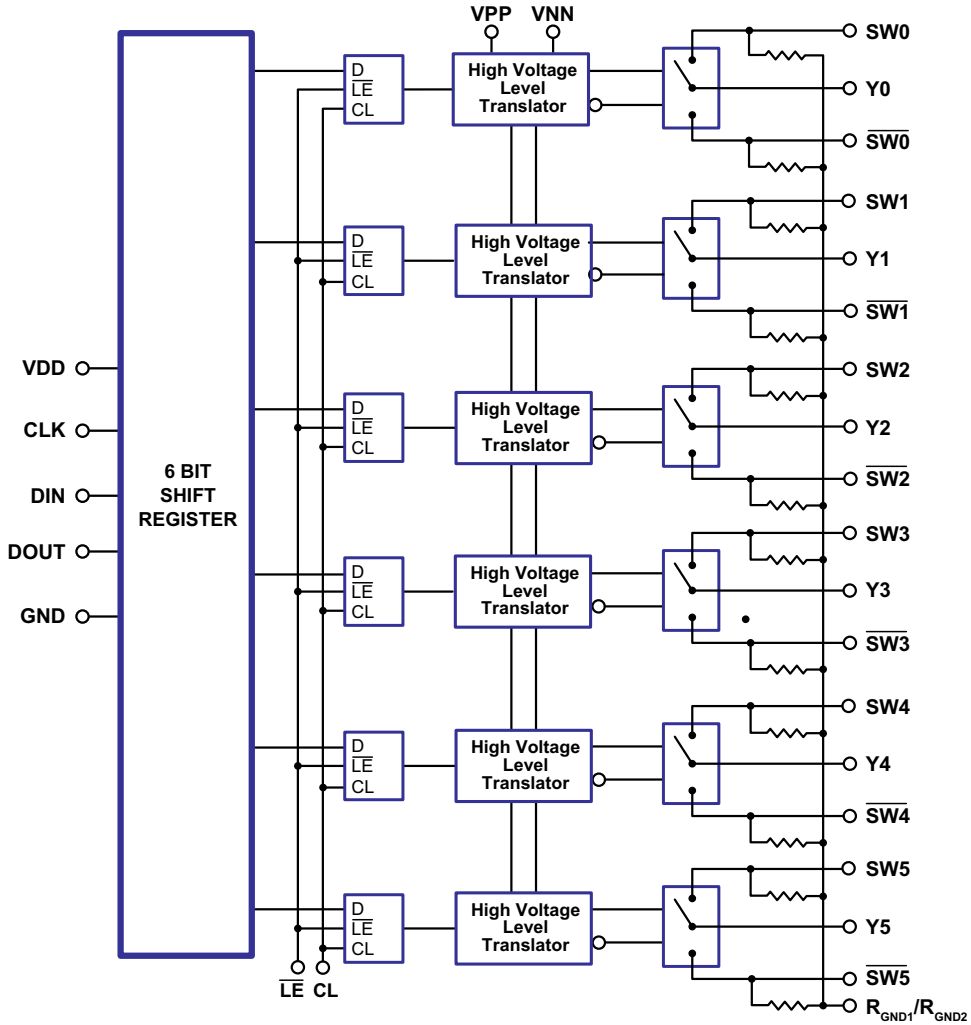
- HVCMOS® technology for high performance
- Operating voltage of up to 200V
- Output on-resistance typically 22Ω
- Integrated bleed resistors on the outputs
- 5.0V to 12.0V CMOS logic compatibility
- Very low quiescent current consumption (-10µA)
- -58dB typical off isolation at 5.0MHz
- Low parasitic capacitance
- Excellent noise immunity
- Flexible high voltage supplies

General Description

The Supertex HV209 is a 200V low charge injection 12-channel high voltage analog switch configured as 6 SPDT analog switches intended for medical ultrasound applications.

Bleed resistors are integrated on the output switches to eliminate charge built up on the piezo electric transducers.The bleed resistors are at a nominal value of 35kΩ. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals. The outputs are configured as single-pole double-throw analog switches. Data is shifted into a 6-bit shift register using an external clock. The $\overline{LE}$ latches the shift register data into the individual switch latches. A logic HI connects a switch common Y_X to $\overline{SW_X}$. A logic LOW connects Y_X to $\overline{SW_X}$. A logic HI in CL resets all switches to SW_X simultaneously.

Block Diagram



Ordering Information

Part Number	Package Option	Packing
HV209FG-G	48-Lead LQFP	250/Tray
HV209FG-G M931		1000/Reel

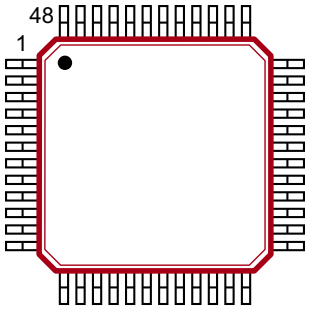
-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

Parameter	Value
V_{DD} Logic power supply voltage	-0.5V to +15V
V_{PP} - V_{NN} Supply voltage	+220V
V_{PP} Positive high voltage supply	-0.5V to +200V
V_{NN} Negative high voltage supply	+0.5V to -200V
Logic input voltages	-0.5V to V_{DD} +0.3V
V_{SIG} Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation: 48-lead LQFP	1.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



48-Lead LQFP
(top view)

Product Marking

Top Marking

Bottom Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging
**May be part of top marking*

Package may or may not include the following marks: Si or

48-Lead LQFP

Typical Thermal Resistance

Package	θ_{ja}
48-Lead LQFP	52°C/W

Recommended Operating Conditions

Sym	Parameter	Value
V_{PP}	Positive high voltage supply[1]	+40V to V_{NN} +200V
V_{NN}	Negative high voltage supply[1]	-10V to -160V
V_{DD}	Logic power supply voltage[1]	+4.5V to +13.2V
V_{IH}	High-level input voltage	0.8V_{DD} to V_{DD}
V_{IL}	Low-level input voltage	0V to 0.2V_{DD}
V_{SIG}	Analog signal voltage peak-to-peak[2]	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air-temperature	0°C to 70°C

Notes:

1. *Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.*
2. *V_{SIG} must be within V_{PP} and V_{NN} voltage range or floating during power up/down transition.*

DC Electrical Characteristics

(over recommended operating conditions unless otherwise noted)

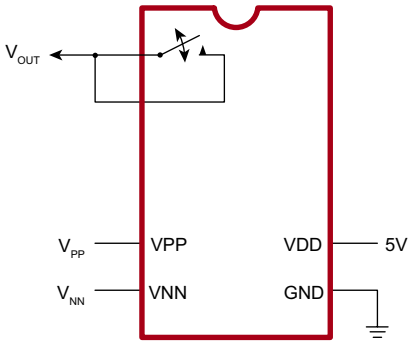
Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		min	max	min	typ	max	min	max			
R_{ONS}	Small signal switch on-resistance	-	30	-	26	38	-	48	Ω	I_{SIG} = 5.0mA	V_{PP} = 40V, V_{NN} = -160V
		-	25	-	22	27	-	32		I_{SIG} = 200mA	
		-	25	-	22	27	-	30		I_{SIG} = 5.0mA	V_{PP} = 100V, V_{NN} = -100V
		-	18	-	18	24	-	27		I_{SIG} = 200mA	
		-	23	-	20	25		30		I_{SIG} = 5.0mA	V_{PP} = 190V, V_{NN} = -10V
		-	22	-	16	25		27		I_{SIG} = 200mA	
ΔR_{ONS}	Small signal switch on-resistance matching	-	20	-	5.0	20	-	20	%	I_{SW} = 5.0mA, V_{PP} = 100V, V_{NN} = -100V	
R_{ONL}	Large signal switch on-resistance	-	-	-	15	-	-	-	Ω	V_{SIG} = V_{PP} -10V, I_{SIG} = 1.0A	
R_{INT}	Output switch shunt resistance	-	-	20	35	50	-	-	KΩ	Output switch to R_{GND}, I_{RINT} = 0.5mA	
V_{OS}	DC offset switch off	-	50	-	-	50	-	50	mV	No load, R_{GND} = 0V	
	DC offset switch on	-	50	-	-	50	-	50	mV	No load, R_{GND} = 0V	
I_{PPQ}	Pos. HV supply current	-	-	-	10	50	-	-	µA	All SWs off	
I_{NNQ}	Neg. HV supply current	-	-	-	-10	-50	-	-			
I_{PPQ}	Pos. HV supply current	-	-	-	10	50	-	-	µA	All SWs on, I_{SW} = 5.0mA	
I_{NNQ}	Neg. HV supply current	-	-	-	-10	-50	-	-			
I_{SW}	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V_{SIG} duty cycle ≤ 0.1%	
f_{SW}	Output switch frequency	-	-	-	-	50	-		KHz	Duty cycle = 50%	
I_{PP}	I_{PP} supply current	-	6.5	-	-	7.0	-	8.0	mA	V_{PP} = 40V, V_{NN} = -160V	50KHz output switching frequency with no load
		-	4.0	-	-	5.0	-	5.5		V_{PP} = 100V, V_{NN} = -100V	
		-	4.0	-	-	5.0	-	5.5		V_{PP} = 190V, V_{NN} = -10V	
I_{NN}	I_{NN} supply current	-	6.5	-	-	7.0	-	8.0	mA	V_{PP} = 40V, V_{NN} = -160V	50KHz output switching frequency with no load
		-	4.0	-	-	5.0	-	5.5		V_{PP} = 100V, V_{NN} = -100V	
		-	4.0	-	-	5.0	-	5.5		V_{PP} = 190V, V_{NN} = -10V	
I_{DD}	Logic supply average current	-	4.0	-	-	4.0	-	4.0	mA	f_{CLK} = 5.0MHz, V_{DD} = 5.0V	
I_{DDQ}	Logic supply quiescent current	-	10	-	-	10	-	10	µA	---	
I_{SOR}	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = V_{DD} -0.7V	
I_{SINK}	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = 0.7V	
C_{IN}	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

AC Electrical Characteristics

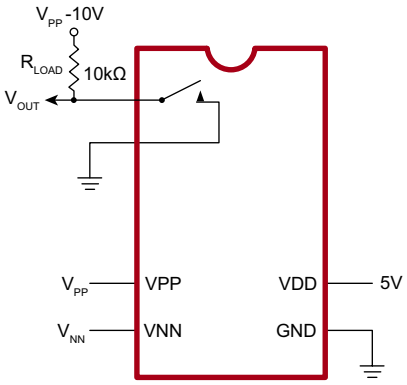
(over recommended operating conditions V_{DD} = 5.0V unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		min	max	min	typ	max	min	max		
t_{SD}	Set up time before $\overline{LE}$ rises	150	-	150	-	-	150	-	ns	---
t_{WLE}	Time width of $\overline{LE}$	150	-	150	-	-	150	-	ns	---
t_{DO}	Clock delay time to data out	-	150	-	-	150	-	150	ns	---
t_{WCL}	Time width of CL	150	-	150	-	-	150	-	ns	---
t_{SU}	Set up time data to clock	15		15	8.0	-	20	-	ns	---
t_{H}	Hold time data from clock	35	-	35	-	-	35	-	ns	---
f_{CLK}	Clock frequency	-	5.0	-	-	5.0	-	5.0	MHz	50% duty cycle, $f_{DATA} = f_{CLK}/2$
t_{ON}	Turn on time	-	5.0	-	-	5.0	-	5.0	µs	$V_{SIG} = V_{PP}$ -10V, R_L = 10kΩ
t_{OFF}	Turn off time	-	5.0	-	-	5.0	-	5.0	µs	$V_{SIG} = V_{PP}$ -10V, R_L = 10kΩ
dv/dt	Maximum V_{SIG} slew rate	-	20	-	-	20	-	20	V/ns	V_{PP} = 40V, V_{NN} = -160V
		-	20	-	-	20	-	20		V_{PP} = 100V, V_{NN} = -100V
		-	20	-	-	20	-	20		V_{PP} = 190V, V_{NN} = -10V
K_O	Off Isolation	-30	-	-30	-33	-	-30	-	dB	f = 5.0MHz, 1.0kΩ//15pF load
		-58	-	-58	-	-	-58	-	dB	f = 5.0MHz, 50Ω load
K_{CR}	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	f = 5.0MHz, 50Ω load
I_{ID}	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{GS(OFF)}$	Off capacitance switch to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, 1.0MHz
$C_{GS(ON)}$	On capacitance switch to GND	25	50	25	38	50	25	50	pF	0V, 1.0MHz
$+V_{SPK}$	Output voltage spike	-	150	-	-	150	-	150	mV	R_{LOAD} = 50Ω
$-V_{SPK}$		-	150	-	-	150	-	150		R_{LOAD} = 50Ω

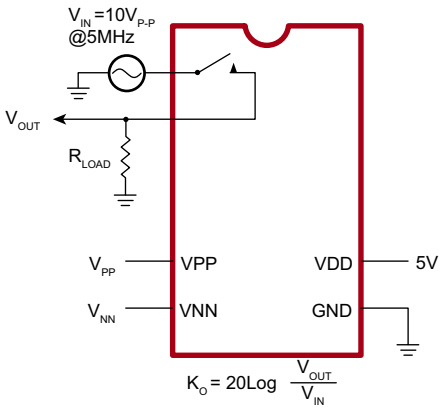
Test Circuits



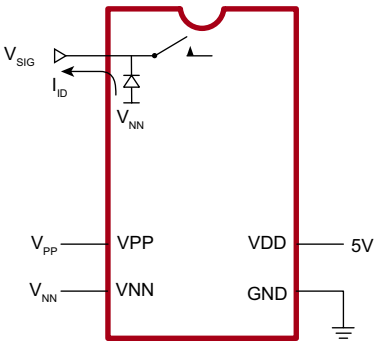
DC Offset ON/OFF



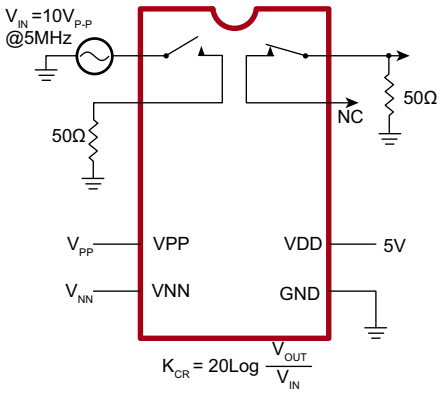
T_{ON}/T_{OFF} Test Circuit



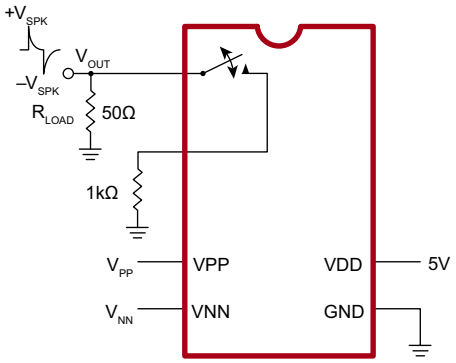
OFF Isolation



Isolation Diode Current

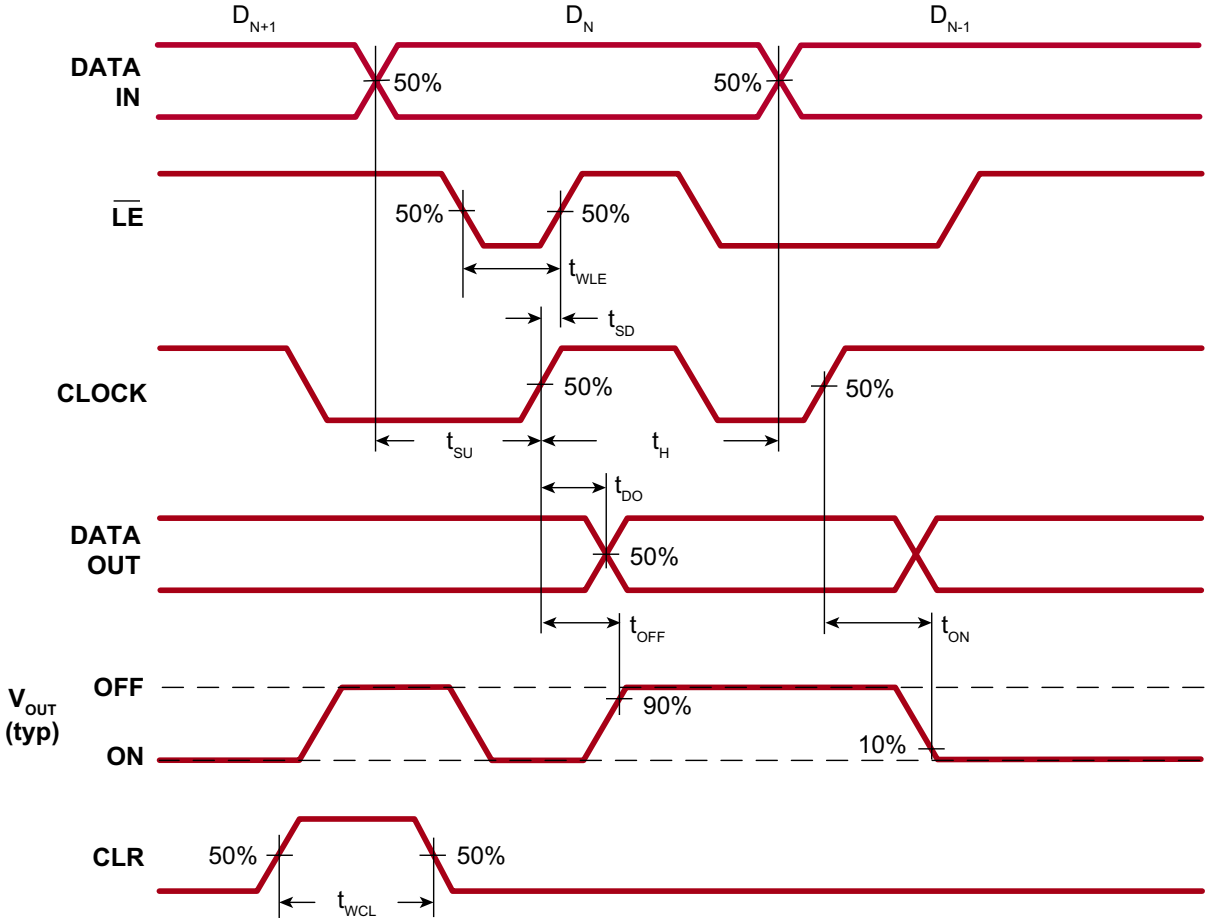


Crosstalk



Output Voltage Spike

Logic Timing Waveforms



Logic Truth Table

Data Inputs						$\overline{LE}$	CL	Switch States					
D0	D1	D2	D3	D4	D5			Y0	Y1	Y2	Y3	Y4	Y5
L						L	L	$\overline{SW0}$					
H						L	L	SW0					
	L					L	L		$\overline{SW1}$				
	H					L	L		SW1				
		L				L	L			$\overline{SW2}$			
		H				L	L			SW2			
			L			L	L				$\overline{SW3}$		
			H			L	L				SW3		
				L		L	L					$\overline{SW4}$	
				H		L	L					SW4	
					L	L	L						$\overline{SW5}$
					H	L	L						SW5
X	X	X	X	X	X	H	L	Hold Previous State					
X	X	X	X	X	X	X	H	$\overline{SW0}$	$\overline{SW1}$	$\overline{SW2}$	$\overline{SW3}$	$\overline{SW4}$	$\overline{SW5}$

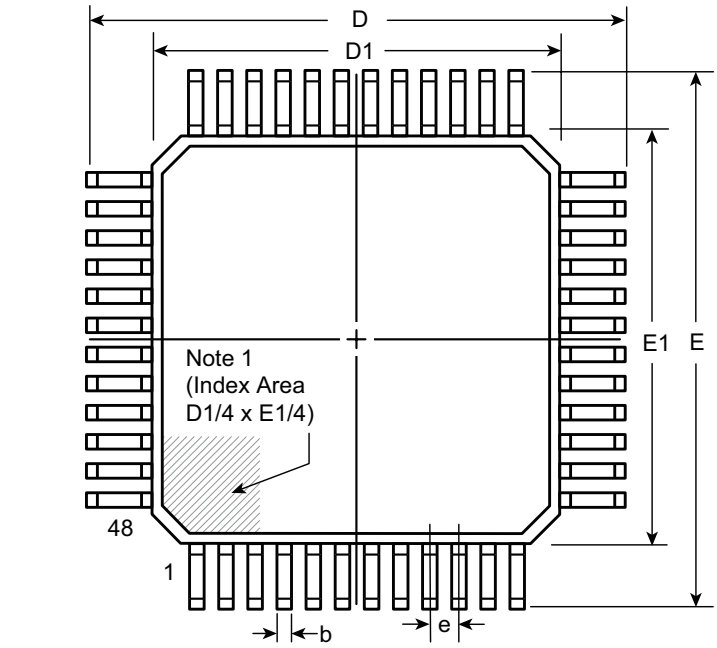
Pin Description

Pin #	Function
1	N/C
2	SW0
3	Y0
4	$\overline{SW0}$
5	N/C
6	SW2
7	Y2
8	$\overline{SW2}$
9	N/C
10	SW4
11	Y4
12	$\overline{SW4}$
13	N/C
14	N/C
15	N/C
16	VNN
17	N/C
18	N/C
19	N/C
20	N/C
21	VPP
22	N/C
23	N/C
24	N/C

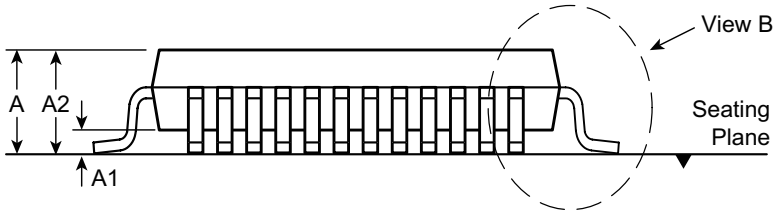
Pin #	Function
25	$\overline{SW5}$
26	Y5
27	SW5
28	N/C
29	$\overline{SW3}$
30	Y3
31	SW3
32	N/C
33	$\overline{SW1}$
34	Y1
35	SW1
36	N/C
37	RGND1
38	N/C
39	DOUT
40	VDD
41	DIN
42	CLR
43	$\overline{LE}$
44	CLK
45	GND
46	N/C
47	N/C
48	RGND2

48-Lead LQFP Package Outline (FG)

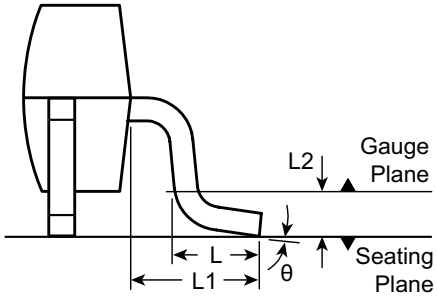
7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Top View



Side View



View B

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75			7°

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.
** This dimension is not specified in the JEDEC drawing.*

Drawings are not to scale.
Supertex Doc. #: *DSPD-48LQFPFG Version, D041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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