16-Channel, High Voltage Analog Switch

Features

- HVCMOS® technology for high performance
- 220V operating conditions
- Output on-resistance typically 22Ω
- 5.0 and 12.0V CMOS logic compatibility
- Very low quiescent current consumption (-10µA)
- -45dB min off isolation at 7.5MHz
- Low parasitic capacitance
- Excellent noise immunity
- Flexible high voltage supplies

Applications

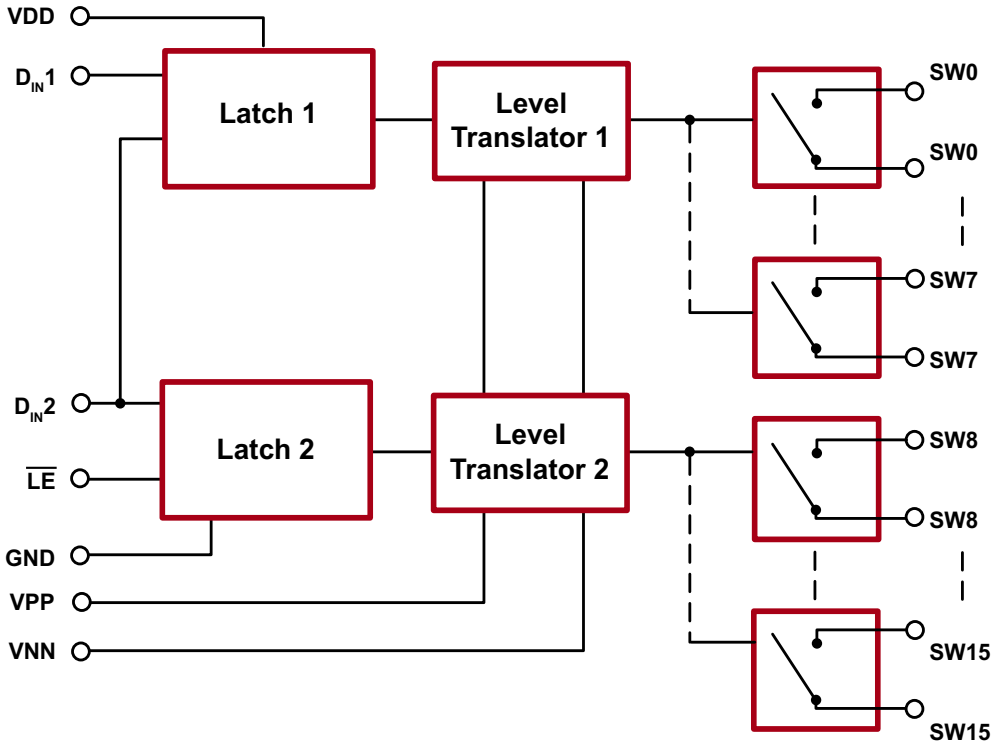
- Medical ultrasound imaging
- Piezoelectric transducer drivers

General Description

The Supertex HV20822 is a 220V, 16-channel, high-voltage analog switch integrated circuit (IC) configured as 2 sets of 8 single-pole single-throw analog switches. It is intended for use in applications requiring high voltage switching controlled by low voltage control signals such as ultrasound imaging and printers.

The 2 sets of 8 analog switches are controlled by 2 input logic controls, $D_{IN}1$ and $D_{IN}2$. A logic high on $D_{IN}1$ will turn On switches 0 to 7 and a logic high on $D_{IN}2$ will turn On switches 8 to 15.

Block Diagram



Ordering Information

Part Number	Package Option	Packing
HV20820FG-G	48-Lead LQFP	250/Tray
HV20820FG-G M931	48-Lead LQFP	1000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings

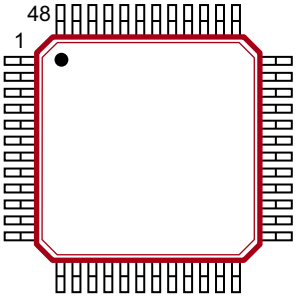
Parameter	Value
V_{DD} Logic power supply voltage	-0.5V to +15V
V_{PP} - V_{NN} Supply voltage	+225V
V_{PP} Positive high voltage supply	-0.5V to V_{NN} +225V
V_{NN} Negative high voltage supply	+0.5V to -225V
Logic input voltages	-0.5V to V_{DD} +0.3V
V_{SIG} Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation	1.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Typical Thermal Resistance

Package	θ_{ja}
48-Lead LQFP	52°C/W

Pin Configuration



48-Lead LQFP
(top view)

Product Marking

Top Marking

Bottom Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging

**May be part of top marking*

Package may or may not include the following marks: Si or

48-Lead LQFP

Recommended Operating Conditions

Sym	Parameter	Value
V_{PP}	Positive high voltage supply[1]	+50V to +110V
V_{NN}	Negative high voltage supply[1]	-10V to V_{PP} -220V
V_{DD}	Logic power supply voltage[1]	+4.75V to +12.6V
V_{IH}	High-level input voltage	V_{DD} -1.0V to V_{DD}
V_{IL}	Low-level input voltage	0V to 1.0V
V_{SIG}	Analog signal voltage peak-to-peak[2]	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air-temperature	0°C to 70°C

Notes:

1. *Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.*
2. *V_{SIG} must be $V_{NN} \le V_{SIG} \le V_{PP}$ or floating during power up/down transition.*

DC Electrical Characteristics *(Over recommended operating conditions unless otherwise noted)*

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		min	max	min	typ	max	min	max		
R_{OnS}	Small signal switch on-resistance	-	30	-	26	32	-	40	Ω	V_{SIG} = 0V, I_{SIG} = 5.0mA, V_{PP} = 50V, V_{NN} = -170V
		-	25	-	22	27	-	35		V_{SIG} = 0V, I_{SIG} = 200mA, V_{PP} = 50V, V_{NN} = -170V
		-	25	-	22	27	-	30		V_{SIG} = 0V, I_{SIG} = 5.0mA, V_{PP} = 110V, V_{NN} = -110V
		-	20	-	18	22	-	25		V_{SIG} = 0V, I_{SIG} = 200mA, V_{PP} = 110V, V_{NN} = -110V
ΔR_{OnS}	Small signal switch on-resistance matching	-	20	-	5.0	20	-	20	%	V_{SIG} = 0V, I_{SIG} = 5.0mA, V_{PP} = 110V, V_{NN} = -110V
R_{OnL}	Large signal switch on-resistance	-	-	-	15	-	-	-	Ω	V_{SIG} = 0V, I_{SIG} = 1.0mA
I_{SOL}	Switch-off leakage per switch	-	5.0	-	1.0	10	-	15	µA	V_{SIG} = V_{PP} -10V and V_{NN} +10V
-	DC offset switch-off	300	-	-	100	300	-	300	mV	R_L = 100KΩ
	DC offset switch-on	500	-	-	100	500	-	500		R_L = 100KΩ
I_{PPQ}	Pos. HV supply current	-	-	-	10	50	-	-	µA	All SWs off
I_{NNQ}	Neg. HV supply current	-	-	-	-10	-50	-	-		
I_{PPQ}	Pos. HV supply current	-	-		10	50	-	-		All SWs on, I_{SW} = 5.0mA
I_{NNQ}	Neg. HV supply current	-	-	-	-10	-50	-	-		
-	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V_{SIG} duty cycle ≤ 0.1%
f_{SW}	Output switch frequency	-	-	-	-	50	-		KHz	Duty cycle = 50%
I_{PP}	I_{PP} supply current	-	8.1	-	-	8.8	-	10	mA	V_{PP} = 50V, V_{NN} = -170V, all SWs turning on and off at 50KHz
I_{NN}	I_{NN} supply current	-	-8.1	-	-	-8.8	-	-10		
I_{PP}	I_{PP} supply current	-	5.0	-	-	6.3	-	6.9		V_{PP} = 110V, V_{NN} = -110V, all SWs turning on and off at 50KHz
I_{NN}	I_{NN} supply current	-	-5.0	-	-	-6.3	-	-6.9		
I_{DDQ}	Logic supply quiescent current	-	10	-	-	10	-	10	µA	All logic states are at DC
I_{DD}	Logic supply average current	-	2.0	-	-	2.0	-	2.0	mA	$D_{IN}1$ = $D_{IN}2$ = 3.0MHz, $\overline{LE}$ = high

AC Electrical Characteristics *(Over recommended operating conditions unless otherwise noted)*

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		min	max	min	typ	max	min	max		
$t_{SIG(Off)}$	Time to turn off V_{SIG}*	0	-	0	-	-	0	-	ns	---
t_{WLE}	Time width of $\overline{LE}$	150	-	150	-	-	150	-	ns	---
t_{WDIN}	Time width of D_{IN}	150	-	150	-	-	150	-	ns	---
t_{SD}	Set up time before $\overline{LE}$ rises	150	-	150	-	-	150	-	ns	---

* *Time required for analog signal to turn off before output switch turns off.*

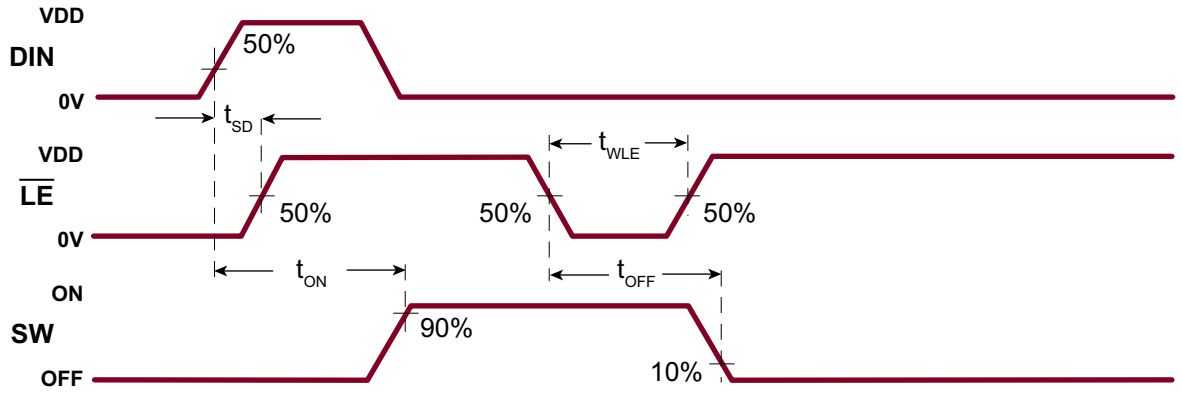
AC Electrical Characteristics *(cont.)*

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		min	max	min	typ	max	min	max		
t_{On}	Turn-on time	-	5.0	-	-	5.0	-	5.0	µs	V_{SIG} = V_{PP} -10V, R_{LOAD} = 10KΩ
t_{Off}	Turn-off time	-	5.0	-	-	5.0	-	5.0	µs	V_{SIG} = V_{PP} -10V, R_{LOAD} = 10KΩ
K_O	Off isolation	-30	-	-30	-33	-	-30	-	dB	f = 5.0MHz, 1.0KΩ/15pF Load
		-45	-	-45	-50	-	-45	-	dB	f = 7.5MHz, R_{LOAD} = 50Ω
K_{CR}	Switch crosstalk	-45	-	-45	-	-	-45	-	dB	f = 5.0MHz, R_{LOAD} = 50Ω
$C_{GS(Off)}$	Off-capacitance switch to GND	5.0	17	5.0	12	17	5.0	17	pF	V_{SIG} = 0V, 1.0MHz
$C_{GS(On)}$	On-capacitance switch to GND	25	50	25	38	50	25	50	pF	V_{SIG} = 0V, 1.0MHz
$+V_{SPK}$	Output voltage spike	-	-	-	4.0	-	-	-	V	---
$-V_{SPK}$		-	-	-	-4.0	-	-	-		---

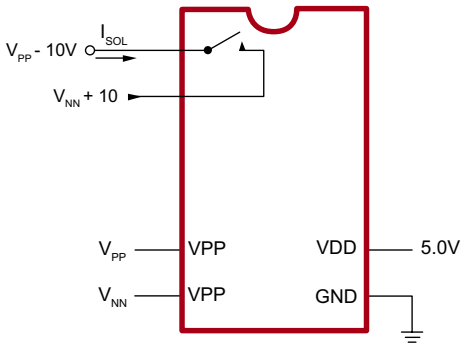
Logic Truth Table

$D_{IN}2$	$D_{IN}1$	$\overline{LE}$	SW0 to SW7	SW8 to SW15
L	L	L	Off	Off
L	H	L	On	Off
H	L	L	Off	On
H	H	L	On	On
X	X	H	Hold Previous State	

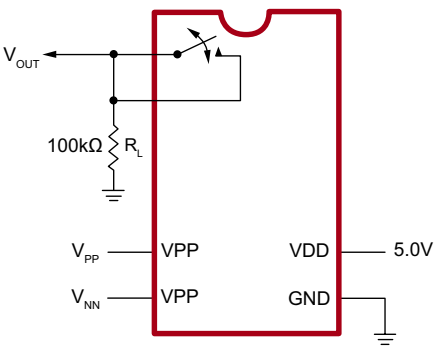
Logic Timing Waveform



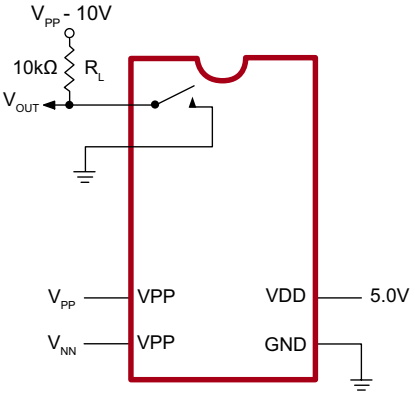
Test Circuits



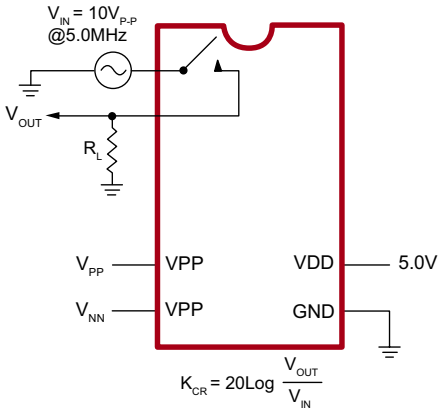
Switch Off Leakage



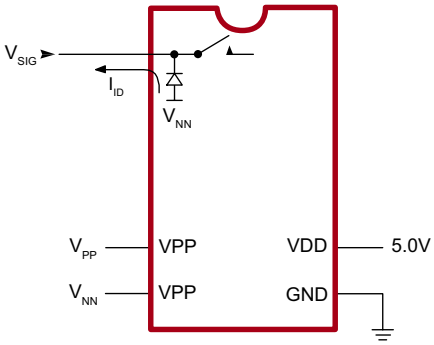
DC Offset ON/OFF



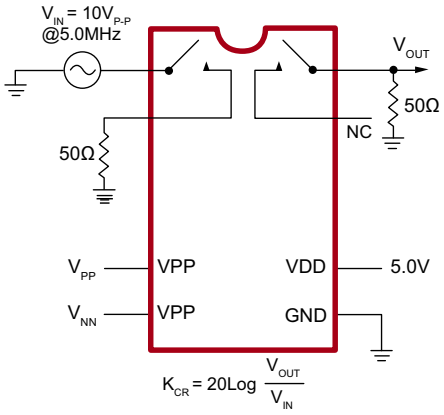
T_{ON}/T_{OFF} Test Circuit



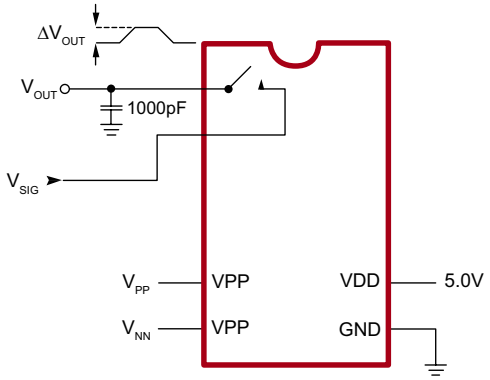
OFF Isolation



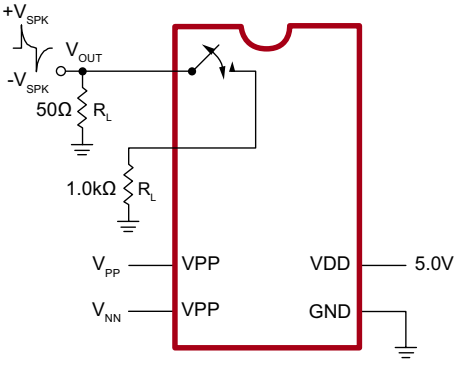
Isolation Diode Current



Crosstalk



Q = 1000pF x ΔV_{OUT}
Charge Injection



Output Voltage Spike

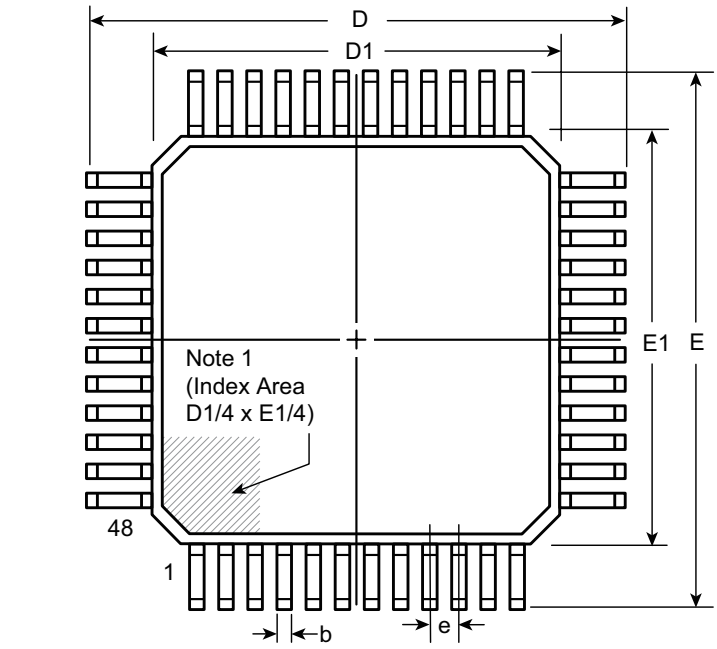
Pin Description

Pin #	Function
1	VNN
2	N/C
3	VPP
4	N/C
5	$D_{IN}1$
6	$\overline{LE}$
7	$D_{IN}2$
8	N/C
9	N/C
10	VDD
11	GND
12	N/C
13	N/C
14	SW15
15	SW15
16	SW14
17	SW14
18	SW13
19	SW13
20	SW12
21	SW12
22	SW11
23	SW11
24	N/C

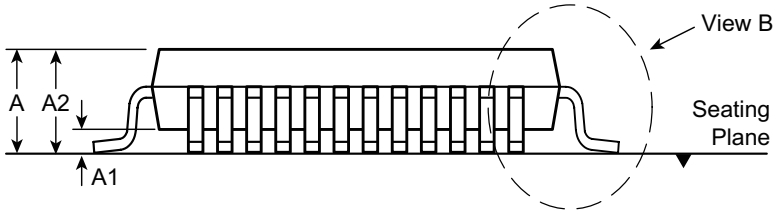
Pin #	Function
25	SW10
26	SW10
27	SW9
28	SW9
29	SW8
30	SW8
31	SW7
32	SW7
33	SW6
34	SW6
35	SW5
36	SW5
37	SW4
38	N/C
39	SW4
40	N/C
41	SW3
42	SW3
43	SW2
44	SW2
45	SW1
46	SW1
47	SW0
48	SW0

48-Lead LQFP Package Outline (FG)

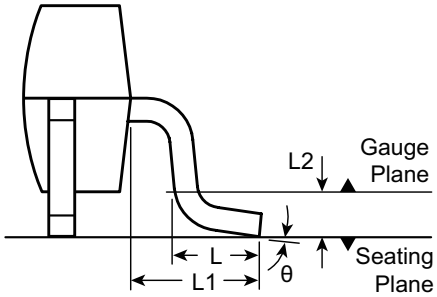
7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Top View



Side View



View B

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75			7°

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.
** This dimension is not specified in the JEDEC drawing.*

Drawings are not to scale.

Supertex Doc. #: *DSPD-48LQFPFG Version, D041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.
1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com