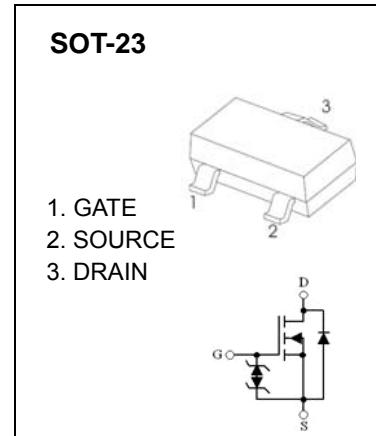


SOT-23 Plastic-Encapsulate MOSFETs

CJ8820 N-Channel Enhancement Mode Field Effect Transistor

DESCRIPTION

The CJ8820 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. It is ESD protected. This device is suitable for use as a uni-directional or bi-directional load switch, facilitated by its common-drain configuration.



Maximum ratings ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Units
Drain-source voltage	V_{DS}	20	V
Gate-source voltage	V_{GS}	± 12	V
Continuous drain current ($t \leq 10\text{s}$)	I_D	7	A
Pulsed drain current *	I_{DM}	25	A
Power dissipation	P_D	0.3	W
Thermal resistance from junction to ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction temperature	T_J	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55~150	$^\circ\text{C}$

* Repetitive rating : Pulse width limited by junction temperature.

Electrical characteristics ($T_a=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$	20			V
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}$			1	μA
Gate-body leakage current	I_{GSS}	$V_{GS} = \pm 10\text{V}, V_{DS} = 0\text{V}$			± 10	μA
Gate threshold voltage (note 1)	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	0.5		1.1	V
Drain-source on-resistance (note 1)	$R_{DS(\text{on})}$	$V_{GS} = 10\text{V}, I_D = 7\text{A}$			21	$\text{m}\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 6.6\text{A}$			24	$\text{m}\Omega$
		$V_{GS} = 3.6\text{V}, I_D = 6\text{A}$			28	$\text{m}\Omega$
		$V_{GS} = 2.5\text{V}, I_D = 5.5\text{A}$			32	$\text{m}\Omega$
		$V_{GS} = 1.8\text{V}, I_D = 2\text{A}$			50	$\text{m}\Omega$
Forward transconductance (note 1)	g_{FS}	$V_{DS} = 5\text{V}, I_D = 7\text{A}$		20		S
Diode forward voltage(note 1)	V_{SD}	$I_S = 1\text{A}, V_{GS} = 0\text{V}$			1	V
SWITCHING PARAMETERS(note 2)						
Turn-on delay time	$t_{d(\text{on})}$	$V_{GS}=5\text{V}, V_{DS}=10\text{V}, R_L=1.4\Omega, R_{\text{GEN}}=3\Omega$		7		ns
Turn-on rise time	t_r			13		ns
Turn-off delay time	$t_{d(\text{off})}$			29		ns
Turn-off fall time	t_f			11		ns
Total Gate Charge	Q_g	$V_{DS} = 10\text{V}, V_{GS} = 4.5\text{V}, I_D = 7\text{A}$			12	nC
Gate-Source Charge	Q_{gs}				1.2	nC
Gate-Drain Charge	Q_{gd}				3	nC

Notes :

1. Pulse Test : Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 0.5\%$.
2. Guaranteed by design, not subject to production testing.

