Low Skew, 1:6 Crystal-to-LVCMOS Fanout Buffer

83905-01

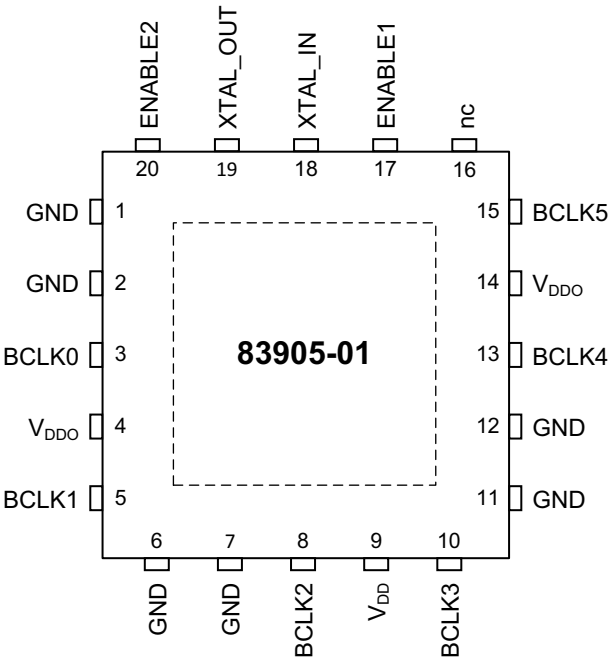
DATA SHEET

General Description

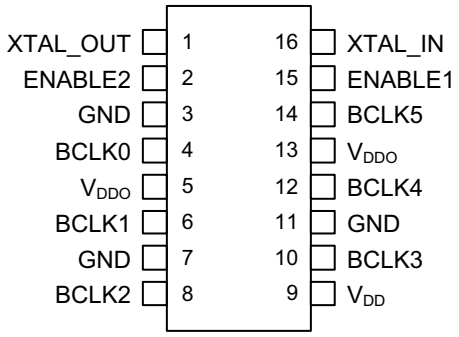
The 83905-01 is a low skew, 1-to-6 LVCMOS Fanout Buffer. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 6 to 12 by utilizing the ability of the outputs to drive two series terminated lines.

The 83905-01 is characterized at full 1.8V, 1.5V, and 1.2V, mixed 1.8V/1.5V, 1.8V/1.2V and 1.5V/1.2V output operating supply mode. Guaranteed output skew characteristics along with the 1.2V output capabilities makes the 83905-01 ideal for high performance, single ended applications that also require a limited output voltage.

Pin Assignments



20-pin, 4mm x 4mm VFQFN Package



83905-01

16-pin, 4.4mm x 5.0mm TSSOP Package

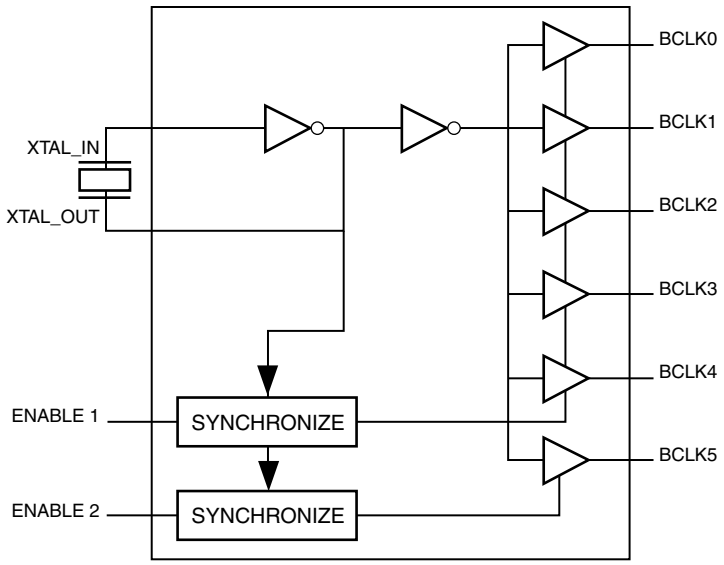
Features

- Six LVCMOS outputs
- Outputs able to drive 12 series terminated lines
- Crystal Oscillator Interface
- Crystal input frequency range: 10MHz to 40MHz
- Output skew: 95ps (maximum)
- RMS phase jitter @ 25MHz, (100Hz – 1MHz): 0.17ps (typical)

Offset	Noise Power
100Hz	-115 dBc/Hz
1kHz	-138 dBc/Hz
10kHz	-154 dBc/Hz
100kHz	-160 dBc/Hz

- Synchronous output enables
- Power supply modes: Full 1.8V, 1.5V, 1.2V
  Mixed 1.8V core/1.5V output operating supply
  Mixed 1.8V core/1.2V output operating supply
  Mixed 1.5V core/1.2V output operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Name	Type	Description
XTAL_OUT	Output	Crystal oscillator interface.
XTAL_IN	Input	Crystal oscillator interface.
ENABLE1, ENABLE2	Input	Clock enable. LVCMOS/LVTTL interface levels. See Table 3.
BCLK0, BCLK1, BCLK2, BCLK3, BCLK4, BCLK5	Output	Clock outputs. LVCMOS interface levels.
GND	Power	Power supply ground.
V_{DD}	Power	Power supply pin.
V_{DDO}	Power	Output supply pin.
nc	Unused	No connect.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	ENABLE[2:1]			4		pF
C_{PD}	Power Dissipation Capacitance (per output)		V_{DDO} = 2.0V		12		pF
			V_{DDO} = 1.6V		12		pF
			V_{DDO} = 1.26V		12		pF
R_{OUT}	Output Impedance		V_{DDO} = 1.8V ± 0.2V		17		Ω
			V_{DDO} = 1.5V ± 0.1V		18		Ω
			V_{DDO} = 1.2V ± 5%		24		Ω

Function Table

Table 3. Clock Enable Function Table

Control Inputs		Outputs	
ENABLE 1	**ENABLE2**	**BCLK[0:4]**	**BCLK5**
0	0	LOW	LOW
0	1	LOW	Toggling
1	0	Toggling	LOW
1	1	Toggling	Toggling

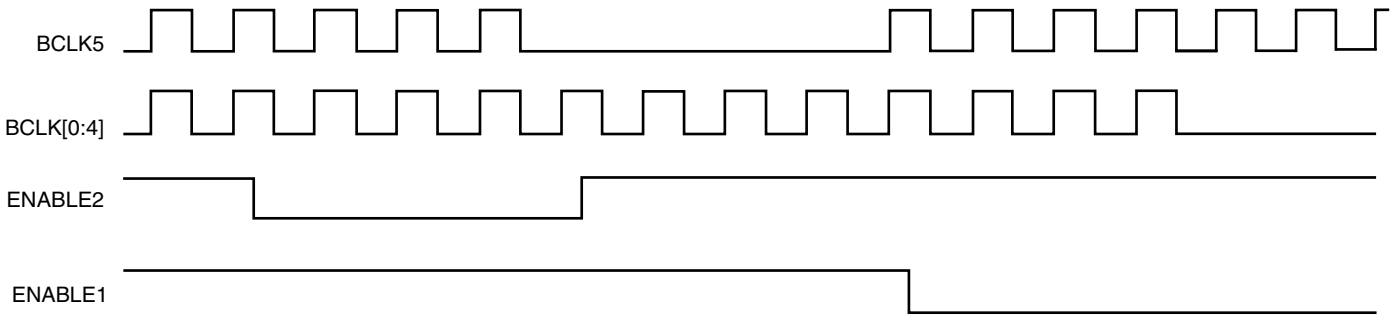


Figure 1. Enable Timing Diagram

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Input, V_I Crystal Oscillator Input	0V to V_{DD}
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, T_J	125°C
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		1.6	1.8	2.0	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}; NOTE 1	Power Supply Current	ENABLE [1:2] = 00		4	10	mA
I_{DDO}; NOTE 1	Output Supply Current	ENABLE [1:2] = 00			1	mA

NOTE 1: Measured with outputs unterminated, and XTAL_IN and XTAL_OUT floated.

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 1.5V \pm 0.1V$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		1.4	1.5	1.6	V
V_{DDO}	Output Supply Voltage		1.4	1.5	1.6	V
I_{DD}; NOTE 1	Power Supply Current	ENABLE [1:2] = 00		3	7	mA
I_{DDO}; NOTE 1	Output Supply Current	ENABLE [1:2] = 00			1	mA

NOTE 1: Measured with outputs unterminated, and XTAL_IN and XTAL_OUT floated.

Table 4C. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 1.2V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		1.14	1.2	1.26	V
V_{DDO}	Output Supply Voltage		1.14	1.2	1.26	V
I_{DD}; NOTE 1	Power Supply Current	ENABLE [1:2] = 00		2	6	mA
I_{DDO}; NOTE 1	Output Supply Current	ENABLE [1:2] = 00			1	mA

NOTE 1: Measured with outputs unterminated, and XTAL_IN and XTAL_OUT floated.

Table 4D. Power Supply DC Characteristics, V_{DD} = 1.8V ±0.2V, V_{DDO} = 1.5V ±0.1V, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		1.6	1.8	2.0	V
V_{DDO}	Output Supply Voltage		1.4	1.5	1.6	V
I_{DD}; NOTE 1	Power Supply Current	ENABLE [1:2] = 00		4	10	mA
I_{DDO}; NOTE 1	Output Supply Current	ENABLE [1:2] = 00			1	mA

NOTE 1: Measured with outputs unterminated, and XTAL_IN and XTAL_OUT floated.

Table 4E. Power Supply DC Characteristics, V_{DD} = 1.8V ±0.2V, V_{DDO} = 1.2V ±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		1.6	1.8	2.0	V
V_{DDO}	Output Supply Voltage		1.14	1.2	1.26	V
I_{DD}; NOTE 1	Power Supply Current	ENABLE [1:2] = 00		4	10	mA
I_{DDO}; NOTE 1	Output Supply Current	ENABLE [1:2] = 00			1	mA

NOTE 1: Measured with outputs unterminated, and XTAL_IN and XTAL_OUT floated.

Table 4F. Power Supply DC Characteristics, V_{DD} = 1.5V ±0.1V, V_{DDO} = 1.2V ±5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		1.4	1.5	1.6	V
V_{DDO}	Output Supply Voltage		1.14	1.2	1.26	V
I_{DD}; NOTE 1	Power Supply Current	ENABLE [1:2] = 00		3	7	mA
I_{DDO}; NOTE 1	Output Supply Current	ENABLE [1:2] = 00			1	mA

NOTE 1: Measured with outputs unterminated, and XTAL_IN and XTAL_OUT floated.

Table 4G. LVCMOS/LVTTL DC Characteristics, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	V_{DD} = 1.8V ± 0.2V	1.2		V_{DD} + 0.3	V
		V_{DD} = 1.5V ± 0.1V	1.0		V_{DD} + 0.3	V
		V_{DD} = 1.2V ± 5%	0.8		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 1.8V ± 0.2V	-0.3		0.4	V
		V_{DD} = 1.5V ± 0.1V	-0.3		0.3	V
		V_{DD} = 1.2V ± 5%	-0.3		0.2	V
V_{OH}	Output High Voltage; NOTE 1	V_{DDO} = 1.8V ± 0.2V	0.7			V
		V_{DDO} = 1.5V ± 0.1V	0.7			V
		V_{DDO} = 1.2V ± 5%	0.7			V
V_{OL}	Output Low Voltage; NOTE 1	V_{DDO} = 1.8V ± 0.2V			0.4	V
		V_{DDO} = 1.5V ± 0.1V			0.4	V
		V_{DDO} = 1.2V ± 5%			0.4	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement Information, *Output Load Test Circuit diagrams.*

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		10		40	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Load Capacitance			12	18	pF

AC Electrical Characteristics

Table 6A. AC Characteristics, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source NOTE 1		1		100	MHz
*t*sk(o)	Output Skew; NOTE 2, 3					90	ps
tjit	RMS Phase Jitter (Random); NOTE 4		25MHz, Integration Range: 100Hz – 1MHz		0.17		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		600	ps
odc	Output Duty Cycle			42	50	58	%
t_{EN}	Output Enable Time; NOTE 5	ENABLE1				4	cycles
		ENABLE2				4	cycles
t_{DIS}	Output Disable Time; NOTE 5	ENABLE1				4	cycles
		ENABLE2				4	cycles

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at $f \leq 40$MHz using a crystal input unless noted otherwise. Outputs terminated with 50Ω to $V_{DDO}/2$.
NOTE 1: XTAL_IN can be overdriven by an external source.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: See phase noise plot.
NOTE 5: These parameters are guaranteed by design. Not tested in production.

Table 6B. AC Characteristics, $V_{DD} = V_{DDO} = 1.5V \pm 0.1V$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source; NOTE 1		1		100	MHz
*t*sk(o)	Output Skew; NOTE 2, 3					90	ps
tjit	RMS Phase Jitter (Random)		25MHz, Integration Range: 100Hz – 1MHz		0.3		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		650	ps
odc	Output Duty Cycle			44	50	56	%
t_{EN}	Output Enable Time; NOTE 4	ENABLE1				4	cycles
		ENABLE2				4	cycles
t_{DIS}	Output Disable Time; NOTE 4	ENABLE1				4	cycles
		ENABLE2				4	cycles

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at $f \leq 40$MHz using a crystal input unless noted otherwise. Outputs terminated with 50Ω to $V_{DDO}/2$.
NOTE 1: XTAL_IN can be overdriven by an external source.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: These parameters are guaranteed by design. Not tested in production.

Table 6C. AC Characteristics, $V_{DD} = V_{DDO} = 1.2V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source; NOTE 1		1		100	MHz
*t*sk(o)	Output Skew; NOTE 2, 3					90	ps
tjit	RMS Phase Jitter (Random)		25MHz, Integration Range: 100Hz – 1MHz		0.7		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	350		800	ps
odc	Output Duty Cycle			44	50	56	%
t_{EN}	Output Enable Time; NOTE 4	ENABLE1				4	cycles
		ENABLE2				4	cycles
t_{DIS}	Output Disable Time; NOTE 4	ENABLE1				4	cycles
		ENABLE2				4	cycles

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at $f \leq 40$MHz using a crystal input unless noted otherwise. Outputs terminated with 50Ω to $V_{DDO}/2$.
NOTE 1: XTAL_IN can be overdriven by an external source.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: These parameters are guaranteed by design. Not tested in production.

Table 6D. AC Characteristics, V_{DD} = 1.8V ±0.2V, V_{DDO} = 1.5V ±0.1V, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source; NOTE 1		1		100	MHz
*t*sk(o)	Output Skew; NOTE 2, 3					90	ps
tjit	RMS Phase Jitter (Random)		25MHz, Integration Range: 100Hz – 1MHz		0.18		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		650	ps
odc	Output Duty Cycle			40	50	60	%
t_{EN}	Output Enable Time; NOTE 4	ENABLE1				4	cycles
		ENABLE2				4	cycles
t_{DIS}	Output Disable Time; NOTE 4	ENABLE1				4	cycles
		ENABLE2				4	cycles

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at $f \leq$ 40MHz using a crystal input unless noted otherwise. Outputs terminated with 50Ω to V_{DDO}/2.
NOTE 1: XTAL_IN can be overdriven by an external source.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: These parameters are guaranteed by design. Not tested in production.

Table 6E. AC Characteristics, V_{DD} = 1.8V ±0.2V, V_{DDO} = 1.2V ±5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source; NOTE 1		1		100	MHz
*t*sk(o)	Output Skew; NOTE 2, 3					95	ps
tjit	RMS Phase Jitter (Random)		25MHz, Integration Range: 100Hz – 1MHz		0.2		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	350		800	ps
odc	Output Duty Cycle			42	50	58	%
t_{EN}	Output Enable Time; NOTE 4	ENABLE1				4	cycles
		ENABLE2				4	cycles
t_{DIS}	Output Disable Time; NOTE 4	ENABLE1				4	cycles
		ENABLE2				4	cycles

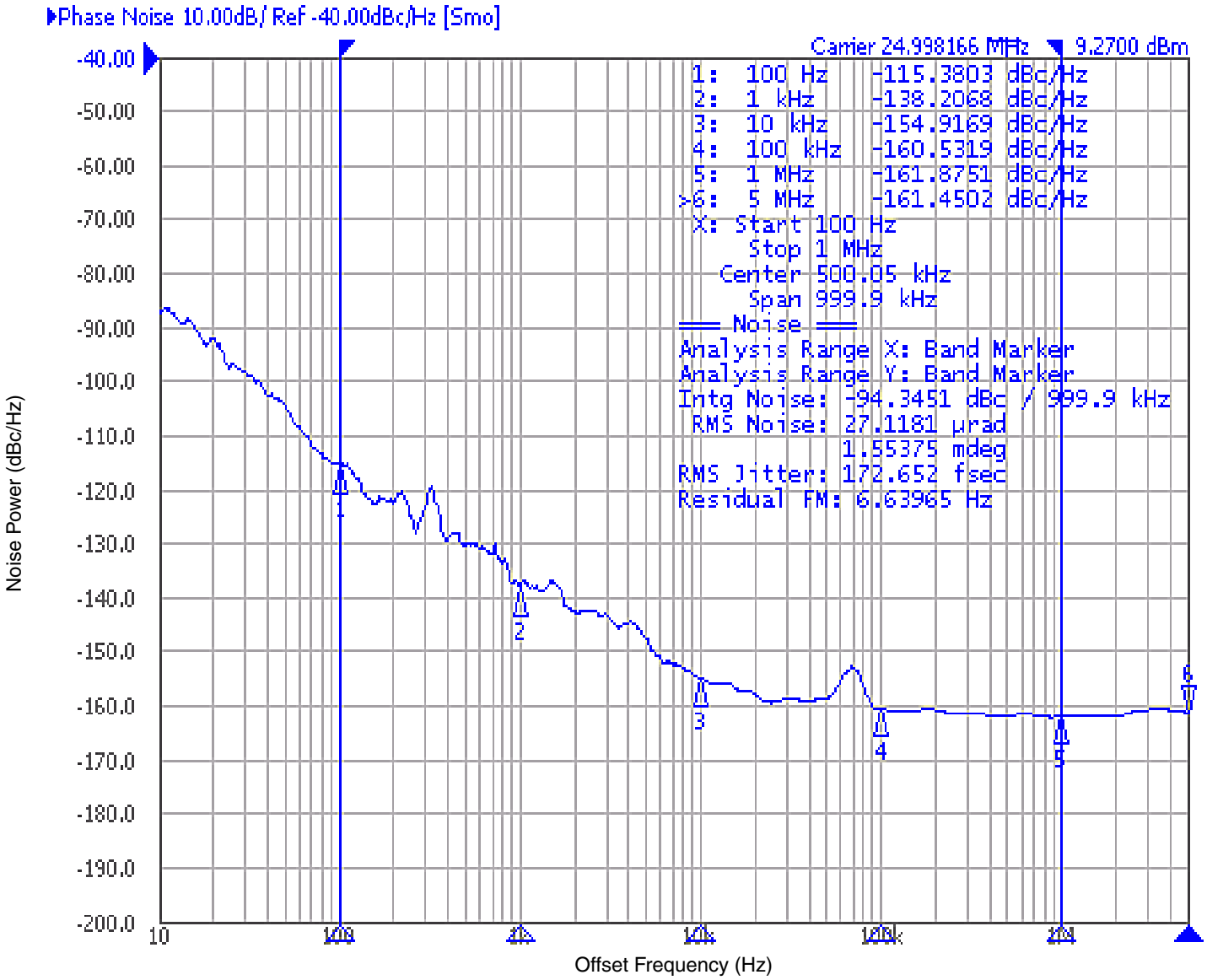
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at $f \leq$ 40MHz using a crystal input unless noted otherwise. Outputs terminated with 50Ω to V_{DDO}/2.
NOTE 1: XTAL_IN can be overdriven by an external source.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: These parameters are guaranteed by design. Not tested in production.

Table 6F. AC Characteristics, V_{DD} = 1.5V ±0.1V, V_{DDO} = 1.2V ±5%, T_A = 0°C to 70°C

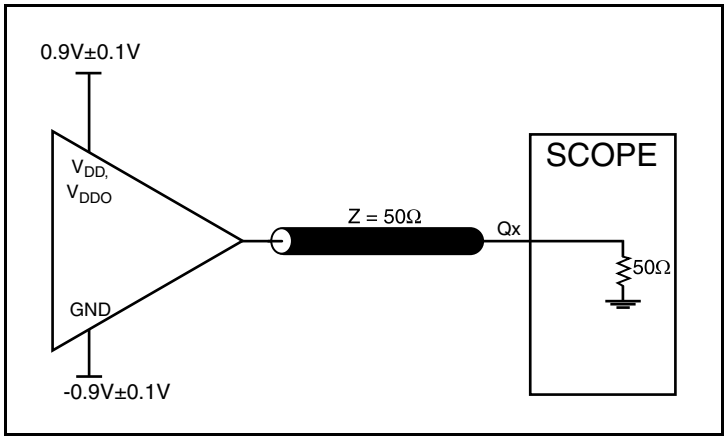
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source; NOTE 1		1		100	MHz
*t*sk(o)	Output Skew; NOTE 2, 3					90	ps
tjit	RMS Phase Jitter (Random)		25MHz, Integration Range: 100Hz – 1MHz		0.34		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	350		800	ps
odc	Output Duty Cycle			42	50	58	%
t_{EN}	Output Enable Time; NOTE 4	ENABLE1				4	cycles
		ENABLE2				4	cycles
t_{DIS}	Output Disable Time; NOTE 4	ENABLE1				4	cycles
		ENABLE2				4	cycles

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
All parameters measured at $f \leq$ 40MHz using a crystal input unless noted otherwise. Outputs terminated with 50Ω to V_{DDO}/2.
NOTE 1: XTAL_IN can be overdriven by an external source.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at V_{DDO}/2.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: These parameters are guaranteed by design. Not tested in production.

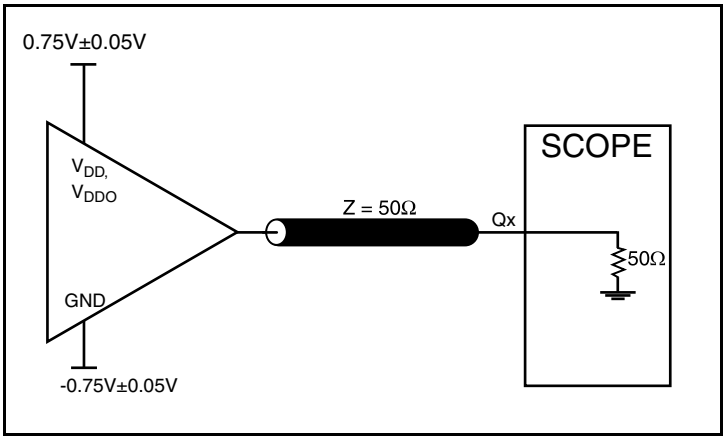
Typical Phase Noise at 25MHz (1.8V Core, 1.8V Output)



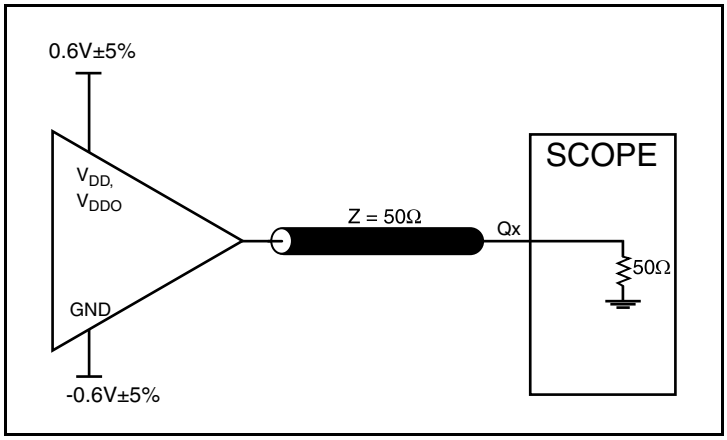
Parameter Measurement Information



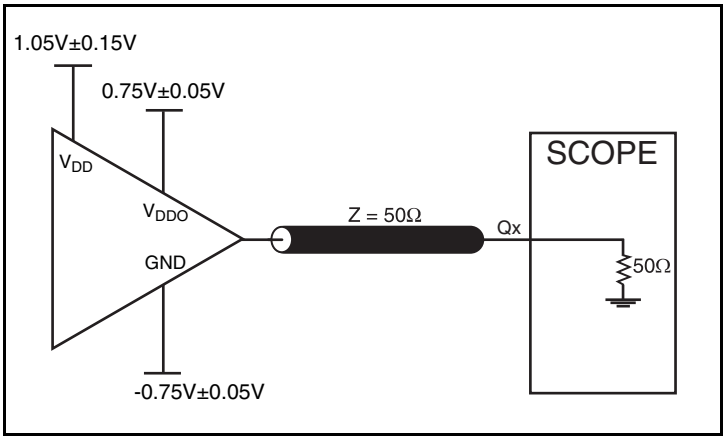
1.8V Core/1.8V LVCMOS Output Load Test Circuit



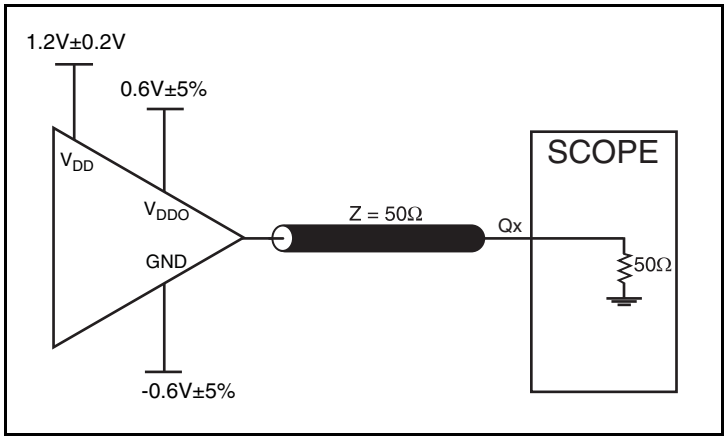
1.5V Core/1.5V LVCMOS Output Load Test Circuit



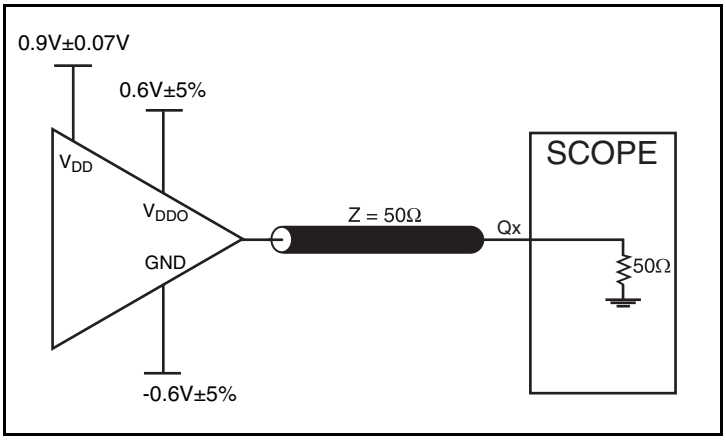
1.2V Core/1.2V LVCMOS Output Load Test Circuit



1.8V Core/1.5V LVCMOS Output Load Test Circuit

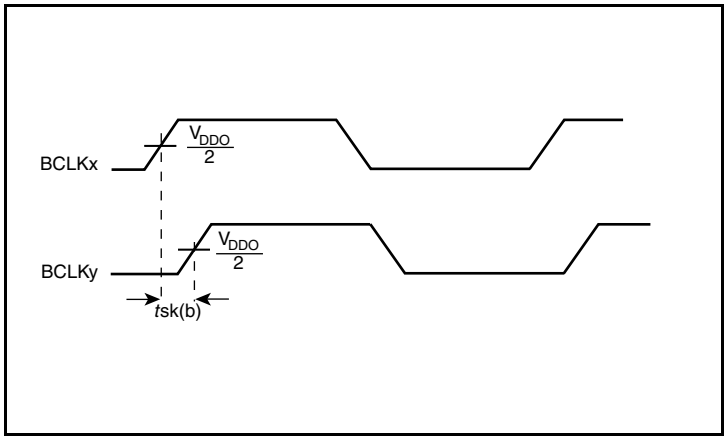


1.8V Core/1.2V LVCMOS Output Load Test Circuit

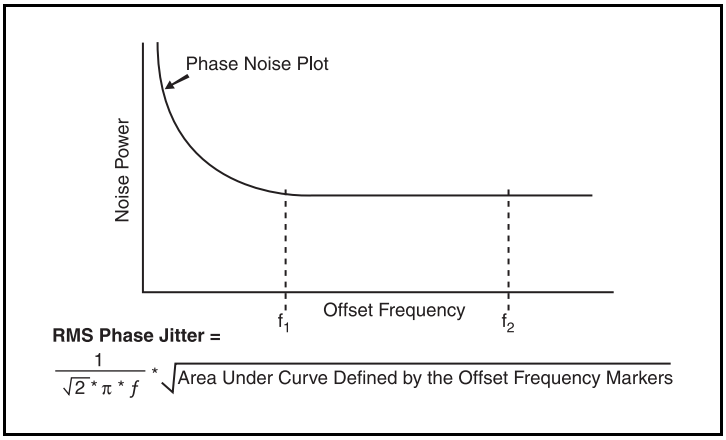


1.5V Core/1.2V LVCMOS Output Load Test Circuit

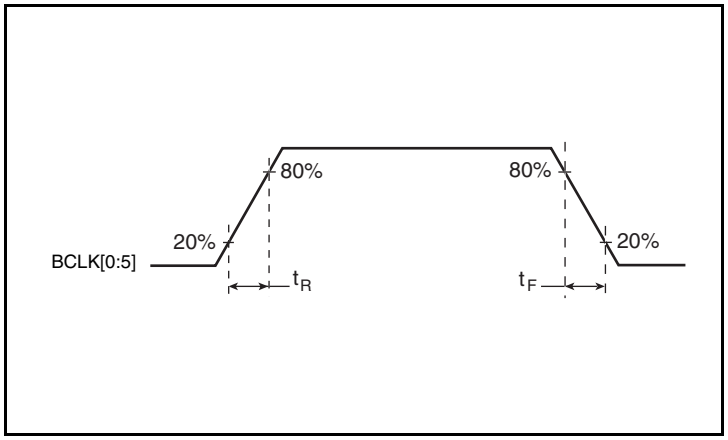
Parameter Measurement Information, continued



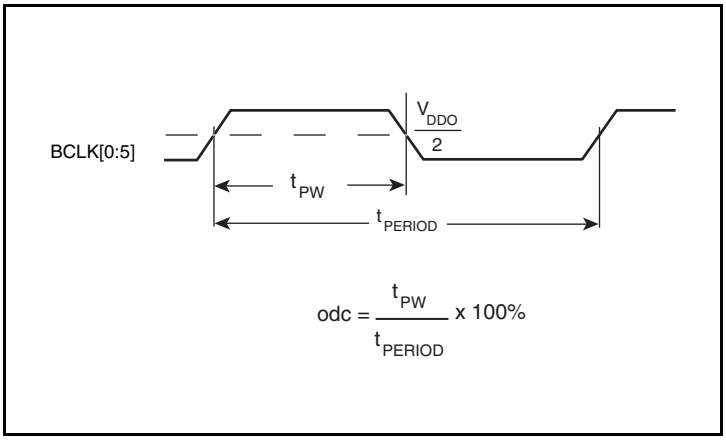
Output Skew



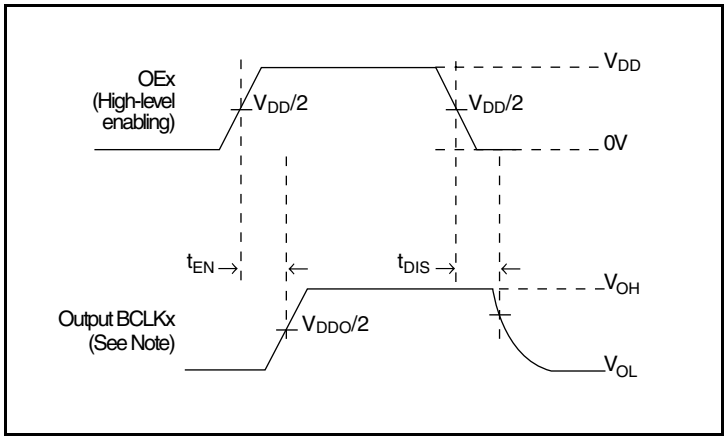
RMS Phase Jitter



Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Output Enable/Disable

Application Information

Recommendations for Unused Output Pins

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Crystal Input Interface

The 83905-01 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

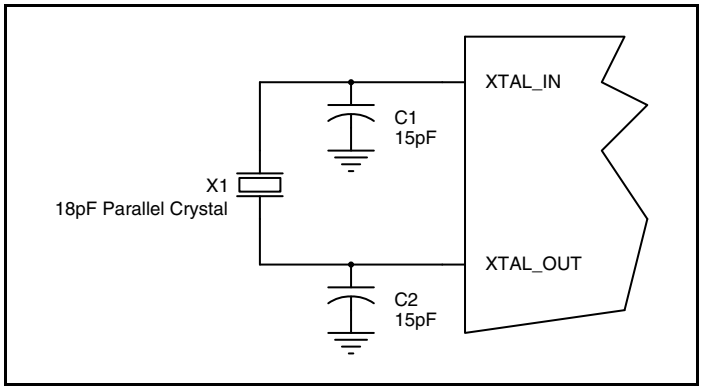


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

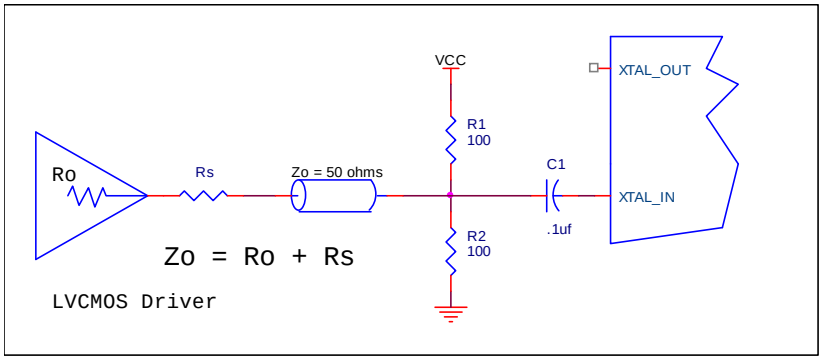


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

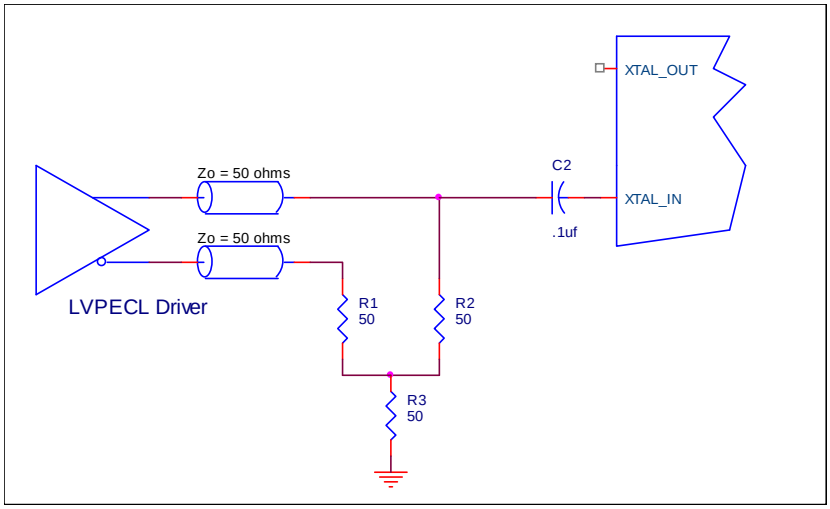


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Schematic Example

Figure 4 shows an example of the 83905-01 application schematic. In this example, the device is operated at V_{DD} = V_{DDO} = 1.8V. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by an 18pF load resonant quartz crystal. The tuning capacitors C1 and C2 are fairly accurate, but minor adjustments might be required. For the LVCMOS output drivers, two termination examples are shown in this schematic. For additional termination examples, see LVCMOS Termination Application Note.

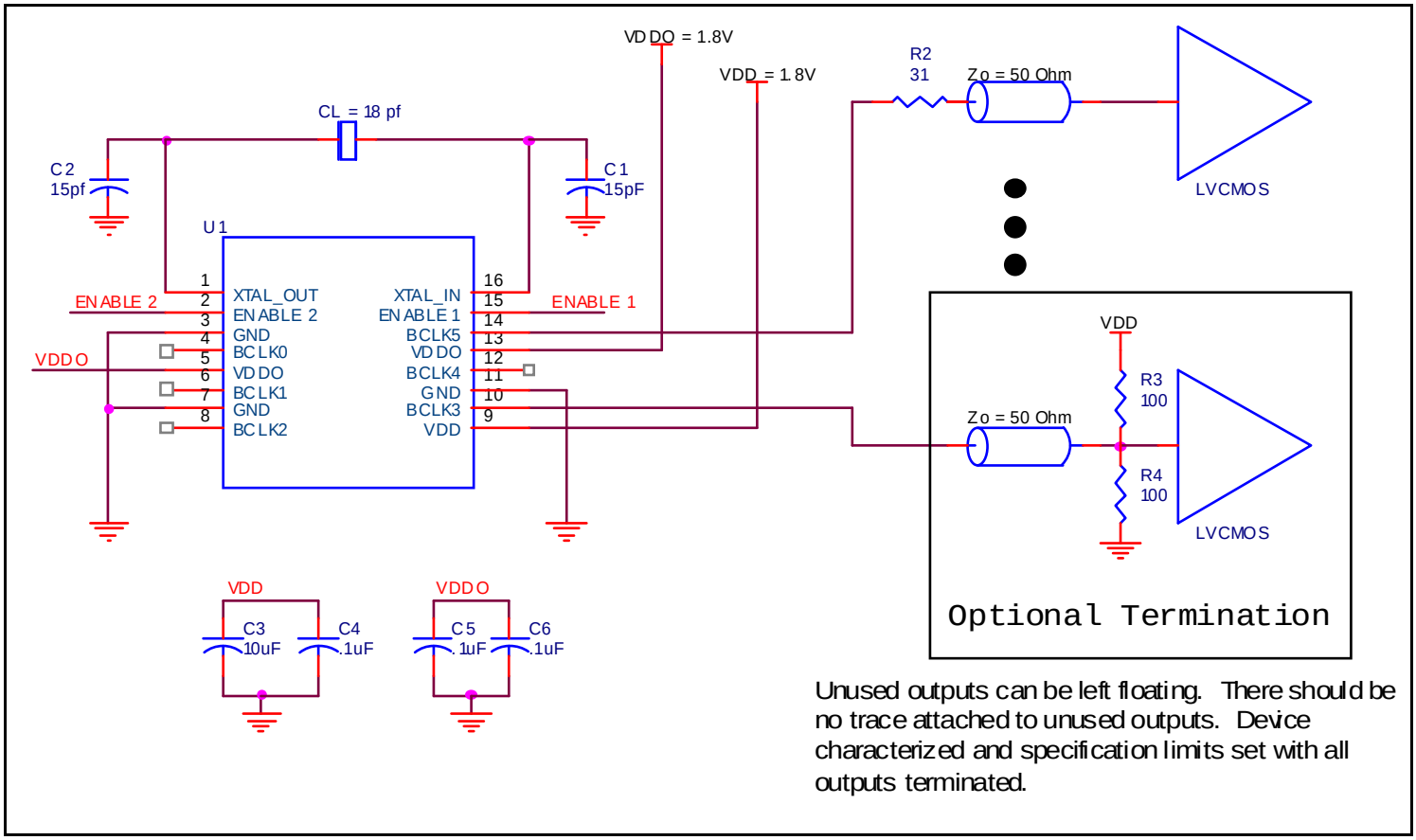


Figure 4. 83905-01 Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the 83905-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 83905-01 is the sum of the core power plus the analog power plus the power dissipated due to the load. The following is the power dissipation for V_{DD} = 1.8V + 0.2V = 2.0V, which gives worst case results.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD}$ = 2V * 10mA = **20mW**
- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DD}/2$
  Output Current $I_{OUT} = V_{DD\_MAX} / [2 * (50Ω + R_{OUT})]$ = 2V / [2 * (50Ω + 17Ω)] = **14.9mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power $(R_{OUT}) = R_{OUT} * (I_{OUT})^2$ = 17Ω * (14.9mA)^2 = **3.8mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 3.8mW * 6 = **22.8mW**

Dynamic Power Dissipation at 100MHz

Power (100MHz) = C_{PD} * Frequency * $(V_{DD})^2$ = 12pF * 100MHz * (2V)^2 = **4.8mW per output**
Total Power (100MHz) = 4.8mW * 6 = **28.8mW**

Total Power Dissipation

- **Total Power**
  = Power $(core)_{MAX}$ + Total Power (R_{OUT}) + Total Power (100MHz)
  = 20mW + 22.8mW + 28.8mW
  = 71.6mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 100.3°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.072W *100.3°C/W = 77.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 16-Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

Reliability Information

Table 8A. θ_{JA} vs. Air Flow Table for a 16-Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	100.3°C/W	96.0°C/W	93.9°C/W

Table 8B. θ_{JA} vs. Air Flow Table for a 20-Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	57.5°C/W	50.3°C/W	45.1°C/W

Transistor Count

The transistor count for 83905-01: 505

16-Lead TSSOP Package Outline and Package Dimensions

Package Outline - G Suffix for 16-Lead TSSOP

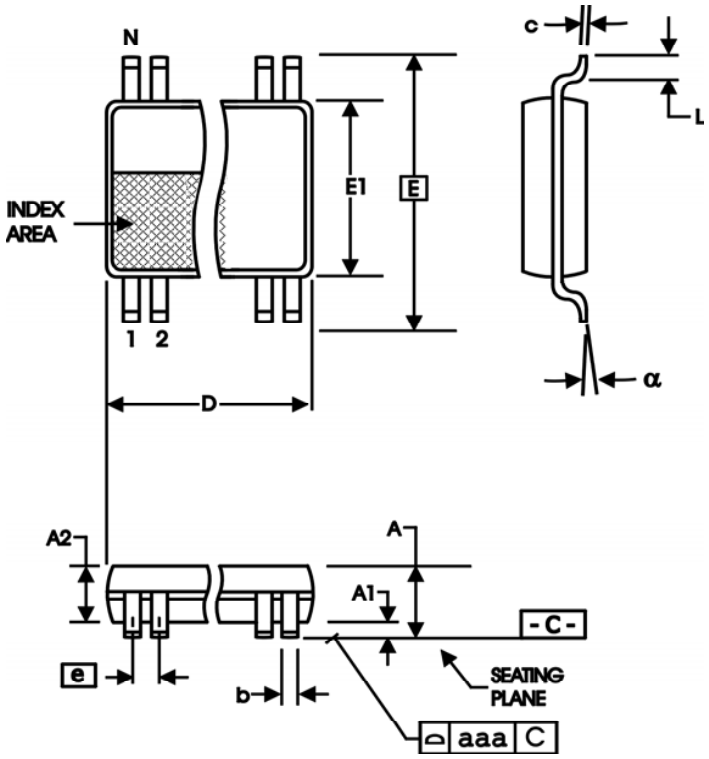


Table 9A. Package Dimensions for 16-Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

20-Lead VFQFN Package Outline and Package Dimensions

Package Outline - K Suffix for 20-Lead VFQFN

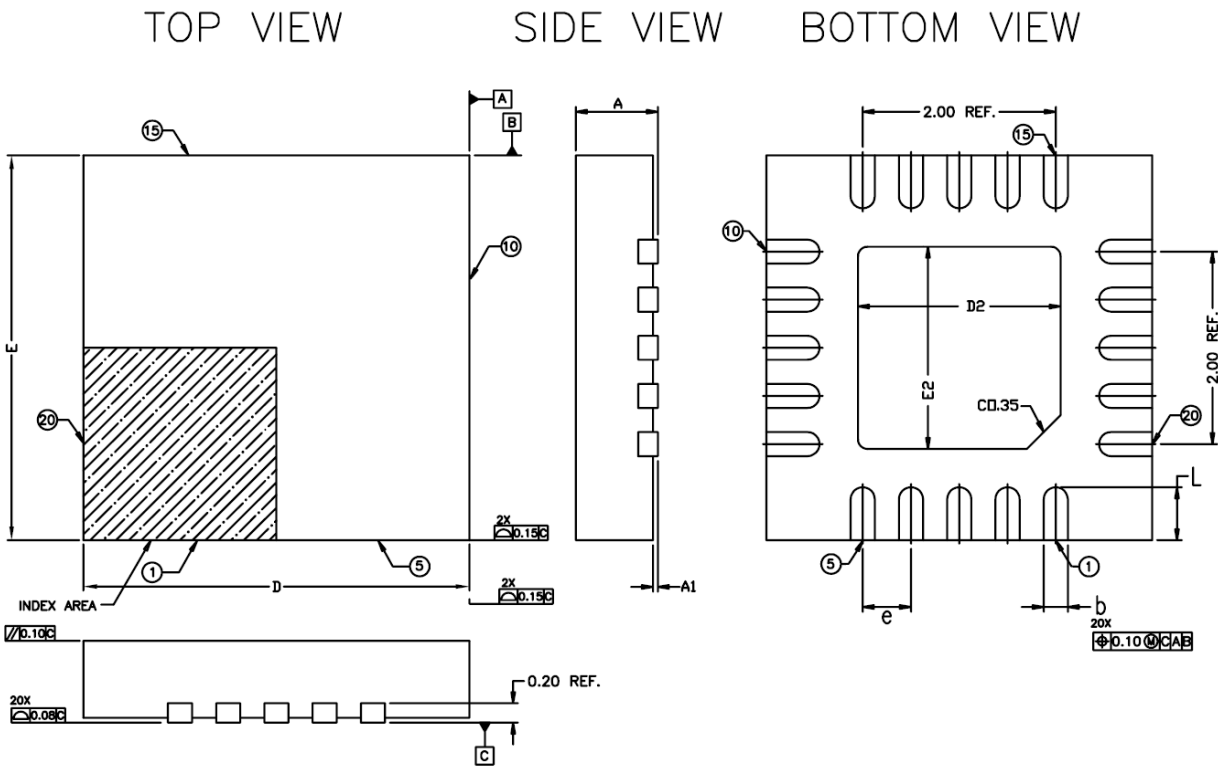


Table 9C. Package Dimensions for 20-Lead VFQFN

All Dimensions in Millimeters			
Symbol	**Minimum**	**Nom**	**Maximum**
b	0.20	0.25	0.30
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	1.95	2.10	2.25
E2	1.95	2.10	2.25
L	0.45	0.55	0.65
e	0.50 BSC		
N	20		
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.2 REF		

Reference Document: JEDEC Publication 95, MO-220

NOTE:

The drawing and dimension data originate from IDT package outline drawing PSC-4170, rev03.

1. Dimensions and tolerances conform to ASME Y14.5M-1994
2. All dimensions are in millimeters. All angles are in degrees.
3. N is the total number of terminals.
4. All specifications comply with JEDEC MO-220.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83905AG-01LF	3905A01L	16-Lead TSSOP, Lead-Free	Tube	0°C to 70°C
83905AG-01LFT	3905A01L	16-Lead TSSOP, Lead-Free	Tape & Reel	0°C to 70°C
83905AK-01LF	5A01L	20-Lead VFQFN, Lead-Free	Tray	0°C to 70°C
83905AK-01LFT	5A01L	20-Lead VFQFN, Lead-Free	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com

Tech Support
email: clocks@idt.com