Standard Products

UT700 32-bit Fault-Tolerant SPARC™ V8/LEON 3FT Processor

Datasheet
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www.aeroflex.com/LEON

FEATURES

- Supports up to 166 MHz clock rate
- Separate instruction and data cache architecture
- High-performance fully pipelined IEEE-754 FPU
- Enhanced pipeline with 1.2 DMIPS / MHz performance
- Implemented on 130nm CMOS technology
- Internally configured clock network
- Power saving 1.2V core power supply
- 3.3V I/O compatibility
- Hardened-by-design flip-flops and memory cells
- Reed Solomon EDAC
- Multifunctional memory controller
- 10/100 Base-T Ethernet port for VxWorks development
- Integrated PCI 2.2 compatible core
- Four integrated multi-protocol SpaceWire nodes that support the RMAP protocol
- SPI interface
- Two CAN 2.0 compliant bus interfaces
- MIL-STD-1553 BC/RT/MT
- -55°C to +105°C temperature range
- Operational environment:
  - Intrinsic total-dose: 100 krad(Si)
  - SEL Immune ≤110 MeV-cm^2/mg
- Packaging options:
  - 484-pin Ceramic Land Grid, Column Grid and Ball Grid Array packages
- Standard Microcircuit Drawing 5962-13238
  - QML Q, Q+, and V
- Applications
  - Nuclear power plant controls
  - Critical transportation systems
  - High-altitude avionics
  - Medical electronics
  - X-Ray cargo scanning
  - Spaceborne computer
  - System controller boards
  - Avionics processing boards

INTRODUCTION

The UT700 features a seven stage pipelined monolithic, high-performance, fault-tolerant SPARC™ V8/LEON 3FT Processor. L1 cache consists of 16kB for both instruction and data caches. A Reed Solomon EDAC provides fault-tolerant protection for SDRAM. Integer performance is 1.2 DMIPS / MHz. RMAP protocol is supported for all four SpaceWire ports. The UT700 provides a 32-bit master/target PCI interface, including a 16 bit user I/O interface for off-chip peripherals. A compliant 2.0 AMBA bus interface integrates the on-chip LEON 3FT, SpaceWire, Ethernet, memory controller, cPCI, CAN bus, MIL-STD-1553, SPI and programmable interrupt peripherals.

The UT700 is SPARC V8 compliant; therefore, developers may use industry standard compilers, kernels, and development tools. A full software development suite is available including a C/C++ cross-compiler system based on GCC and the Newlib embedded C-library.

BCC includes a small run-time kernel with interrupt support and Pthreads library. For multi-threaded applications, a SPARC™ compliant port of the eCos real-time kernel, RTEMS 4.10, and VxWorks 6.x is supported.

1.0 Introduction

The UT700 LEON 3FT processor is based upon the industry-standard SPARC V8 architecture. The system-on-chip incorporates the SPARC V8 core and the peripheral blocks indicated below. The core and peripherals communicate internally via the AMBA (Advanced Microcontroller Bus Architecture) interconnect. This bus is comprised of the AHB (Advanced High-speed Bus) which is used for high-speed data transfer, and the APB (Advanced Peripheral Bus) which is used for low-speed data transfer.

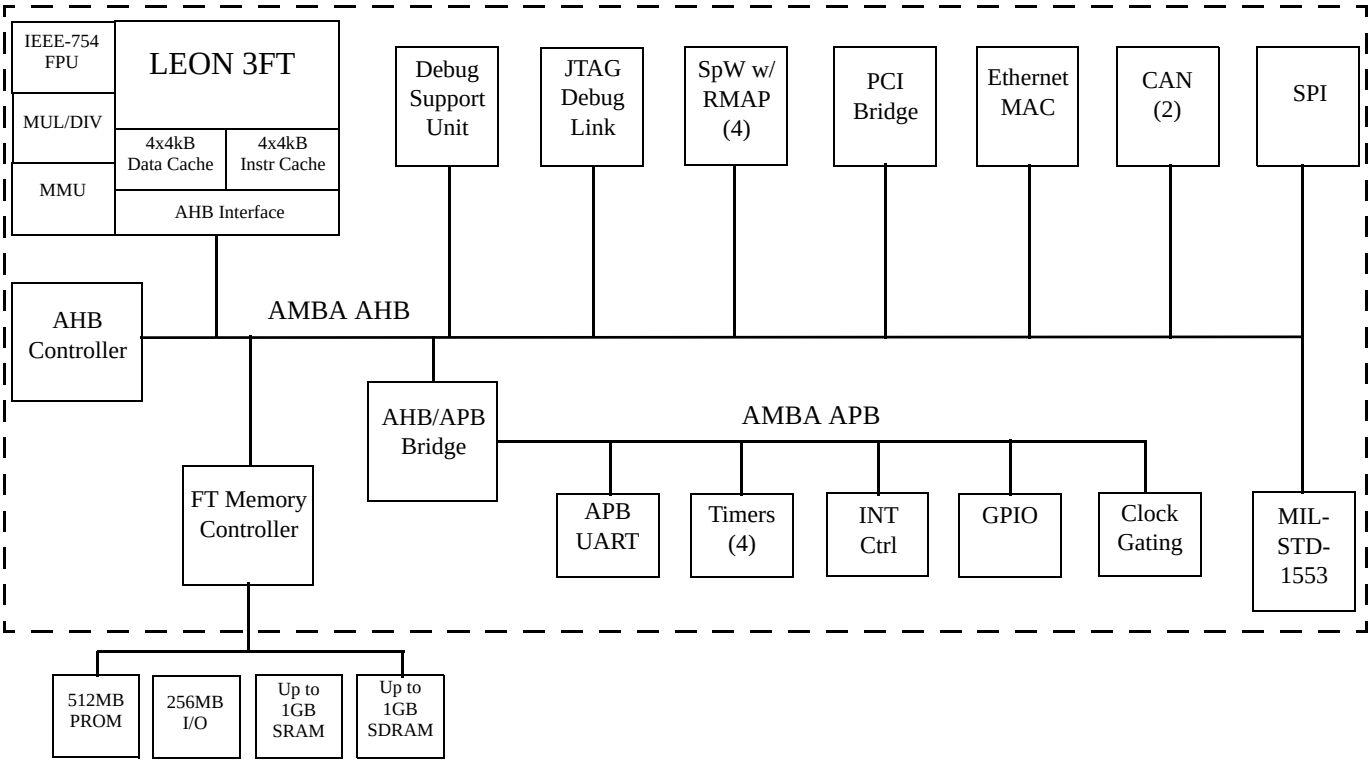


Figure 1. UT700 Functional Block Diagram

The LEON 3FT architecture includes the following peripheral blocks:

- LEON3 SPARC V8 integer unit with 16kB instruction cache and 16kB of data cache
- IEEE-754 floating point unit
- Debug support unit
- UART, JTAG, SpaceWire, PCI, and Ethernet debug links
- 8/16/32-bit memory controller with BCH EDAC for external PROM and SRAM
- 32-bit SDRAM controller with Reed Solomon EDAC for external SDRAM
- Timer unit with three 32-bit timers and watchdog
- Interrupt controller for 15 interrupts in two priority levels
- 16-bit general purpose I/O port (GPIO) which can be used as external interrupt sources
- Up to four SpaceWire links with RMAP on all channels
- MIL-STD-1553 interface supports BC/RT/MT
- Up to two CAN controllers
- Ethernet with support for MII
- cPCI interface with 8-channel arbiter

2.0 Pin Identification and Description

Pin Function	Description
I	CMOS input
IS	CMOS input Schmitt
O	CMOS output
I/O	CMOS bi-direct
OD	CMOS open drain
PCI-I	PCI input
PCI-O	PCI output
PCI-I/O	PCI bi-direct
PCI-3	PCI three-state

2.1. System Signals

Pin Name	Function	Pin Number	Reset Value	Description
		484 CLGA		
SYSCLK	I	Y20	--	Main system clock
NODIV	I	E19	--	Clock divider input. Set to '1' for 1x memory clock, '0' for 1/2x memory clock, relative to SYSCLK.
$\overline{\text{RESET}}$	IS	L19	--	System reset
$\overline{\text{ERROR}}$[1]	OD	K19	--	Processor error mode indicator. This is an active low output.
$\overline{\text{WDOG}}$[1]	OD	J19	--	Watchdog indicator. This is an active low output.

Notes:
1. This pin is actively driven low and must be tied to V_{DD} through a pull-up resistor.

2.2 Address Bus

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
ADDR[0]	O	W5	low	Bit 0 of the address bus
ADDR[1]	O	Y5	low	Bit 1 of the address bus
ADDR[2]	O	W6	low	Bit 2 of the address bus
ADDR[3]	O	AA5	low	Bit 3 of the address bus
ADDR[4]	O	Y6	low	Bit 4 of the address bus
ADDR[5]	O	AB5	low	Bit 5 of the address bus
ADDR[6]	O	W7	low	Bit 6 of the address bus

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
ADDR[7]	O	AA6	low	Bit 7 of the address bus
ADDR[8]	O	Y7	low	Bit 8 of the address bus
ADDR[9]	O	AA7	low	Bit 9 of the address bus
ADDR[10]	O	AB6	low	Bit 10 of the address bus
ADDR[11]	O	W8	low	Bit 11 of the address bus
ADDR[12]	O	AB7	low	Bit 12 of the address bus
ADDR[13]	O	Y8	low	Bit 13 of the address bus
ADDR[14]	O	AA8	low	Bit 14 of the address bus
ADDR[15]	O	W9	low	Bit 15 of the address bus
ADDR[16]	O	AB8	low	Bit 16 of the address bus
ADDR[17]	O	Y9	low	Bit 17 of the address bus
ADDR[18]	O	W10	low	Bit 18 of the address bus
ADDR[19]	O	AB9	low	Bit 19 of the address bus
ADDR[20]	O	Y10	low	Bit 20 of the address bus
ADDR[21]	O	AA9	low	Bit 21 of the address bus
ADDR[22]	O	W11	low	Bit 22 of the address bus
ADDR[23]	O	AA10	low	Bit 23 of the address bus
ADDR[24]	O	Y11	low	Bit 24 of the address bus
ADDR[25]	O	AB10	low	Bit 25 of the address bus
ADDR[26]	O	AB11	low	Bit 26 of the address bus
ADDR[27]	O	AA11	low	Bit 27 of the address bus

2.3 Data Bus

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
DATA[0]	I/O	W12	high-z	Bit 0 of the data bus
DATA[1]	I/O	W13	high-z	Bit 1 of the data bus
DATA[2]	I/O	Y12	high-z	Bit 2 of the data bus

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
DATA[3]	I/O	AA13	high-z	Bit 3 of the data bus
DATA[4]	I/O	AA12	high-z	Bit 4 of the data bus
DATA[5]	I/O	AB13	high-z	Bit 5 of the data bus
DATA[6]	I/O	W14	high-z	Bit 6 of the data bus
DATA[7]	I/O	AA14	high-z	Bit 7 of the data bus
DATA[8]	I/O	Y13	high-z	Bit 8 of the data bus
DATA[9]	I/O	W15	high-z	Bit 9 of the data bus
DATA[10]	I/O	AB15	high-z	Bit 10 of the data bus
DATA[11]	I/O	Y14	high-z	Bit 11 of the data bus
DATA[12]	I/O	AB14	high-z	Bit 12 of the data bus
DATA[13]	I/O	W16	high-z	Bit 13 of the data bus
DATA[14]	I/O	AA18	high-z	Bit 14 of the data bus
DATA[15]	I/O	Y15	high-z	Bit 15 of the data bus
DATA[16]	I/O	AB16	high-z	Bit 16 of the data bus
DATA[17]	I/O	AA15	high-z	Bit 17 of the data bus
DATA[18]	I/O	AB17	high-z	Bit 18 of the data bus
DATA[19]	I/O	AA16	high-z	Bit 19 of the data bus
DATA[20]	I/O	AA19	high-z	Bit 20 of the data bus
DATA[21]	I/O	W17	high-z	Bit 21 of the data bus
DATA[22]	I/O	AB18	high-z	Bit 22 of the data bus
DATA[23]	I/O	Y16	high-z	Bit 23 of the data bus
DATA[24]	I/O	Y17	high-z	Bit 24 of the data bus
DATA[25]	I/O	AA17	high-z	Bit 25 of the data bus
DATA[26]	I/O	W18	high-z	Bit 26 of the data bus
DATA[27]	I/O	AB19	high-z	Bit 27 of the data bus
DATA[28]	I/O	Y19	high-z	Bit 28 of the data bus
DATA[29]	I/O	AB20	high-z	Bit 29 of the data bus
DATA[30]	I/O	Y18	high-z	Bit 30 of the data bus
DATA[31]	I/O	AA20	high-z	Bit 31 of the data bus

2.4 Check Bits

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
CB[0]	I/O	V19	high-z	Bit 0 of EDAC BCH/RS checkbits
CB[1]	I/O	AA21	high-z	Bit 1 of EDAC BCH/RS checkbits
CB[2]	I/O	Y21	high-z	Bit 2 of EDAC BCH/RS checkbits
CB[3]	I/O	W19	high-z	Bit 3 of EDAC BCH/RS checkbits
CB[4]	I/O	Y22	high-z	Bit 4 of EDAC BCH/RS checkbits
CB[5]	I/O	W20	high-z	Bit 5 of EDAC BCH/RS checkbits
CB[6]	I/O	W22	high-z	Bit 6 of EDAC BCH/RS checkbits
CB[7]	I/O	W21	high-z	Bit 7 of EDAC BCH/RS checkbits
CB[8]	I/O	V18	high	Bit 8 of EDAC RS checkbits
CB[9]	I/O	U18	high	Bit 9 of EDAC RS checkbits
CB[10]	I/O	T18	high	Bit 10 of EDAC RS checkbits
CB[11]	I/O	R18	high	Bit 11 of EDAC RS checkbits
CB[12]	I/O	P18	high	Bit 12 of EDAC RS checkbits
CB[13]	I/O	N18	high	Bit 13 of EDAC RS checkbits
CB[14]	I/O	M18	high	Bit 14 of EDAC RS checkbits
CB[15]	I/O	M19	high	Bit 15 of EDAC RS checkbits

2.5 Memory Control Signals

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
$\overline{\text{WRITE}}$	O	V21	high	PROM and I/O write enable strobe
$\overline{\text{OE}}$	O	U19	high	PROM and I/O output enable
$\overline{\text{IOS}}$	O	T20	high	I/O area chip select
$\overline{\text{ROMS[0]}}$	O	V22	high	PROM chip select
$\overline{\text{ROMS[1]}}$	O	U20	high	PROM chip select
$\overline{\text{RWE[0]}}$	O	U22	high	SRAM write enable strobe
$\overline{\text{RWE[1]}}$	O	T19	high	SRAM write enable strobe

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
$\overline{\text{RWE[2]}}$	O	T22	high	SRAM write enable strobe
$\overline{\text{RWE[3]}}$	O	T21	high	SRAM write enable strobe
$\overline{\text{RAMOE[0]}}$	O	V20	high	SRAM output enable
$\overline{\text{RAMOE[1]}}$	O	R21	high	SRAM output enable
$\overline{\text{RAMOE[2]}}$	O	R20	high	SRAM output enable
$\overline{\text{RAMOE[3]}}$	O	R22	high	SRAM output enable
$\overline{\text{RAMOE[4]}}$	O	R19	high	SRAM output enable
$\overline{\text{RAMS[0]}}$	O	P22	high	SRAM chip select
$\overline{\text{RAMS[1]}}$	O	P20	high	SRAM chip select
$\overline{\text{RAMS[2]}}$	O	P21	high	SRAM chip select
$\overline{\text{RAMS[3]}}$	O	P19	high	SRAM chip select
$\overline{\text{RAMS[4]}}$	O	N19	high	SRAM chip select
READ	O	K20	high	SRAM, PROM, and I/O read indicator
$\overline{\text{BEXC}}$	I	K22	--	Bus exception
$\overline{\text{BRDY}}$	I	K21	--	Bus ready

2.6 SDRAM

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
SDCLK	O	AB12	high	SDRAM clock
$\overline{\text{SDRAS}}$	O	N22	high	SDRAM row address strobe
$\overline{\text{SDCAS}}$	O	N20	high	SDRAM column address strobe
$\overline{\text{SDWE}}$	O	N21	high	SDRAM write enable
$\overline{\text{SDCS[0]}}$	O	M21	high	SDRAM chip select
$\overline{\text{SDCS[1]}}$	O	M22	high	SDRAM chip select
SDDQM[0]	O	L21	high	SDRAM data mask
SDDQM[1]	O	M20	high	SDRAM data mask
SDDQM[2]	O	L20	high	SDRAM data mask

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
SDDQM[3]	O	L22	high	SDRAM data mask

2.7 CAN 2.0 Interface

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
CAN_RXD[0]	I	J20	--	CAN receive data
CAN_TXD[0]	O	J22	high	CAN transmit data
CAN_RXD[1]	I	J21	--	CAN receive data
CAN_TXD[1]	O	H22	high	CAN transmit data

2.8 Debug Support Unit (DSU)

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
DSUACT	O	H19	low	DSUmode indicator
DSUBRE	I	H20	--	DSU break
DSUEN	I	G19	--	DSU enable
DSURX	I	G20	--	DSU UART receive data
DSUTX	O	G21	high	DSU UART transmit data

2.9 JTAG Interface

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
$\overline{\text{TRST}}$	I	F20	--	JTAG reset
$\overline{\text{TMS}}$	I	F21	--	JTAG test mode select
TCK	I	G22	--	JTAG clock
TDI	I	F22	--	JTAG test data input

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
TDO	O	F19	undef	JTAG test data output

2.10 Ethernet Interface

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
EMDC	O	E22	low	Ethernet media interface clock
ERX_CLK	I	D22	--	Ethernet RX clock
EMDIO	I/O	D20	high-z	Ethernet media interface data
ERX_COL	I	E21	--	Ethernet collision error
ERX_CRS	I	E20	--	Ethernet carrier sense detect
ERX_DV	I	D21	--	Ethernet receiver data valid
ERX_ER	I	C21	--	Ethernet reception error
ERXD[0]	I	C22	--	Ethernet receive data
ERXD[1]	I	B21	--	Ethernet receive data
ERXD[2]	I	C20	--	Ethernet receive data
ERXD[3]	I	B20	--	Ethernet receive data
ETXD[0]	O	C19	low	Ethernet transmit data
ETXD[1]	O	C18	high	Ethernet transmit data
ETXD[2]	O	B18	low	Ethernet transmit data
ETXD[3]	O	B19	high	Ethernet transmit data
ETX_CLK	I	A19	--	Ethernet TX clock
ETX_EN	O	A18	low	Ethernet transmit enable
ETX_ER	O	A20	low	Ethernet transmit error. Always driven low.
EDCLDIS	I	E17	--	Ethernet EDCL disable
$\overline{\text{EMDINT}}$	I	E18	--	Ethernet management interface data interrupt

2.11 General Purpose I/O

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
GPIO[0]	I/O	B17	high-z	Bit 0 of general purpose I/O
GPIO[1]	I/O	C17	high-z	Bit 1 of general purpose I/O
GPIO[2]	I/O	A17	high-z	Bit 2 of general purpose I/O
GPIO[3]	I/O	D17	high-z	Bit 3 of general purpose I/O
GPIO[4]	I/O	C16	high-z	Bit 4 of general purpose I/O
GPIO[5]	I/O	D16	high-z	Bit 5 of general purpose I/O
GPIO[6]	I/O	C15	high-z	Bit 6 of general purpose I/O
GPIO[7]	I/O	D15	high-z	Bit 7 of general purpose I/O
GPIO[8]	I/O	C7	high-z	Bit 8 of general purpose I/O
GPIO[9]	I/O	B5	high-z	Bit 9 of general purpose I/O
GPIO[10]	I/O	D7	high-z	Bit 10 of general purpose I/O
GPIO[11]	I/O	A5	high-z	Bit 11 of general purpose I/O
GPIO[12]	I/O	D6	high-z	Bit 12 of general purpose I/O
GPIO[13]	I/O	C5	high-z	Bit 13 of general purpose I/O
GPIO[14]	I/O	C6	high-z	Bit 14 of general purpose I/O
GPIO[15]	I/O	D5	high-z	Bit 15 of general purpose I/O

2.12 SpaceWire Interface

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
SPW_CLK	I	A11	--	SpaceWire clock
SPW_RXS[0]	I	A16	--	SpaceWire receive strobe
SPW_RXD[0]	I	A15	--	SpaceWire receive data
SPW_TXS[0]	O	B16	low	SpaceWire transmit strobe
SPW_TXD[0]	O	B15	low	SpaceWire transmit data
SPW_RXS[1]	I	A14	--	SpaceWire receive strobe
SPW_RXD[1]	I	A13	--	SpaceWire receive data

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
SPW_TXS[1]	O	B14	low	SpaceWire transmit strobe
SPW_TXD[1]	O	B13	low	SpaceWire transmit data
SPW_RXS[2]	I	A9	--	SpaceWire receive strobe
SPW_RXD[2]	I	A8	--	SpaceWire receive data
SPW_TXS[2]	O	B9	low	SpaceWire transmit strobe
SPW_TXD[2]	O	B8	low	SpaceWire transmit data
SPW_RXS[3]	I	A7	--	SpaceWire receive strobe
SPW_RXD[3]	I	A6	--	SpaceWire receive data
SPW_TXS[3]	O	B7	low	SpaceWire transmit strobe
SPW_TXD[3]	O	B6	low	SpaceWire transmit data

2.13 UART Interface

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
RXD	I	C12	--	UART receive data
TXD	O	C11	high	UART transmit data

2.14 PCI Address and Data Bus

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
PCI_AD[0]	PCI-I/O	AA2	high-z	Bit 0 of PCI address and data bus
PCI_AD[1]	PCI-I/O	AA3	high-z	Bit 1 of PCI address and data bus
PCI_AD[2]	PCI-I/O	Y1	high-z	Bit 2 of PCI address and data bus
PCI_AD[3]	PCI-I/O	Y2	high-z	Bit 3 of PCI address and data bus
PCI_AD[4]	PCI-I/O	Y3	high-z	Bit 4 of PCI address and data bus
PCI_AD[5]	PCI-I/O	W1	high-z	Bit 5 of PCI address and data bus
PCI_AD[6]	PCI-I/O	W2	high-z	Bit 6 of PCI address and data bus

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
PCI_AD[7]	PCI-I/O	W3	high-z	Bit 7 of PCI address and data bus
PCI_AD[8]	PCI-I/O	V2	high-z	Bit 8 of PCI address and data bus
PCI_AD[9]	PCI-I/O	V3	high-z	Bit 9 of PCI address and data bus
PCI_AD[10]	PCI-I/O	U1	high-z	Bit 10 of PCI address and data bus
PCI_AD[11]	PCI-I/O	U2	high-z	Bit 11 of PCI address and data bus
PCI_AD[12]	PCI-I/O	U3	high-z	Bit 12 of PCI address and data bus
PCI_AD[13]	PCI-I/O	T1	high-z	Bit 13 of PCI address and data bus
PCI_AD[14]	PCI-I/O	R2	high-z	Bit 14 of PCI address and data bus
PCI_AD[15]	PCI-I/O	R1	high-z	Bit 15 of PCI address and data bus
PCI_AD[16]	PCI-I/O	J1	high-z	Bit 16 of PCI address and data bus
PCI_AD[17]	PCI-I/O	K2	high-z	Bit 17 of PCI address and data bus
PCI_AD[18]	PCI-I/O	K1	high-z	Bit 18 of PCI address and data bus
PCI_AD[19]	PCI-I/O	G1	high-z	Bit 19 of PCI address and data bus
PCI_AD[20]	PCI-I/O	H3	high-z	Bit 20 of PCI address and data bus
PCI_AD[21]	PCI-I/O	H2	high-z	Bit 21 of PCI address and data bus
PCI_AD[22]	PCI-I/O	F1	high-z	Bit 22 of PCI address and data bus
PCI_AD[23]	PCI-I/O	F2	high-z	Bit 23 of PCI address and data bus
PCI_AD[24]	PCI-I/O	E1	high-z	Bit 24 of PCI address and data bus
PCI_AD[25]	PCI-I/O	E2	high-z	Bit 25 of PCI address and data bus
PCI_AD[26]	PCI-I/O	F3	high-z	Bit 26 of PCI address and data bus
PCI_AD[27]	PCI-I/O	D1	high-z	Bit 27 of PCI address and data bus
PCI_AD[28]	PCI-I/O	D2	high-z	Bit 28 of PCI address and data bus
PCI_AD[29]	PCI-I/O	E3	high-z	Bit 29 of PCI address and data bus
PCI_AD[30]	PCI-I/O	D3	high-z	Bit 30 of PCI address and data bus
PCI_AD[31]	PCI-I/O	C1	high-z	Bit 31 of PCI address and data bus

2.15 PCI Control Signals

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
$\overline{\text{PCI\_RST}}$	PCI-I	C3	--	PCI reset input
PCI_CLK	PCI-I	C2	--	PCI clock input
PCI_C/$\overline{\text{BE}}$[0]	PCI-I/O	V1	high-z	PCI bus command and byte enable
PCI_C/$\overline{\text{BE}}$[1]	PCI-I/O	P2	high-z	PCI bus command and byte enable
PCI_C/$\overline{\text{BE}}$[2]	PCI-I/O	H1	high-z	PCI bus command and byte enable
PCI_C/$\overline{\text{BE}}$[3]	PCI-I/O	G2	high-z	PCI bus command and byte enable
PCI_PAR	PCI-I/O	P1	high-z	PCI parity checkbit
$\overline{\text{PCI\_FRAME}}$[1]	PCI-3	L1	high-z	PCI cycle frame indicator
$\overline{\text{PCI\_IRDY}}$[1]	PCI-3	L2	high-z	PCI initiator ready indicator
$\overline{\text{PCI\_TRDY}}$[1]	PCI-3	M1	high-z	PCI target ready indicator
$\overline{\text{PCI\_STOP}}$[1]	PCI-3	N1	high-z	PCI target stop request
$\overline{\text{PCI\_DEVSEL}}$[1]	PCI-3	M2	high-z	PCI device select
$\overline{\text{PCI\_PERR}}$[1]	PCI-3	N2	high-z	PCI parity error indicator
PCI_IDSEL	PCI-I	G3	--	PCI initialization device select
$\overline{\text{PCI\_REQ}}$	PCI-O	A4	high-z	PCI request to arbiter in point to point configuration
$\overline{\text{PCI\_GNT}}$	PCI-I	B2	--	PCI bus access indicator in point to point configuration
$\overline{\text{PCI\_HOST}}$	PCI-I	AB3	--	PCI host enable input (Connect to $\overline{\text{SYSEN}}$ in PCI bus)

Notes:
1. This pin must be tied to V_{DD} through a pull-up resistor as specified in the PCI Local Bus Specification Revision 2.1 Section 4.3.3.

2.16 PCI Arbiter

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
$\overline{\text{PCI\_ARB\_REQ[0]}}$	PCI-I	B4	--	PCI arbiter bus request
$\overline{\text{PCI\_ARB\_REQ[1]}}$	PCI-I	AB4	--	PCI arbiter bus request

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
$\overline{\text{PCI\_ARB\_REQ[2]}}$	PCI-I	Y4	--	PCI arbiter bus request
$\overline{\text{PCI\_ARB\_REQ[3]}}$	PCI-I	T3	--	PCI arbiter bus request
$\overline{\text{PCI\_ARB\_REQ[4]}}$	PCI-I	P3	--	PCI arbiter bus request
$\overline{\text{PCI\_ARB\_REQ[5]}}$	PCI-I	M3	--	PCI arbiter bus request
$\overline{\text{PCI\_ARB\_REQ[6]}}$	PCI-I	K3	--	PCI arbiter bus request
$\overline{\text{PCI\_ARB\_REQ[7]}}$	PCI-I	C4	--	PCI arbiter bus request
$\overline{\text{PCI\_ARB\_GNT[0]}}$	PCI-O	B3	high-z	PCI arbiter bus grant
$\overline{\text{PCI\_ARB\_GNT[1]}}$	PCI-O	AA4	high-z	PCI arbiter bus grant
$\overline{\text{PCI\_ARB\_GNT[2]}}$	PCI-O	W4	high-z	PCI arbiter bus grant
$\overline{\text{PCI\_ARB\_GNT[3]}}$	PCI-O	R3	high-z	PCI arbiter bus grant
$\overline{\text{PCI\_ARB\_GNT[4]}}$	PCI-O	N3	high-z	PCI arbiter bus grant
$\overline{\text{PCI\_ARB\_GNT[5]}}$	PCI-O	L3	high-z	PCI arbiter bus grant
$\overline{\text{PCI\_ARB\_GNT[6]}}$	PCI-O	J3	high-z	PCI arbiter bus grant
$\overline{\text{PCI\_ARB\_GNT[7]}}$	PCI-O	A3	high-z	PCI arbiter bus grant

2.17 Serial Peripheral Interface (SPI)

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
SPICLK	O	E12		SPI Clock
SPIMOSI	O	E13		SPI Master Out Slave In
SPIMISO	I	E11	--	SPI Master In Slave Out
SPISLVSEL	O	E10		SPI Select

2.18 MIL-STD-1553 Signals

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
1553CLK	I	B11	--	MIL-STD-1553B Clock

Pin Name	Direction	Pin Number	Reset Value	Description
		484 CLGA		
1553RXA	I	C13	--	MIL-STD-1553B Receive Positive A
$\overline{1553RXA}$	I	D12	--	MIL-STD-1553B Receive Negative A
1553RXB	I	C8	--	MIL-STD-1553B Receive Positive B
$\overline{1553RXB}$	I	C9	--	MIL-STD-1553B Receive Negative B
1553RXENA	O	D11	high-z	MIL-STD-1553B Receive Enable A
1553RXENB	O	D9	high-z	MIL-STD-1553B Receive Enable B
1553TXINHA	O	D13	high-z	MIL-STD-1553B Transmit Inhibit A
1553TXINHB	O	D10	high-z	MIL-STD-1553B Transmit Inhibit B
1553TXA	O	D14	high-z	MIL-STD-1553B Transmit Positive A
$\overline{1553TXA}$	O	C14	high-z	MIL-STD-1553B Transmit Negative A
1553TXB	O	B10	high-z	MIL-STD-1553B Transmit Positive B
$\overline{1553TXB}$	O	C10	high-z	MIL-STD-1553B Transmit Negative B

2.19 Power and Ground Pins

Pin Name	Pin Number	Description
	484 CLGA	
V_{DD}	B1, B12, B22, E7, E9, E14, E16, F6, F10, F13, F17, G5, G9, G14, H6, H8, H10, H13, H15, J7, J16, K5, K8, K15, K17, L6, M6, N5, N8, N15, N17, P7, P16, R6, R8, R10, R13, R15, T5, T9, T14, U6, U9, U11, U12, U14, U17, V10, V13, AA1, AA22	I/O supply voltage
V_{SS}	A1, A12, A22, E6, F4, G4, G8, G11, G12, G15, G17, H4, H7, H16, H18, J2, J4, J9, J14, K4, K10, K13, L7, L11, L12, L17, M7, M11, M12, M17, N4, N10, N13, P4, P9, P14, R4, R7, R16, T2, T4, T8, T15, T17, U4, U10, U13, V4, V5, V8, V11, V12, V15, AB1, AB22	I/O supply ground
V_{DDC}	A2, A21, E5, F8, F15, G7, G10, G13, G16, G18, H5, H9, H11, H12, H14, H17, J6, J8, J15, K7, K16, L8, L15, L18, M4, M8, M15, N7, N16, P6, P8, P15, R5, R9, R11, R12, R14, R17, T7, T10, T13, T16, U8, U15, V6, V17, AB2, AB21	Core supply voltage
V_{SSC}	A10, E8, E15, F5, F7, F9, F11, F12, F14, F16, F18, G6, H21, J5, J10, J11, J12, J13, J17, K6, K9, K11, K12, K14, K18, L5, L9, L10, L13, L14, L16, M5, M9, M10, M13, M14, M16, N6, N9, N11, N12, N14, P5, P10, P11, P12, P13, P17, T6, T11, T12, U5, U7, U16, U21, V7, V14, V16	Core supply ground

Pin Name	Pin Number	Description
	484 CLGA	
N/C	D4, D18, E4, J18, L4, V9	No connect. These pins may be left floating, or tied to V_{DD} or V_{SS}
Unused	D8	This pin may be left floating or tied to V_{SS}
Unused	D19	This pin must be tied to V_{SS}

2.20 Bootstrap Signals

The states of the following signals are latched in upon the rising edge of reset in order to configure the UT700 for the indicated operation.

Pin Name	Function
GPIO[1:0]	Sets the data width of the PROM area 00: 8 bits 01: 16 bits 10: 32 bits 11: Not used
GPIO[2]	Enable EDAC checking of the PROM area 0: EDAC disabled 1: EDAC enabled
GPIO[7:4]	Set the SpW clock divisor link bits in the SpW Clock Divisor Register
GPIO[15:12]	Sets the least significant address nibble of the IP and MAC address for the Ethernet Debug Communication Link (EDCL)

3.0 AC and DC Electrical Specifications

3.1 Absolute Maximum Ratings[1]

Symbol	Description		Min	Max	Units
V_{DDC}	Core supply voltage		-0.3	1.85	V
V_{DD}	I/O supply voltage		-0.3	5.2	V
V_{IN}	Input voltage any pin		V_{SS} - 0.3	V_{DD} + 0.3	V
P_D[2]	Maximum power dissipation permitted @ $T_C = 105^oC$		--	4	W
T_J	Junction temperature		--	150	^oC
Θ_{JC}	Thermal resistance, junction to case	484 CLGA/CCGA/CBGA	--	5	$^oC/W$
T_{STG}	Storage temperature		-65	150	^oC
ESD_{HBM}	ESD protection (human body model) Class 2		2000	--	V

Notes:
1. Stresses greater than those listed in the following table can result in permanent damage to the device. These parameters cannot be violated.
2. Per MIL-STD-883, Method 1012, Section 3.4.1, PD = $(T_J(max)-T_c(max))/\Theta_{JC}$

3.2 Recommended Operating Conditions

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Min	Max	Units
V_{DDC}	Core supply voltage	1.1	1.3	V
V_{DD}	I/O supply voltage	3.0	3.6	V
V_{IN}	Input voltage any pin	0	V_{DD}	V
T_C	Case operating temperature	-55	105	^oC
t_R	Rise time, all CMOS and PCI inputs ($0.1V_{DD}$ to $0.9V_{DD}$)	--	20	ns
t_F	Fall time, all CMOS and PCI inputs ($0.9V_{DD}$ to $0.1V_{DD}$)	--	20	ns

3.3 Operational Environment

The UT700 processor includes the following SEU mitigation features:
* Cache memory error-detecting of up to 4 errors per tag or 32-bit word
* Autonomous and software transparent error handling
* No timing impact due to error detection or correction

PARAMETER	LIMIT	UNITS
Total Ionizing Dose (TID) [1]	1E5	rad (Si)
Single Event Latchup Immune (SEL) [2]	≤110	MeV-cm^2/mg
Single Event Upset (SEU) [3, 4] Inherent register upset rate	5.2E-7	errors/device-day
Single Event Upset (SEU) [3, 4] Multiple-bit error (MBE) rate which over-comes internal error detection & correction architecture	2.8E-11	MBE/device-day

Notes:

1. TID irradation per MIL-STD-883, Test Method 1019, condition A. Post irradiation electrical testing performed at room temperature.
2. Worst case temperature of T_C = +105^{o}C, V_{DD} = 3.6V, V_{DD} = 1.3V.
3. Contact factory for additional information regarding the determination of the inherent and multiple-bit upset rates.
4. The error rate calculation was performed using SpaceRad 6.0 for a Geosynchronous orbit in the Adams 90% worst-case environment with 100mil Al shielding.

3.4 Power Supply Operating Characteristics (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions			Min	Max	Units
I_{DDCS}	Standby core power supply quiescent current	V_{DDC} = 1.3V, V_{DD}= 3.6V All clock inputs at 0MHz		T_C = -55°C and 25°C	--	8	mA
				T_C = 105°C	--	100	
			RHA: R	T_C = 25°C	--	50	
I_{DDS}	Standby I/O power supply quiescent current	V_{DDC} = 1.3V, V_{DD} = 3.6V All clock inputs at 0MHz		T_C = -55°C and 25°C	--	0.7	mA
				T_C = 105°C	--	2	

3.5 DC Characteristics for LVCMOS3 Inputs (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
V_{IH}[1]	High-level input voltage		$0.7V_{DD}$	--	V
V_{IL}[1]	Low-level input voltage		--	$0.3V_{DD}$	V
V_{T+}	Positive going threshold voltage for Schmitt inputs		--	$0.7V_{DD}$	V
V_{T-}	Negative going threshold voltage for Schmitt inputs		$0.3V_{DD}$	--	V
V_H	Hysteresis voltage for Schmitt inputs		0.4	--	V
I_{IN}	Input leakage current (All inputs except pull-ups and pull-downs)	$V_{IN} = V_{DD}$	--	1	µA
		$V_{IN} = V_{SS}$	-1	--	
I_{IN}	Input leakage current for pins with internal pull-up resistors (CB[15:8], $\overline{\text{EMDINT}}$, and NODIV)	$V_{IN} = V_{DD}$	-10	10	µA
		$V_{IN} = V_{SS}$	-100	-10	
I_{IN}	Input leakage current for pins with internal pull-down resistors (EDCLDIS, SPIMISO, 1553CLK, 1553RXA, $\overline{\text{1553RXA}}$, 1553RXB, and $\overline{\text{1553RXB}}$)	$V_{IN} = V_{DD}$	+10	+150	µA
		$V_{IN} = V_{SS}$	-10	10	
C_{IN}[2]	Input pin capacitance	f = 1MHz; V_{DD} = 0V, V_{DDC} = 0V	--	16	pF

Notes:
1. JTAG inputs are not tested.
2. Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance.

3.6 DC Characteristics for LVCMOS3 Outputs (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
V_{OL1}[1]	Low-level output voltage (All outputs except those listed below and in Section 3.8)	I_{OL} = 100µA	--	0.25	V
		I_{OL} = 4mA	--	0.4	
V_{OH1}[1,2]	High-level output voltage (All outputs except those listed below and in Section 3.8)	I_{OH} = -100µA	V_{DD}-0.25	--	V
		I_{OH} = -4mA	2.4	--	
V_{OL2}	Low-level output voltage (GPIO[15:0], SPW_TXD[3:0], SPW_TXS[3:0], TXD)	I_{OL} = 100µA	--	0.25	V
		I_{OL} = 12mA	--	0.4	
V_{OH2}	High-level output voltage (GPIO[15:0], SPW_TXD[3:0], SPW_TXS[3:0], TXD)	I_{OH} = -100µA	V_{DD}-0.25	--	V
		I_{OH} = -12mA	2.4	--	
V_{OL3}	Low-level output voltage ($\overline{WRITE}$, $\overline{OE}$, $\overline{IOS}$, $\overline{ROMS[1:0]}$, $\overline{RWE\ [3:0]}$, $\overline{RAMOE\ [4:0]}$, $\overline{RAMS[4:0]}$, $\overline{SDCS[1:0]}$, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCLK, READ, SDDQM[3:0], ADDR[27:0], DATA[31:0] and CB[15:0])	I_{OL} = 100µA	--	0.25	V
		I_{OL} = 24mA	--	0.4	
V_{OH3}	High-level output voltage ($\overline{WRITE}$, $\overline{OE}$, $\overline{IOS}$, $\overline{ROMS[1:0]}$, $\overline{RWE\ [3:0]}$, $\overline{RAMOE\ [4:0]}$, $\overline{RAMS[4:0]}$, $\overline{SDCS[1:0]}$, $\overline{SDRAS}$, $\overline{SDCAS}$, $\overline{SDWE}$, SDCLK, READ, SDDQM[3:0], ADDR[27:0], DATA[31:0] and CB[15:0])	I_{OH} = -100µA	V_{DD}-0.25	--	V
		I_{OH} = -24mA	2.4	--	
V_{OL4}	Low-level output voltage (SPICLK, SPIMOSI, SPISLVSEL)	I_{OL} = 100µA	--	0.25	V
		I_{OL} = 8mA	--	0.4	
V_{OH4}	High-level output voltage (SPICLK, SPIMOSI, SPISLVSEL)	I_{OH} = -100µA	V_{DD}-0.25	--	V
		I_{OH} = -8mA	2.4	--	
I_{OZ}	Three-state output current	$V_O = V_{DD}$	-10	10	µA
		$V_O = V_{SS}$	-10	10	
I_{OS}[3]	Short-circuit output current (All outputs except PCI outputs)	$V_O = V_{DD}$; V_{DD} = 3.6V	--	130	mA
		$V_O = V_{SS}$; V_{DD} = 3.6V	-65	--	
C_{OUT}[4]	Output pin capacitance	f = 1MHz; V_{DD} = 0V, V_{DDC} = 0V	--	16	pF

Notes:
1. JTAG outputs are not tested.
2. Except open-drain output.
3. Guaranteed by design.
4. Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance.

3.7 AC Electrical Characteristics for LVCMOS3 Inputs and Outputs (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
f_{CLK}	System clock frequency		--	166	MHz
t_{HIGH}	System clock high time		2.4	--	ns
t_{LOW}	System clock low time		2.4	--	ns
t_{DSD}[1]	System clock to SDRAM clock propagation delay		2.0	6.0	ns

Notes:
1. Reference Figure 17 for test load.

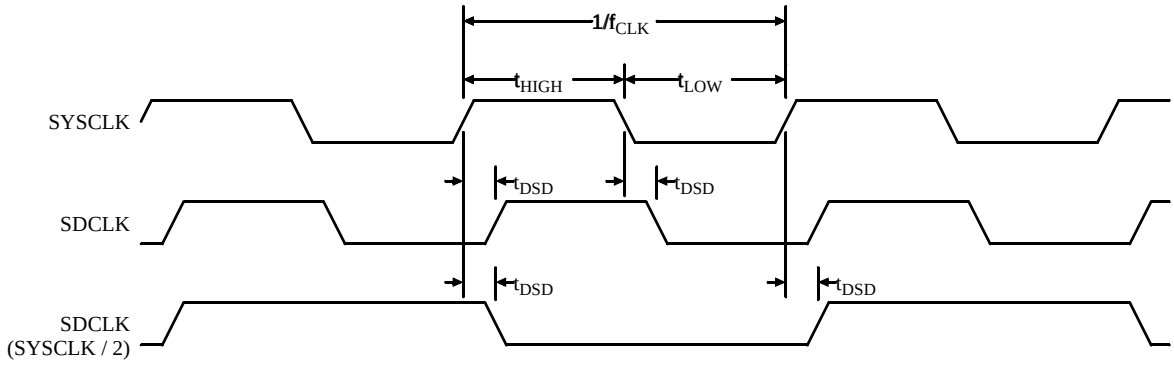


Figure 2. System Clock and SDCLK Timing Diagram

3.8 DC Electrical Characteristics for PCI Inputs (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
V_{IH}	High-level input voltage		$0.5V_{DD}$	--	V
V_{IL}	Low-level input voltage		--	$0.3V_{DD}$	V
I_{IN}	Input leakage current	$V_{IN} = V_{DD}$	--	+10	µA
		$V_{IN} = V_{SS}$	-10	--	
C_{IN}[1]	Input pin capacitance	f = 1MHz; V_{DD} = 0V, V_{DDC} = 0V	--	22	pF

Notes:
1. Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance.

3.9 DC Electrical Characteristics for PCI Outputs (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
V_{OH}	High-level output voltage (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], $\overline{PCI\_RST}$, PCI_IDSEL, $\overline{PCI\_FRAME}$, $\overline{PCI\_IRDY}$, $\overline{PCI\_TRDY}$, $\overline{PCI\_DEVSEL}$, $\overline{PCI\_STOP}$, $\overline{PCI\_PERR}$, PCI_PAR)	I_{OH} = -500µA	$0.9V_{DD}$	--	V
V_{OL}	Low-level output voltage (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], $\overline{PCI\_RST}$, PCI_IDSEL, $\overline{PCI\_FRAME}$, $\overline{PCI\_IRDY}$, $\overline{PCI\_TRDY}$, $\overline{PCI\_DEVSEL}$, $\overline{PCI\_STOP}$, $\overline{PCI\_PERR}$, PCI_PAR)	I_{OL} = 1500µA	--	$0.1V_{DD}$	V
I_{OZ}	Three-state output current	$V_O = V_{DD}$	-10	+10	µA
		$V_O = V_{SS}$	-10	+10	
I_{OS}[1]	Short-circuit output current	$V_O = V_{DD}$; V_{DD} = 3.6V	--	270	mA
		$V_O = V_{SS}$; V_{DD} = 3.6V	-130	--	
C_{OUT}[2]	Output pin capacitance	f = 1MHz; V_{DD} = 0V, V_{DDC} = 0V	--	22	pF

Notes:
1. Guaranteed by design.
2. Capacitance is measured for initial qualification and when design changes might affect the input/output capacitance.

3.10 AC Electrical Characteristics for PCI Inputs (pre- and post-radiation)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
f_{PCI_CLK}	PCI clock frequency		--	33	MHz
t_{HIGH}	PCI clock high time		11	--	ns
t_{LOW}	PCI clock low time		11	--	ns

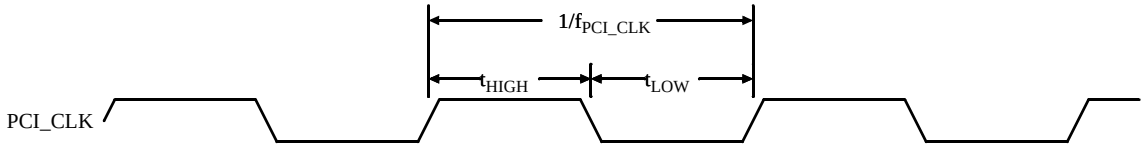


Figure 3. PCI Clock Timing Diagram

4.0 Timing Specifications

4.1 Power Sequencing and Reset

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
t_{VCD}[1]	V_{DD} valid to V_{DDC} delay	$V_{DD} \geq$ 3.0V; $V_{DDC} \geq$ 1.1V	0	--	ns
t_{VHBZ}[1]	V_{DD} valid to control signals high-z ($\overline{WRITE}$, $\overline{OE}$, $\overline{IOS}$, $\overline{ROMS[1:0]}$, $\overline{RWE[3:0]}$, $\overline{RAMOE\ [4:0]}$, READ $\overline{SDWE}$, and $\overline{SDCS[1:0]}$) V_{DD} valid to outputs high-z ([DATA[31:0], CB[15:0], and GPIO[15:0])	$V_{DD} \geq$ 1.5V; V_{DDC} = 0V	--	4	t_{CLK}
t_{CHBV}[1]	V_{DDC} valid to control signals valid-inactive ($\overline{WRITE}$, $\overline{OE}$, $\overline{IOS}$, $\overline{ROMS[1:0]}$, $\overline{RWE[3:0]}$, $\overline{RAMOE\ [4:0]}$, READ $\overline{SDWE}$, and $\overline{SDCS[1:0]}$)	$V_{DD} \geq$ 3.0V; $V_{DDC} \geq$ 1.1V	--	4	t_{CLK}
t_{RESET1}[1]	V_{DDC} valid to $\overline{RESET}$ deassert	$V_{DDC} \geq$ 1.1V	4	--	t_{CLK}
t_{RESET2}[1]	$\overline{RESET}$ deasserted to outputs valid-active ($\overline{ROMS[0]}$ and $\overline{OE}$)		--	12	t_{CLK}
t_{RESET3}[1]	$\overline{RESET}$ asserted to control signals valid-inactive ($\overline{WRITE}$, $\overline{OE}$, $\overline{IOS}$, $\overline{ROMS[1:0]}$, $\overline{RWE[3:0]}$, $\overline{RAMOE\ [4:0]}$, READ $\overline{SDWE}$, and $\overline{SDCS[1:0]}$) $\overline{RESET}$ asserted to outputs high-z (DATA[31:0], CB[15:0], and GPIO[15:0])		--	4	t_{CLK}

Notes:
1. Guaranteed by design.

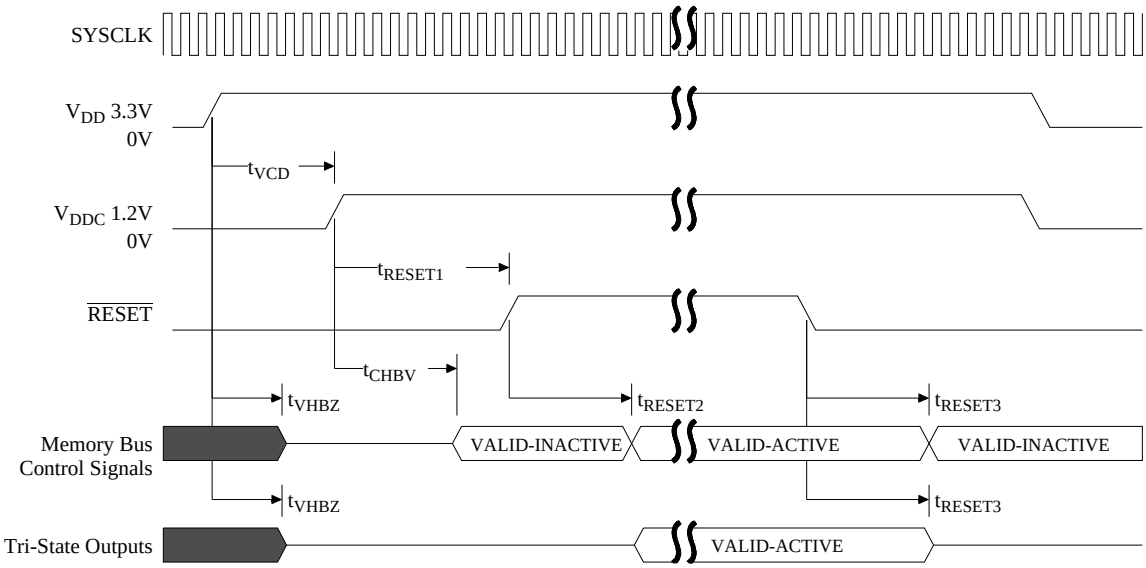


Figure 4. Power Sequencing and Reset Timing Diagram

4.1.1. Power Sequencing

For optimal power sequencing, both power-up and power-down, ramp both V_{DD} and V_{DDC} together. During power-up, if $V_{DDC} > V_{DD} + 0.3V$, excessive current or damage may occur to the device. During power down, it is acceptable for V_{DD} to be less than V_{DDC} by more than 0.3V as long as V_{DDC} is not actively driven.

4.1.2 Bus Control and Bi-Direct Fail-Safe Circuitry

In order to prevent bus contention on the external memory interface while V_{DDC} is ramping up, the UT700 has functionality to ensure that the bi-direct and memory bus control signals described in Section 4.1 will be in a high-z state t_{VHBZ} delay after V_{DD} reaches 1.5V. The core logic will put these signals into their valid-inactive states t_{CHBV} clock cycles after V_{DDC} reaches 1.1V.

Aeroflex recommends that users place pull-up resistors on the indicated output enable, write enable, and chip select pins, and a pull-down resistor on the READ pin, if t_{VCD} is greater than 100ns. This will prevent bus capacitance or transients from inadvertently placing these pins in an active state, which could result in external memory devices driving the address and data buses.

4.1.3 Reset Circuitry

The reset circuitry is controlled by the core logic; therefore, the circuitry is functional only after V_{DDC} reaches its minimum operating voltage of 1.1V. After V_{DDC} is stable, the system must continue to assert $\overline{RESET}$ for a minimum of t_{RESET1} clock cycles before it can be de-asserted. Asserting $\overline{RESET}$ for less time could result in the $\overline{RESET}$ signal not being recognized.

The UT700 will begin fetching code from external memory no more than t_{RESET2} clock cycles after $\overline{RESET}$ is de-asserted. Control signals $\overline{ROMS[0]}$ and $\overline{OE}$ will be driven to their valid-active states in order for the UT700 to begin fetching code from PROM. During normal operation, the indicated bus control signals will go to a valid-inactive state, and the bi-directs will go to a high-z state, within t_{RESET3} clock cycles after the assertion of $\overline{RESET}$.

Boot Strap Programming on GPIO

Data on pins GPIO[2:0], GAPIO[7:4] and GPIO[15:12] are latched on the rising edge of reset. The states of GPIO[2:0] determine the data width of the PROM area, and enable EDAC for the PROM area. Chapter 3 of the User's Manual describes the value of these inputs to achieve the required operation. The states of GPIO[7:4] provides a means to configure the SpaceWire clock divisor link bits in the Clock Divisor Register. The states of GPIO[15:12] set the least significant address nibble of the IP and MAC address for the Ethernet Debug Communication Link (EDCL).

In order for the state of GPIO pins to be properly latched, Aeroflex recommends placing pull-up or pull-down resistors on these pins to ensure that the setup and hold timing is met. The states of these pins should be statically set prior to the rising edge of $\overline{\text{RESET}}$.

4.2 Output Timing Characteristics for Memory Interface, $\overline{\text{ERROR}}$, and $\overline{\text{WDOG}}$

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Min	Max	Units
t1a[1]	SDCLK↑ to ADDR[27:0] valid	1.5	8.5	ns
t1b[1]	SDCLK↑ to $\overline{\text{SDCS[1:0]}}$ valid	2	7.5	ns
t1c[1]	SDCLK↑ to output valid $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, and $\overline{\text{SDWE}}$	1.5	8.5	ns
t1d[1]	SDCLK↑ to SDDQM[3:0] valid	2.5	8.5	ns
t1e[1]	SDCLK↑ to output valid ($\overline{\text{WRITE}}$, $\overline{\text{OE}}$, $\overline{\text{IOS}}$, $\overline{\text{ROMS[1:0]}}$, $\overline{\text{RWE [3:0]}}$, $\overline{\text{RAMOE [4:0]}}$, $\overline{\text{RAMS[4:0]}}$, and READ)	1	8	ns
t2[1,2]	SDCLK↑ to output valid (DATA[31:0] and CB[15:0])	2.5	8.5	ns
t3[1,2,3]	SDCLK↑ to output high-Z (DATA[31:0] and CB[15:0])	2.5	8.5	ns
t4[1]	SDCLK↑ to signal low ($\overline{\text{ERROR}}$ and $\overline{\text{WDOG}}$[4])	--	10	ns
t8[1,2,3]	$\overline{\text{WRITE}}$↑ or $\overline{\text{RWE[3:0]}}$↑ to output high-z (DATA [31:0] and CB[15:0])	0.5	--	ns
t9[1]	Skew from first memory output signal transition to last memory output signal transition	--	2	ns

Notes:

1. All outputs are measured using the load conditions shown in Figure 17.
2. CB[7] is not tested in the case of BCH EDAC.
3. High-Z defined as +/-300mV change from steady state.
4. Guaranteed by design.

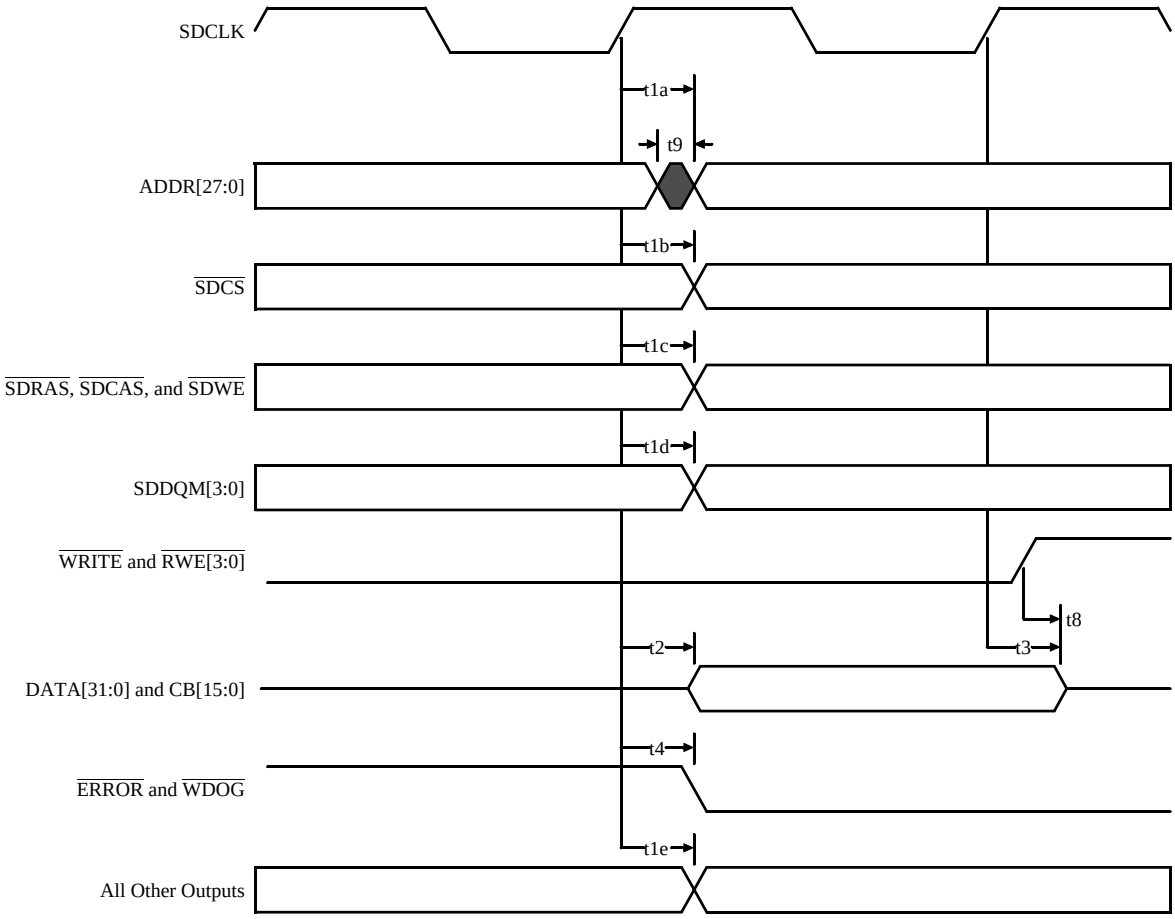


Figure 5. Memory Interface, $\overline{\text{ERROR}}$, and $\overline{\text{WDOG}}$ Output Timing Diagram

4.3 Input Timing Characteristics for Memory Interface

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Min	Max	Units
t5a[1]	Setup time to SDCLK↑ (DATA[31:0] and CB[15:0])	1	--	ns
t5b	Setup time to SDCLK↑ ($\overline{BEXC}$, and synchronous $\overline{BRDY}$)	2	--	ns
t6a[1]	Hold time from SDCLK↑ (DATA[31:0] and CB[15:0])	1.5	--	ns
t6b	Hold time from SDCLK↑ (Synchronous $\overline{BRDY}$)	0	--	ns
t7[2]	Asynchronous $\overline{BRDY}$ pulse width	1.5	--	t_{CLK}

Notes:
1. CB[7] is not tested in the case of BCH EDAC.
2. Supplied as a design limit. Neither guaranteed nor tested.

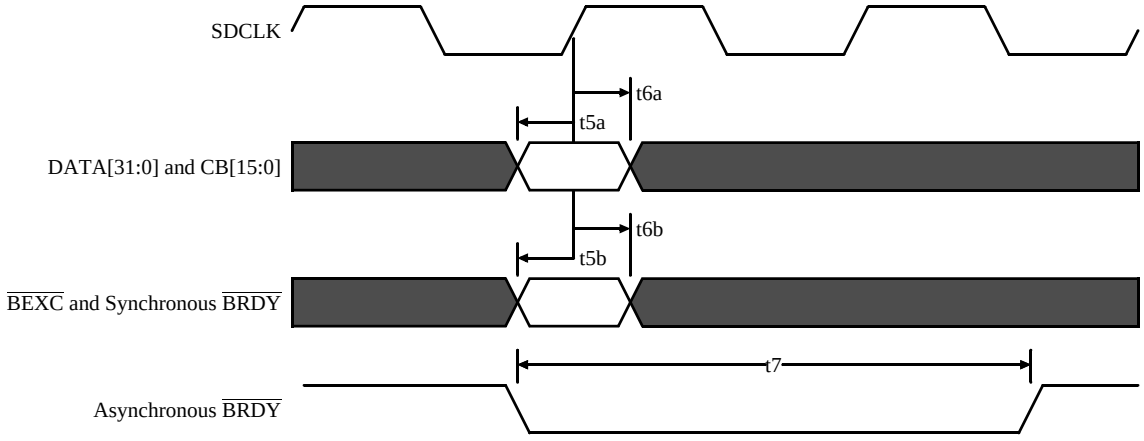


Figure 6. Memory Interface Input Timing Diagram

4.4 Timing Characteristics for General Purpose Input / Output (GPIO)

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Min	Max	Units
t10[1]	SDCLK↑ to GPIO output valid (GPIO[15:0])	--	10	ns

Notes:
1. All outputs are measured using the load conditions shown in Figure 17.

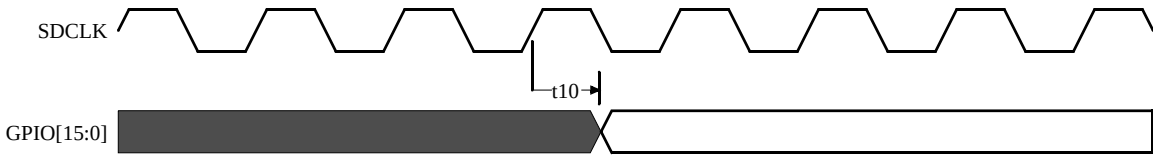


Figure 7. General Purpose I/O Timing Diagram

4.5 Timing Characteristics SpaceWire Interface

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Min	Max	Units
t11 [1,2]	SPW_CLK period	5	--	ns
t14 [3,4,5]	Transmit data and strobe bit width variation (SPW_TXD[3:0] and SPW_TXS[3:0])	UI-600	UI+600	ps
t15 [5,6]	Receive data and strobe bit width (SPW_RXD[3:0] and SPW_RXS[3:0])	5	--	ns
t16 [5]	Receive data and strobe edge separation (SPW_RXD[3:0] and SPW_RXS[3:0])	1/2*t11 + 0.5	--	ns

Notes:

1. The SPW_CLK frequency must be less than or equal to 10x the SYSCLK frequency. For example, if SPW_CLK is running at 200MHz, the SYSCLK frequency must be greater than or equal to 20MHz.
2. Functionally tested.
3. Applies to both high pulse and low pulse.
4. A unit interval (UI) is defined as the nominal, or ideal, bit width.
5. Guaranteed by design.
6. The SPW_CLK period must be less than or equal to the minimum receive data/strobe bit width.

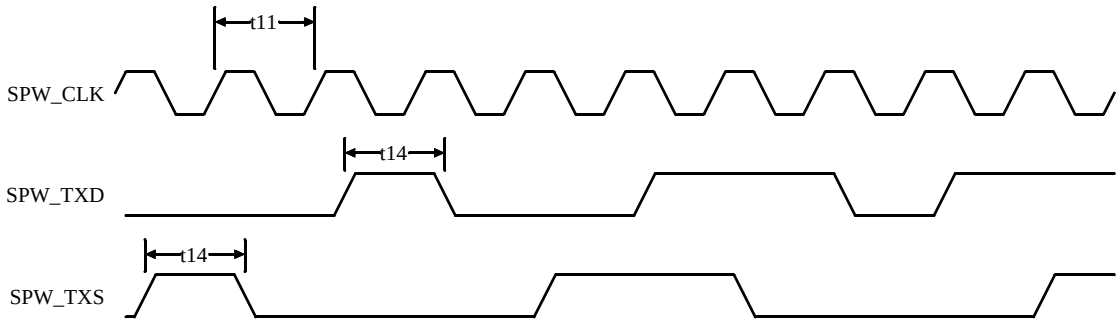


Figure 8. SpaceWire Transmit Timing Diagram

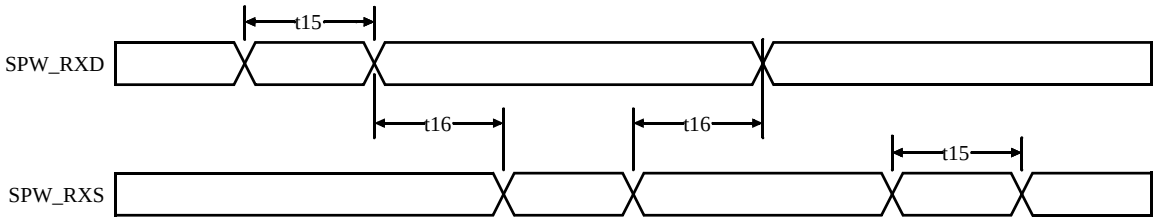


Figure 9. SpaceWire Receive Timing Diagram

4.6 Timing Characteristics for PCI Interface

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Min	Max	Units
t17[1]	PCI_CLK↑ to output valid (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], PCI_PAR, $\overline{PCI\_FRAME}$, $\overline{PCI\_IRDY}$, $\overline{PCI\_TDRY}$, $\overline{PCI\_STOP}$, $\overline{PCI\_DEVSEL}$, $\overline{PCI\_PERR}$, $\overline{PCI\_REQ}$, and $\overline{PCI\_ARB\_GNT}$[7:0])	2	13	ns
t18[1,2]	PCI_CLK↑ to output valid from high-z (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], PCI_PAR, $\overline{PCI\_FRAME}$, $\overline{PCI\_IRDY}$, $\overline{PCI\_TDRY}$, $\overline{PCI\_STOP}$, $\overline{PCI\_DEVSEL}$, and $\overline{PCI\_PERR}$	2	13	ns
t19[1,2]	PCI_CLK↑ to output high-Z (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], PCI_PAR, $\overline{PCI\_FRAME}$, $\overline{PCI\_IRDY}$, $\overline{PCI\_TDRY}$, $\overline{PCI\_STOP}$, $\overline{PCI\_DEVSEL}$, and $\overline{PCI\_PERR}$	--	14	ns
t20[3,4]	Setup time to PCI_CLK↑ (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], PCI_PAR, $\overline{PCI\_FRAME}$, $\overline{PCI\_IRDY}$, $\overline{PCI\_TDRY}$, $\overline{PCI\_STOP}$, $\overline{PCI\_DEVSEL}$, $\overline{PCI\_PERR}$, PCI_IDSEL, $\overline{PCI\_GNT}$, and $\overline{PCI\_AR-B\_REQ}$[7:0])	4	--	ns
t21[3,4]	Hold time from PCI_CLK↑ (PCI_AD[31:0], PCI_C/$\overline{BE}$[3:0], PCI_PAR, $\overline{PCI\_FRAME}$, $\overline{PCI\_IRDY}$, $\overline{PCI\_TDRY}$, $\overline{PCI\_STOP}$, $\overline{PCI\_DEVSEL}$, $\overline{PCI\_PERR}$, PCI_IDSEL, $\overline{PCI\_GNT}$, and $\overline{PCI\_AR-B\_REQ}$[7:0])	1	--	ns
t22[5]	PCI_CLK↑ to $\overline{RESET}$ deassertion	10	--	PCI Clocks
t23a[5]	PCI_CLK↑ to $\overline{PCI\_RST}$ deassertion	10	--	PCI Clocks
t23b[5]	$\overline{PCI\_RST}$ assertion to PCI_CLK idle	10		PCI Clocks
t24	$\overline{PCI\_RST}$ active to output high-Z	--	40	ns

Notes:

1. All outputs are measured using the load conditions shown in Figure 17.
2. High-Z defined as +/-300mV change from steady state.
3. $\overline{PCI\_TRDY}$, $\overline{PCI\_STOP}$, and $\overline{PCI\_DEVSEL}$ timing is guaranteed by design when used as inputs.
4. $\overline{PCI\_PERR}$ and $\overline{PCI\_GNT}$ are guaranteed by design.
5. Guaranteed by design.

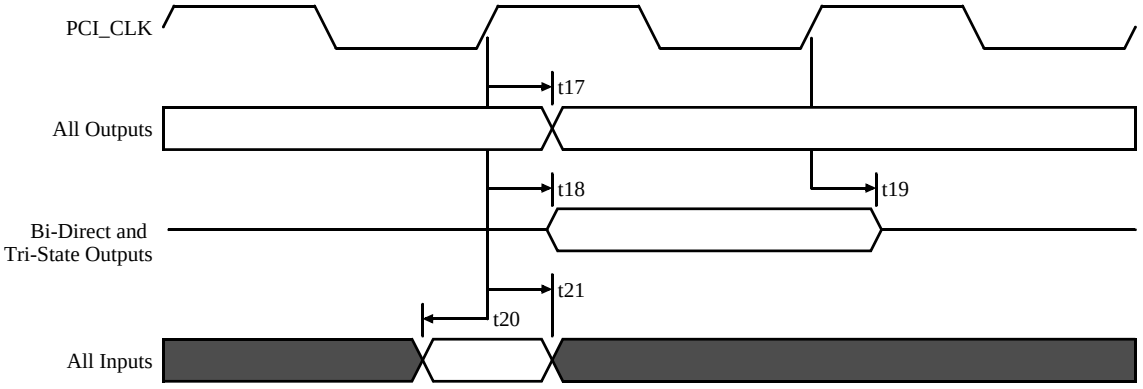


Figure 10. PCI Timing Diagram

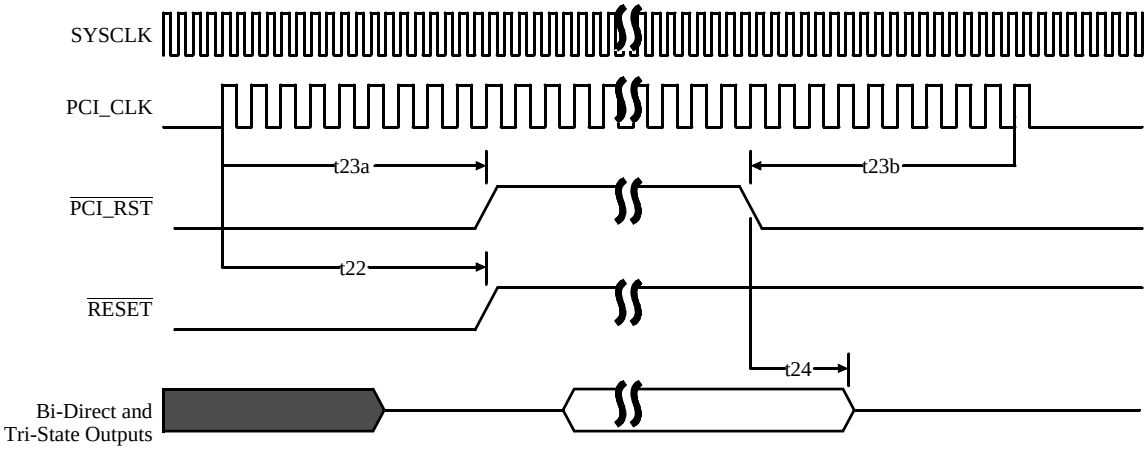


Figure 11. Timing Relationships of Clock and Reset for PCI Core Utilization

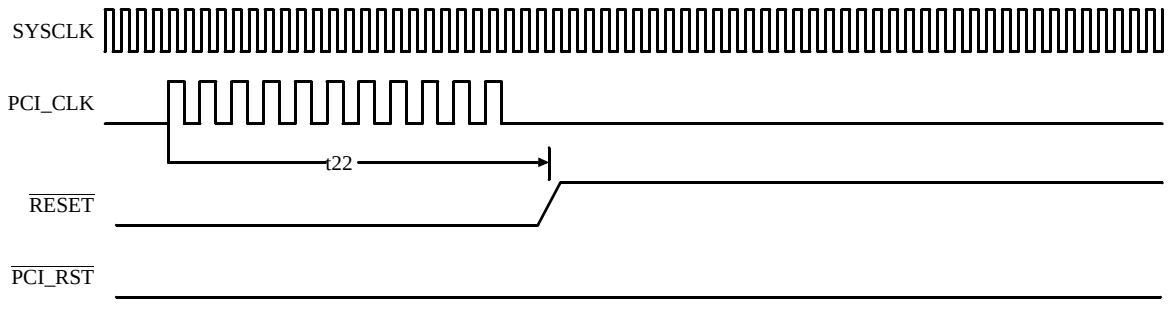


Figure 12. Timing Relationships of Clock and Reset for Unused PCI Core

4.7 Timing Characteristics for Ethernet Interface

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
t25[1]	ETX_CLK↑ to output valid (ETXD[3:0], and ETX_EN)		--	12	ns
t26[2,3]	Setup time to ERX_CLK↑ (ERX_DV, ERX_ER, and ERXD[3:0])		1	--	ns
t27[2,3]	Hold time from ERX_CLK↑ (ERX_DV, ERX_ER, and ERXD[3:0])		1	--	ns
t28[1]	EMDC↑ to output valid (EMDIO)		$-4+t_{AMBA}$[4]	$4+t_{AMBA}$[4]	ns
t29[5]	Setup time to EMDC↑ (EMDIO)		10	--	ns
t30[5]	Hold time from EMDC↑ (EMDIO)		10	--	ns

Notes:
1. All outputs are measured using the load conditions shown in Figure 17.
2. ERX_ER timing is guaranteed by design.
3. ERX_COL and ERX_CRS are asynchronous inputs and are not tested.
4. t_{AMBA} is defined as t_{SYSCLK} for NODIV = 1 and t_{SYSCLK} * 2 for NODIV = 0.
5. Guaranteed by design.

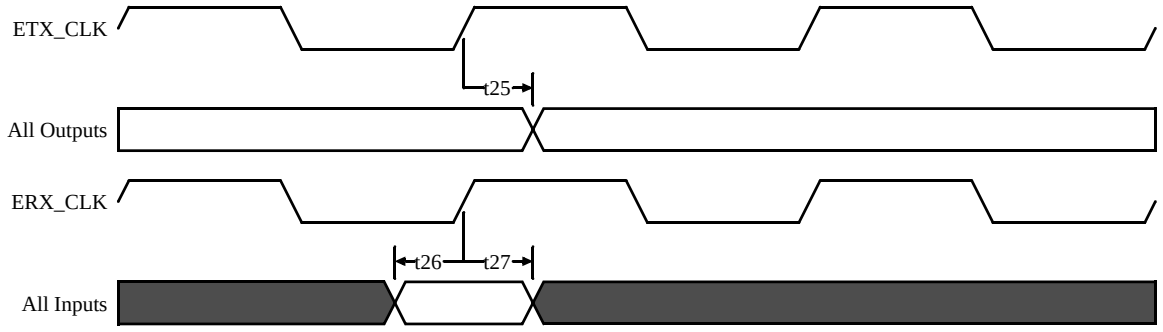


Figure 13. Ethernet Transmit and Receive Timing

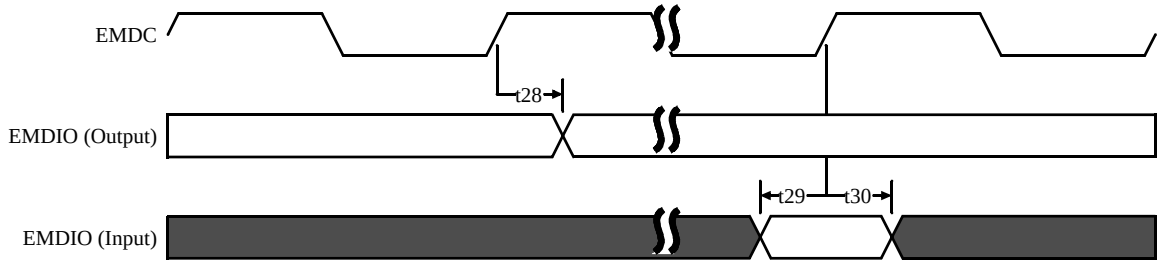


Figure 14. Ethernet MDIO Interface Timing

4.7 Timing Characteristics for MIL-STD-1553 Interface[2]

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
t31[1]	1553CLK↑ to output valid (1553RXENA, 1553RXENB, 1553TX-INHA, 1553TXINHB, 1553TXA, $\overline{1553TXA}$, 1553TXB, and $\overline{1553TXB}$)		--	20	ns

Notes:
1. All outputs are measured using the load conditions shown in Figure 17.
2. The 1553RXA, $\overline{1553RXA}$, 1553RXB and $\overline{1553RXB}$ inputs are resynchronized internally.

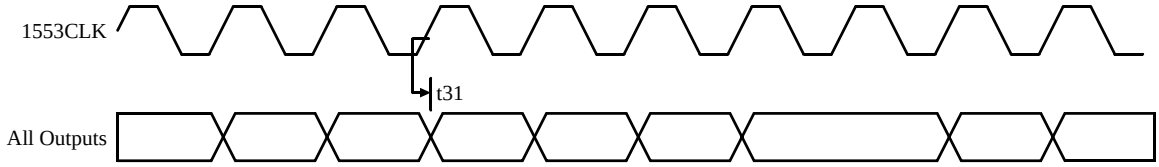


Figure 15. MIL-STD-1553 Interface Timing

4.7 Timing Characteristics for SPI[2]

(V_{DD} = 3.3V ± 0.3V; V_{DDC} = 1.2V ± 0.1V; T_C = -55°C to 105°C)

Symbol	Description	Conditions	Min	Max	Units
t32[1]	SPICLK↑ to output valid (SPIMOSI)		-2	2	ns

Notes:
1. All outputs are measured using the load conditions shown in Figure 17.
2. The SPIMISO input is resynchronized internally.

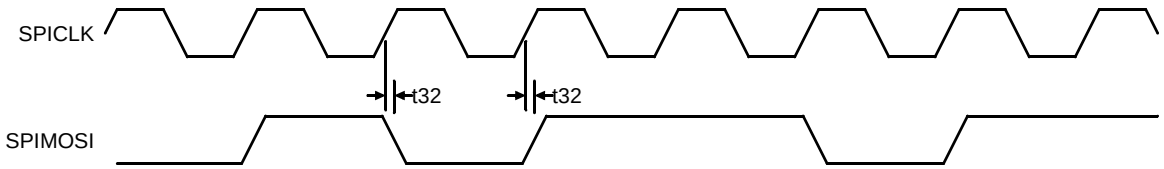


Figure 16. Serial Peripheral Interface (SPI) Timing

4.8 Test Conditions for Timing Specifications

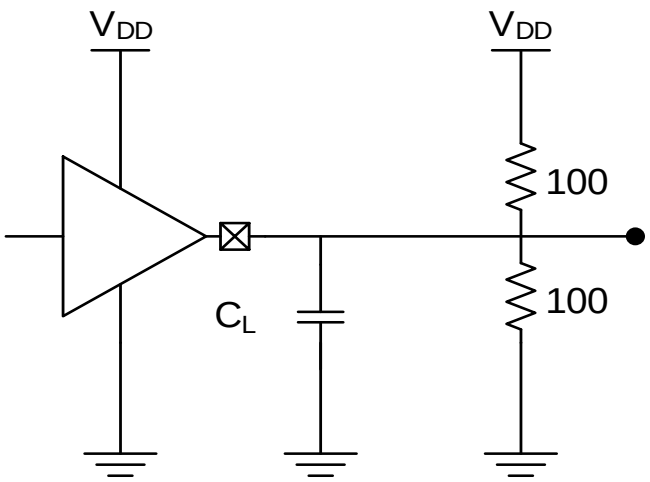


Figure 17. Equivalent Load Circuit for Timing Characteristics Tests
C_L = 50 pF for ATE test load
C_L =15 pF for benchtop test load

5.0 Packaging

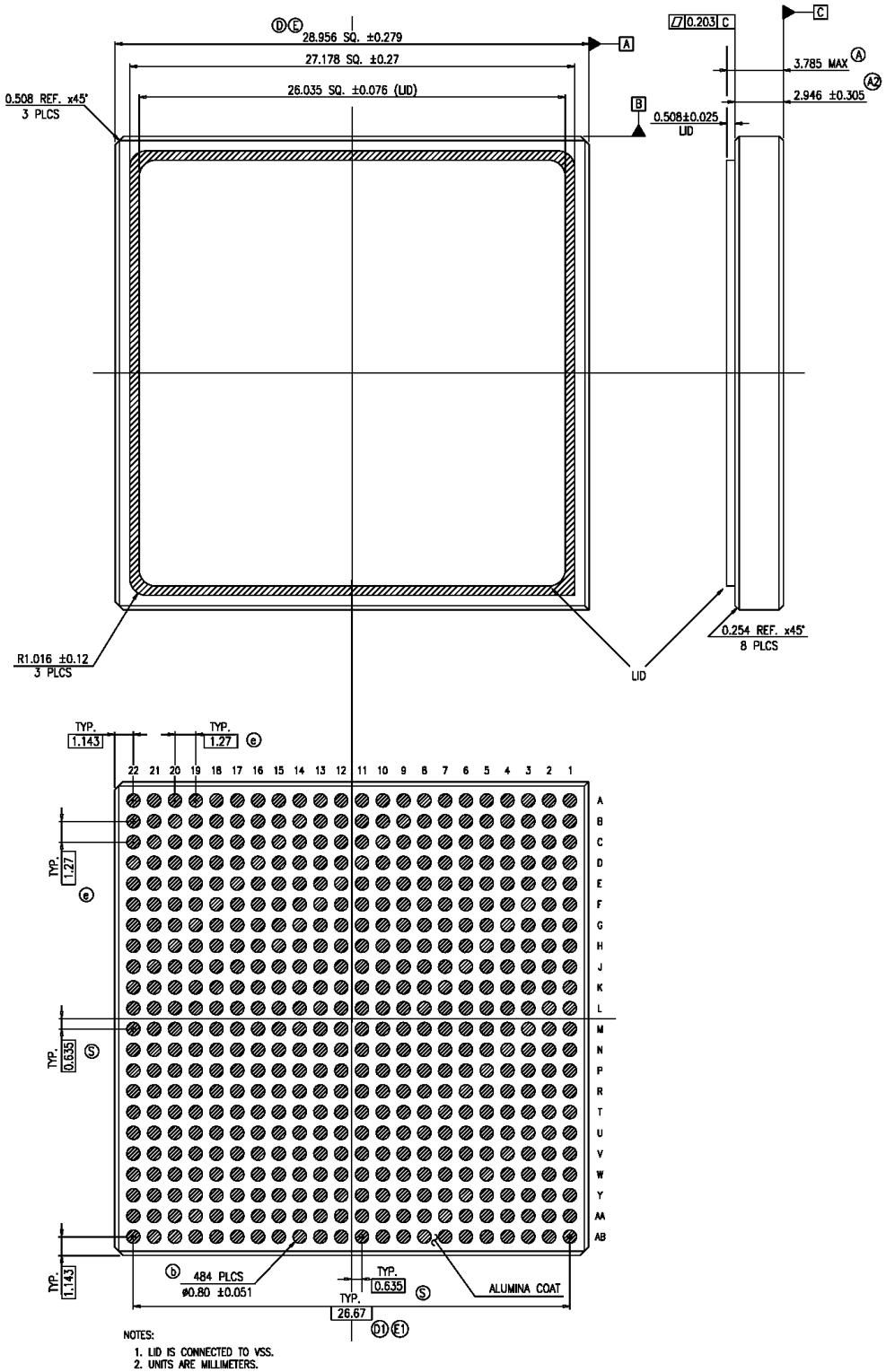


Figure 18. 484-lead Ceramic Land Grid Array

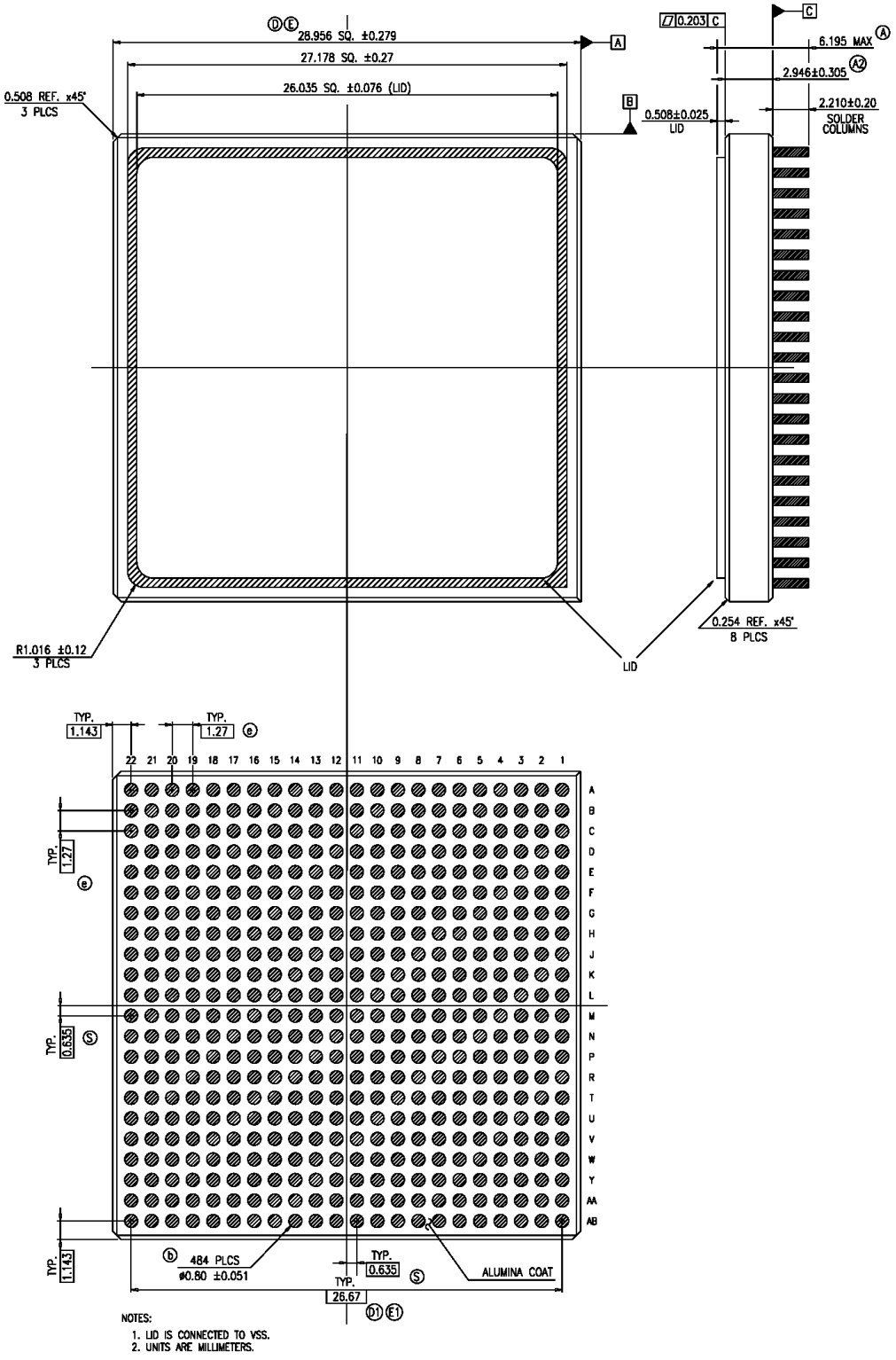


Figure 19. 484-lead Ceramic Column Grid Array

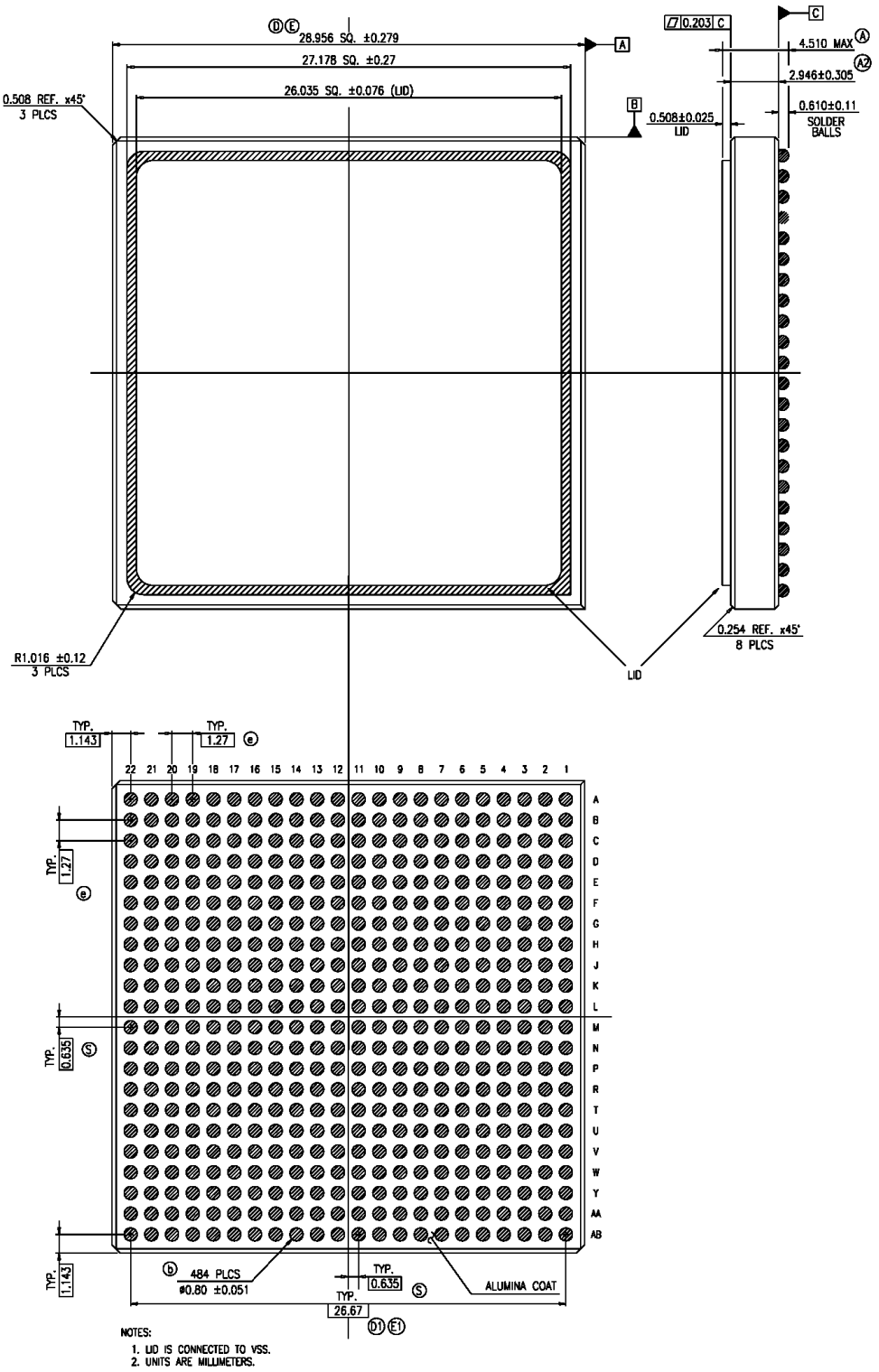
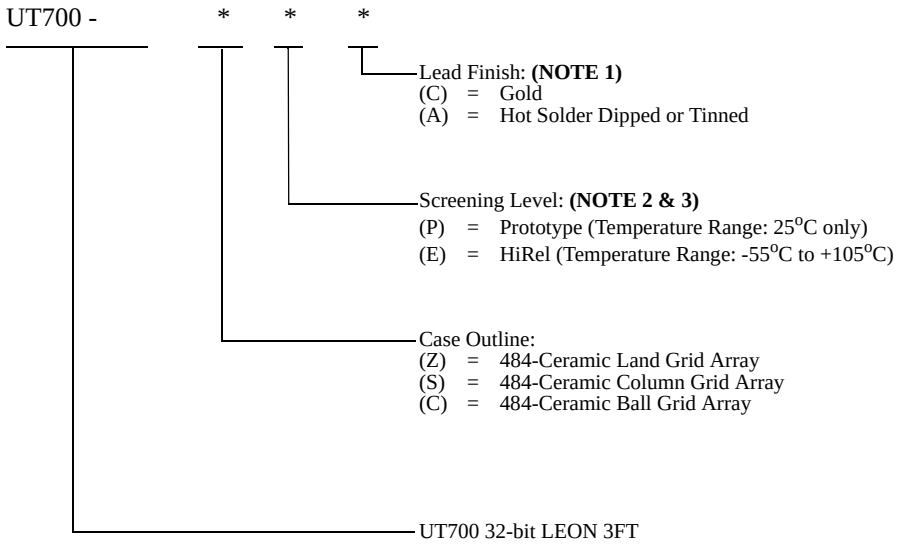


Figure 20. 484-lead Ceramic Ball Grid Array

7.0 Ordering Information

UT700 LEON 3FT

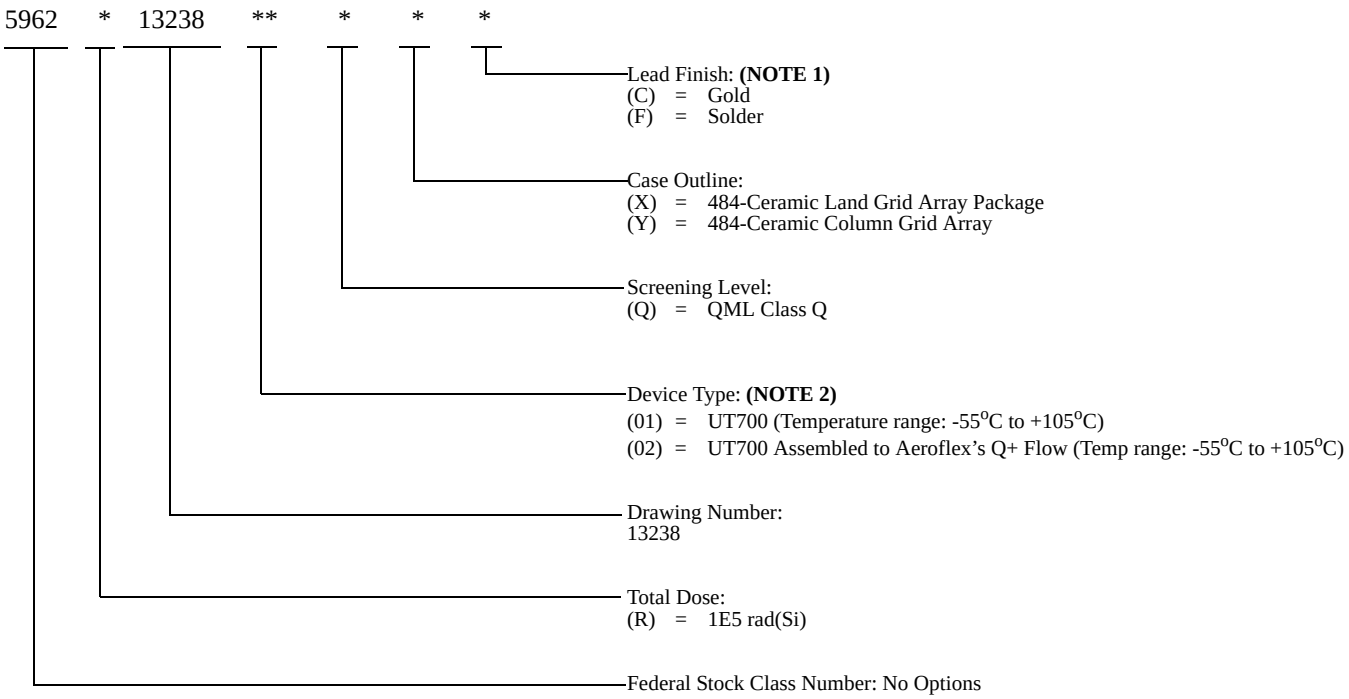


Notes:

1. Lead finish (A or C) must be specified.
2. Prototype Flow per Aeroflex Manufacturing Flows Document. Devices are tested at 25°C only. Radiation is neither tested nor guaranteed.
3. HiRel Flow per Aeroflex Manufacturing Flows Document. Radiation is neither tested nor guaranteed.

Package Option	Associated Lead Finish
(Z) 484-CLGA	(C) Gold
(S) 484-CCGA	(A) Hot Solder Dipped
(C) 484-CBGA	(A) Hot Solder Dipped

UT700 LEON 3FT: SMD



Notes:
1. Lead finish is "C" (gold) only.
2.Aeroflex's Q+ assembly flow, as defined in section 4.2.2.d of the SMD, provides QML-Q product through the SMD that is manufactured with Aeroflex's standard QML-V flow, and has completed QML-V qualification per MIL-PRF-38535.

Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

This product is controlled for export under the Export Administration Regulations (EAR). A license from the U.S. Government is required prior to the export of this product from the United States.

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DATA SHEET REVISION HISTORY

Revision & Date	Description of Change
11/19/13 Ver. 1.0.0	**Release of Preliminary Data Sheet**
8/26/14 Ver. 1.1.0	**Release Production Datasheet** **Page 1: Corrected SEL Immune** **Page 17: Corrected VDDC, VDD limits, and note 3 temperature** **Page 18: Moved Operational Environment table from section 5 to 3.3 and updated** **Page 19: Added IDDCS, IDDS limits from TBD** **Page 20: Added IIN and IIN limits (to bound the range for pull up/down resistors)** **Page 22: Corrected tDSD limits** **Page 23: Corrected IIN and IOZ limits** **Page 32: Corrected symbols t14, t15, t16, and the corresponding timing diagrams** **Page 39: Moved the Operational Environment table to section 3.3 on page 18** **Pages 40-42: Corrected package drawings**
11/21/14 1.2.0	**Page 2: Changed Figure 1 Data and Instr Cache Values from 2x4kB to 4x4kB** **Page 16: Added GPIO[2] entry to Bootstrap signals table.** **Page 28:Re-wrote section 4.1.4** **Page 43:Corrected SMD lead finish designator.** **Page All: Added Footer**
March 2015 Ver. 1.3.1	**Page 17: Removed note 3 and changed the maximum junction temperature value from 125°C to 150°C in the Absolute Maximum Ratings Table.** **Page 26: Rewrote section 4.1.1 on power sequencing.**