

## Dual bidirectional I<sup>2</sup>C-bus and SMBus voltage-level translator

### Features

- 2-bit bidirectional translator for SDA and SCL lines in mixed-mode I<sup>2</sup>C-bus applications
- Standard-mode, Fast-mode, and Fast-mode Plus I<sup>2</sup>C-bus and SMBus compatible
- Less than 1.5 ns maximum propagation delay to accommodate Standard mode and Fast mode I<sup>2</sup>C-bus devices and multiple masters
- Allows voltage level translation between:
  - 0.9V VREF1 and 1.8 V, 2.5 V, 3.3 V or 5 V VREF2
  - 1.2 V VREF1 and 1.8 V, 2.5 V, 3.3 V or 5 V VREF2
  - 1.5 V VREF1 and 2.5 V, 3.3 V or 5 V VREF2
  - 1.8 V VREF1 and 3.3 V or 5 V VREF2
  - 2.5 V VREF1 and 5 V VREF2
  - 3.3 V VREF1 and 5 V VREF2
- Provides bidirectional voltage translation with no direction pin
- Low 3.5 ohm ON-state connection between input and output ports provides less signal distortion
- Open-drain I<sup>2</sup>C-bus I/O ports (SCL1, SDA1, SCL2 and SDA2)
- 5 V tolerant I<sup>2</sup>C-bus I/O ports to support mixed-mode signal operation
- High-impedance SCL1, SDA1, SCL2 and SDA2 pins for EN = LOW
- Lock-up free operation for isolation when EN = LOW
- Flow through pin out for ease of printed-circuit board trace routing
- ESD protection exceeds 4KV HBM per JESD22-A114
- Package: TDFN2x3-8L, MSOP-8L,SOIC-8L
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### Description

The PI6ULS5V9306 is a dual bidirectional I<sup>2</sup>C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.0 V to 3.3 V (VREF1) and 1.8 V to 5.5 V (VREF2).

The PI6ULS5V9306 allows bidirectional voltage translations between 1.0 V and 5 V without the use of a direction pin. The low ON-state resistance (Ron) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state

exists between ports.

The PI6ULS5V9306 is not a bus buffer that provides both level translation and physically isolates to either side of the bus when both sides are connected. The PI6ULS5V9306 only isolates both sides when the device is disabled and provides voltage level translation when active.

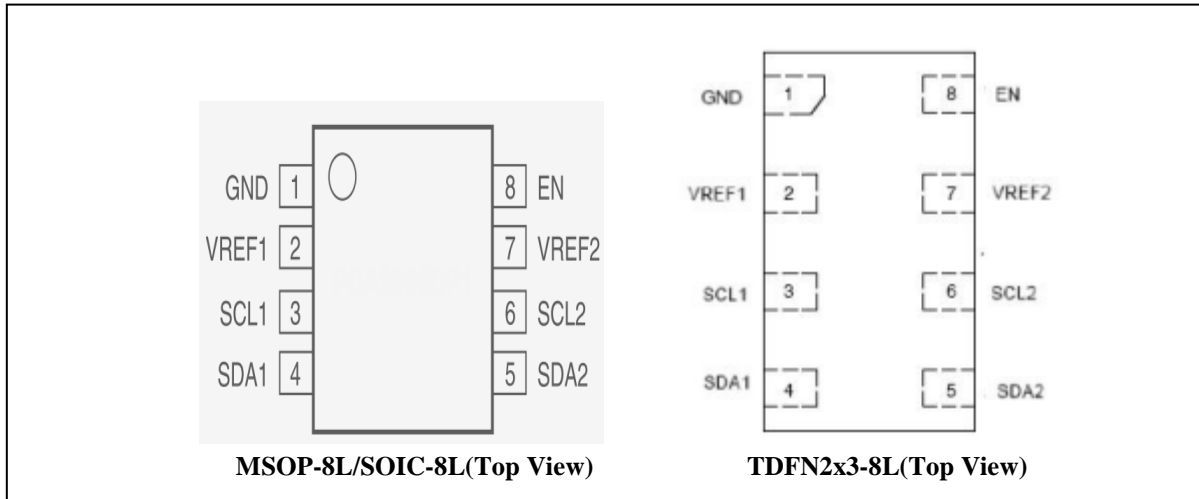
The PI6ULS5V9306 can also be used to run two buses, one at 400 kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400 kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I<sup>2</sup>C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The PI6ULS5V9306 has a standard open-collector configuration of the I<sup>2</sup>C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast mode Plus I<sup>2</sup>C-bus devices in addition to SMBus devices.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. When the higher voltage is on the SDA2 port, and the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage (VDPU) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

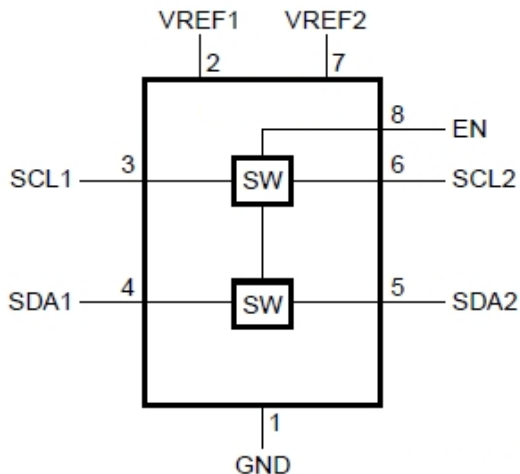
### Pin Configuration



### Pin Description

Pin No	Name	Description
1	GND	ground (0 V)
2	VREF1	low-voltage side reference supply voltage for SCL1 and SDA1
3	SCL1	serial clock, low-voltage side; connect to VREF1 through a pull-up resistor
4	SDA1	serial data, low-voltage side; connect to VREF1 through a pull-up resistor
5	SDA2	serial data, high-voltage side; connect to VREF2 through a pull-up resistor
6	SCL2	serial clock, high-voltage side; connect to VREF2 through a pull-up resistor
7	VREF2	high-voltage side reference supply voltage for SCL2 and SDA2
8	EN	switch enable input; connect to VREF2 and pull-up through a high resistor

### Block Diagram



EN	Function
H	SCL1 = SCL2; SDA1 = SDA2
L	disabled

Figure.1 Block Diagram

## Maximum Ratings

Storage Temperature.....	-65°C to +150°C
Reference Voltage <sup>(2)</sup> .....	-0.5V to +6.0V
Reference bias voltage.....	-0.5V to +6.0V
DC Input Voltage.....	-0.5V to +6.0V
Control Input Voltage(EN).....	-0.5V to +6.0V
channel current (DC).....	128mA
Input clamping Current.....	-50mA
ESD: HBM Mode.....	4000V

### Note:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.

## Recommended operation conditions

VCC = 2.7 V to 5.5 V; GND = 0 V; T<sub>A</sub> = -40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>IO</sub>	Voltage on an input/output pin	SCL1, SDA1, SCL2, SDA2	0	-	5	V
V <sub>REF1</sub>	Reference voltage (1)	VREF1	0	-	5	V
V <sub>REF2</sub>	Reference bias voltage (2)	VREF2	0	-	5	V
V <sub>I(EN)</sub>	Input voltage on pin EN	-	0	-	5	V
I <sub>(pass)</sub>	Pass switch current	-	-	-	64	mA
T <sub>A</sub>	Ambient temperature	-	-40	-	85	°C

## DC Electrical Characteristics

T<sub>A</sub> = -40 °C to +85 °C; unless otherwise specified

Parameter	Description	Test Conditions <sup>(1)</sup>	Min	Typ. <sup>(2)</sup>	Max	Unit	
<b>Input and output SDAB and SCLB</b>							
V <sub>IK</sub>	input clamping voltage	I <sub>I</sub> = -18mA; V <sub>I(EN)</sub> = 0 V	-	-	-1.2	V	
I <sub>IH</sub>	HIGH-level input current	V <sub>I</sub> = 5 V; V <sub>I(EN)</sub> = 0 V	-	-	5	μA	
C <sub>i(EN)</sub>	input capacitance on pin EN	V <sub>I</sub> = 3 V or 0 V	-	11	-	pF	
C <sub>io(off)</sub>	off-state input/output capacitance (SCLn, SDAn)	V <sub>O</sub> = 3 V or 0 V; V <sub>I(EN)</sub> = 0 V	-	4	-	pF	
C <sub>io(on)</sub>	on-state input/output capacitance (SCLn, SDAn)	V <sub>O</sub> = 3 V or 0 V; V <sub>I(EN)</sub> = 3 V	-	10.5	-	pF	
Ron	ON-state resistance <sup>(2)</sup> (SCLn, SDAn)	V <sub>I</sub> = 0V; I <sub>O</sub> = 64mA	V <sub>I(EN)</sub> = 4.5 V	-	3.5	5.5	Ω
			V <sub>I(EN)</sub> = 3 V	-	4.7	7.0	Ω
			V <sub>I(EN)</sub> = 2.3 V	-	6.3	9.5	Ω
			V <sub>I(EN)</sub> = 1.5 V	-	60	140	Ω
		V <sub>I</sub> = 2.4V; I <sub>O</sub> = 15mA	V <sub>I(EN)</sub> = 4.5 V	1	6	15	Ω
			V <sub>I(EN)</sub> = 3 V	20	60	140	Ω
			V <sub>I(EN)</sub> = 2.3 V	20	60	140	Ω

### Notes:

1) All typical values are at T<sub>A</sub> = 25 °C.

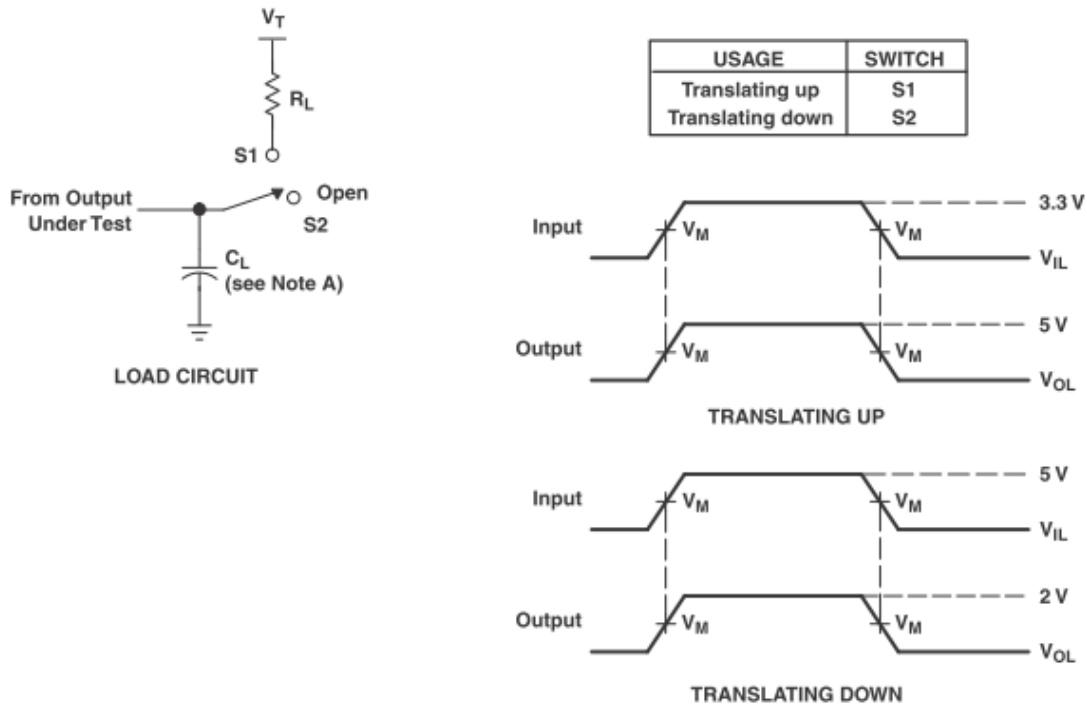
2) Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch. ON-state resistance is determined by the lowest voltage of the two terminals.

### Dynamic characteristics

$T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ ; unless otherwise specified. Values guaranteed by design.

Symbol	Parameter	Conditions	$C_L = 50\text{ pF}$		$C_L = 30\text{ pF}$		$C_L = 15\text{ pF}$		Unit
			Min	Max	Min	Max	Min	Max	
$V_{I(EN)} = 3.3\text{ V}; V_{IH} = 3.3\text{ V}; V_{IL} = 0\text{ V}; V_M = 1.15\text{ V}$									
$t_{PLH}$	LOW-to-HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	0.8	0	0.6	0	0.3	ns
$t_{PHL}$	HIGH-to-LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1.2	0	1	0	0.5	ns
$V_{I(EN)} = 2.5\text{ V}; V_{IH} = 3.3\text{ V}; V_{IL} = 0\text{ V}; V_M = 0.75\text{ V}$									
$t_{PLH}$	LOW-to-HIGH propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1	0	0.7	0	0.4	ns
$t_{PHL}$	HIGH-to-LOW propagation delay	from (input) SCL2 or SDA2 to (output) SCL1 or SDA1	0	1.3	0	1	0	0.6	ns
$V_{I(EN)} = 3.3\text{ V}; V_{IH} = 2.3\text{ V}; V_{IL} = 0\text{ V}; V_T = 3.3\text{ V}; V_M = 1.15\text{ V}; R_L = 300$									
$t_{PLH}$	LOW-to-HIGH propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	0.9	0	0.6	0	0.4	ns
$t_{PHL}$	HIGH-to-LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.4	0	1.1	0	0.7	ns
$V_{I(EN)} = 2.5\text{ V}; V_{IH} = 1.5\text{ V}; V_{IL} = 0\text{ V}; V_T = 2.5\text{ V}; V_M = 0.75\text{ V}; R_L = 300$									
$t_{PLH}$	LOW-to-HIGH propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1	0	0.6	0	0.4	ns
$t_{PHL}$	HIGH-to-LOW propagation delay	from (input) SCL1 or SDA1 to (output) SCL2 or SDA2	0	1.3	0	1.3	0	0.8	ns

### PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 C. The outputs are measured one at a time, with one transition per measurement.

Figure.2 Load Circuit for Outputs

## Functional Description

The PI6ULS5V9306 is a dual bidirectional I<sup>2</sup>C-bus and SMBus voltage-level translator with an enable (EN) input, and is operational from 1.2 V to 3.3 V (VREF1) and 1.8 V to 5.5 V (VREF2).

The PI6ULS5V9306 allows bidirectional voltage translations between 1.2 V and 5 V without the use of a direction pin. The low ON-state resistance (Ron) of the switch allows connections to be made with minimal propagation delay. When EN is HIGH, the translator switch is on, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports.

The PI6ULS5V9306 is not a bus buffer that provides both level translation and physically isolates to either side of the bus when both sides are connected. The PI6ULS5V9306 only isolates both sides when the device is disabled and provides voltage level translation when active.

The PI6ULS5V9306 can also be used to run two buses, one at 400kHz operating frequency and the other at 100 kHz operating frequency. If the two buses are operating at different frequencies, the 100 kHz bus must be isolated when the 400 kHz operation of the other bus is required. If the master is running at 400kHz, the maximum system operating frequency may be less than 400 kHz because of the delays added by the translator.

As with the standard I<sup>2</sup>C-bus system, pull-up resistors are required to provide the logic HIGH levels on the translator's bus. The PI6ULS5V9306 has a standard open-collector configuration of the I<sup>2</sup>C-bus. The size of these pull-up resistors depends on the system, but each side of the translator must have a pull-up resistor. The device is designed to work with Standard-mode, Fast-mode and Fast mode Plus I<sup>2</sup>C-bus devices in addition to SMBus devices.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. When the higher voltage is on the SDA2 port, and the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by VREF1. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage (VDPU) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical. The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

## Application Information

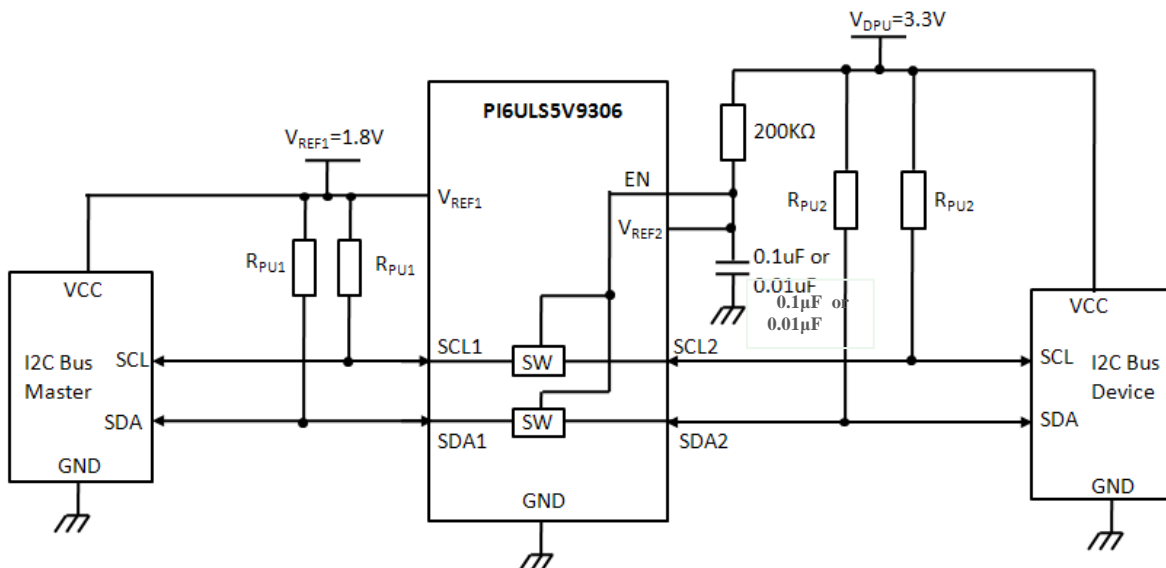


Figure.3 Typical Open Drain Application Circuit (Switch Always Enabled )

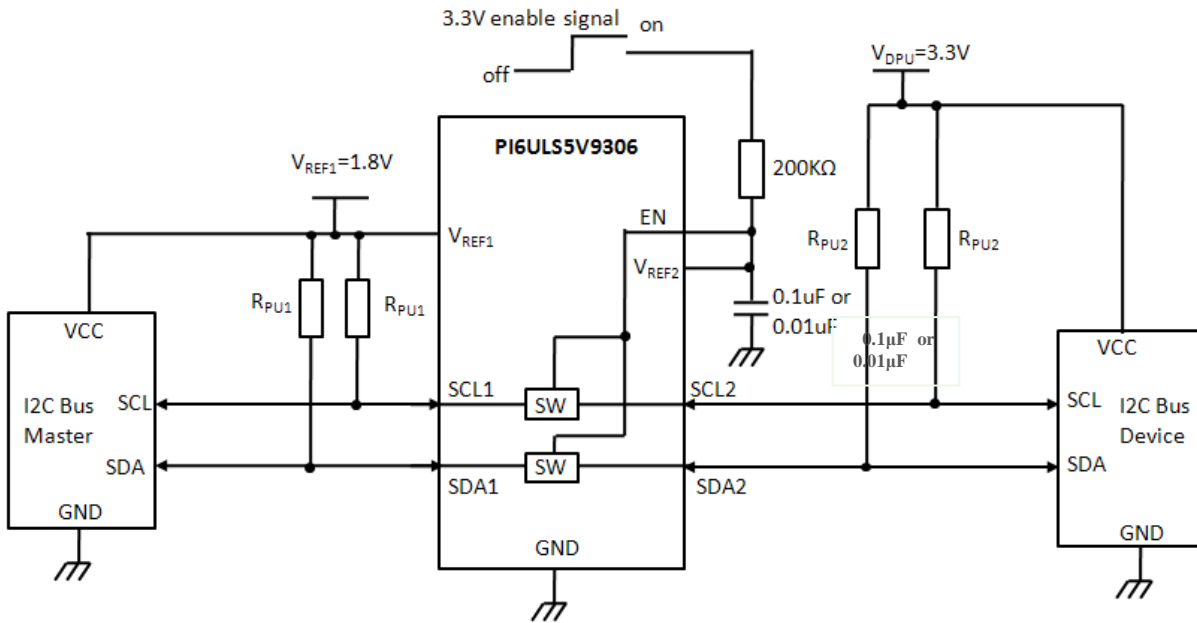


Figure.4 Typical Open Drain Application Circuit (Switch Enabled Control)

### Open Drain Application

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to VREF2 and both pins pulled to high-side V<sub>DPU</sub> through a pull-up resistor (typically 200 kΩ). This allows VREF2 to regulate the EN input. A filter capacitor on VREF2 is recommended.

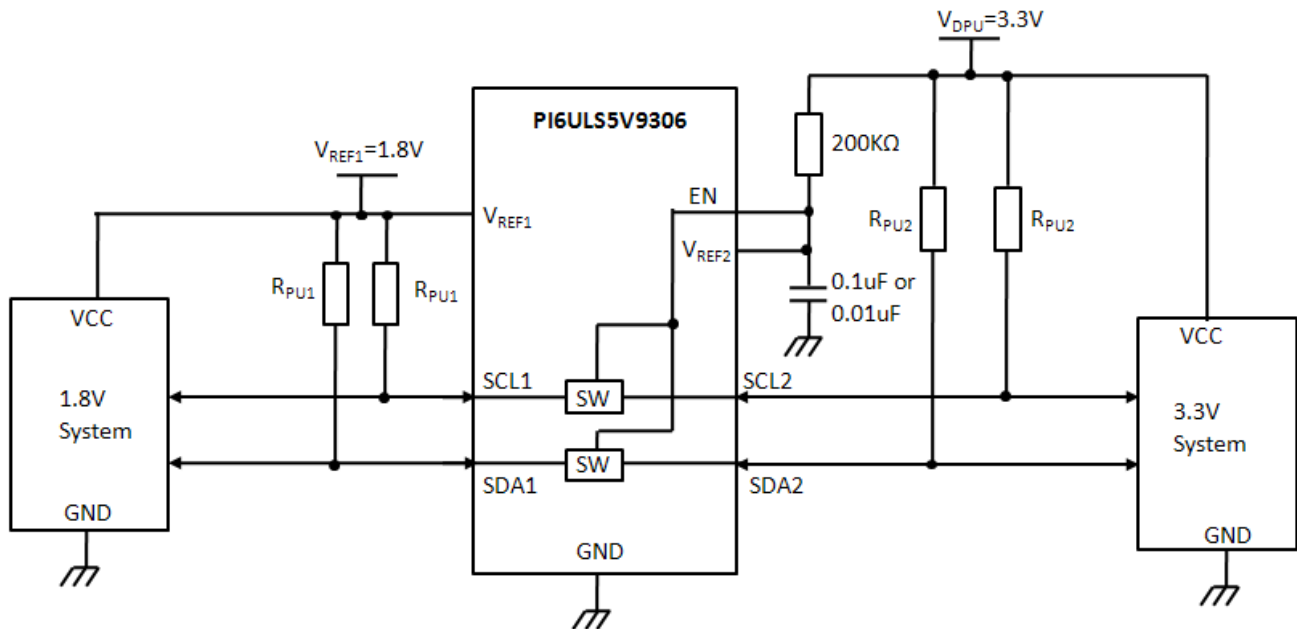


Figure.5 Typical push-pull Application Circuit (Switch Enabled Control)

### Push Pull Application

If used in push-pull system, the pull-up resistors on REF side are also needed. The data must be unidirectional or the outputs must be 3-stateable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction.

## Operating Voltage

Refer to Figure 2

		MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>DPU</sub>	Ref2 side pull-up voltage on 200kΩ	V <sub>REF1</sub> + 0.6	2.1	5	V
EN	Enable input voltage	V <sub>REF1</sub> + 0.6	2.1	5	V
V <sub>REF1</sub>	Reference voltage	0	1.5	4.4	V
I <sub>PASS</sub>	Pass switch current		14		mA
I <sub>REF</sub>	Reference-transistor current		5		μA
T <sub>A</sub>	Operating free-air temperature	-40		85	°C

### The pass through current : I<sub>pass</sub>

I<sub>pass</sub> is determined by the pull-up and the low voltage added on the PI6LS5V9306

In figure 6,  $I_{pass} = (V_{REF1} - V_{OL1\_9306}) / R_{PU1}$

When V<sub>IN</sub> is 0V, the PI6ULS5V9306 can support as large as 64mA pass through current in theory. But we recommend it's better to limit the I<sub>pass</sub> in 15mA

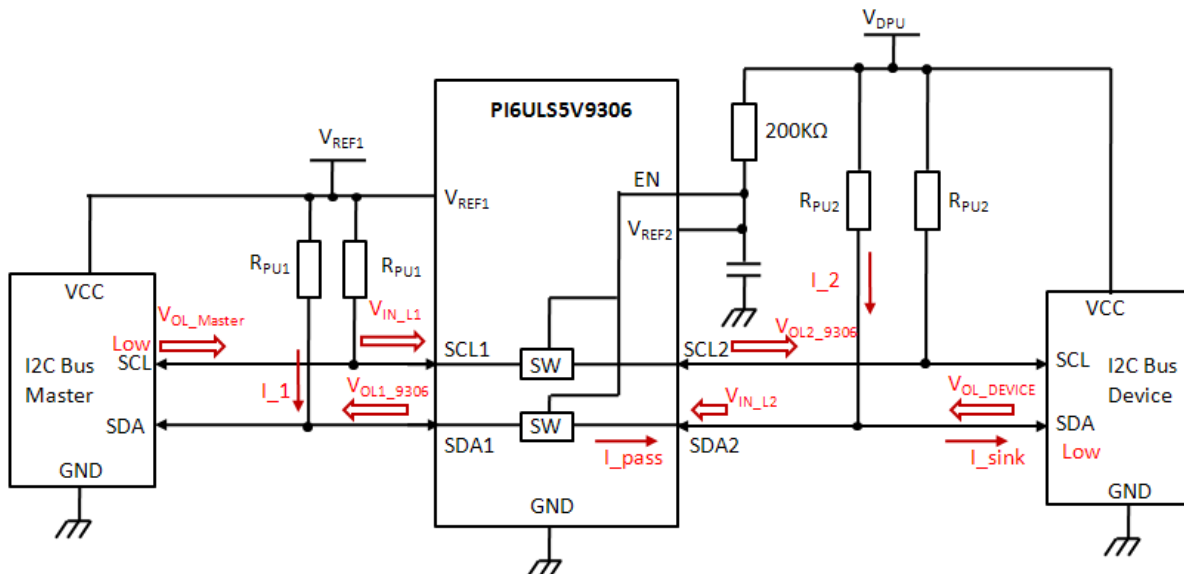


Figure 6. Typical Open Drain Application Circuit

(1) The sink current : I<sub>sink</sub>

The device would sink the total current from both pull-up resistors.

For example, in figure below, when the SDA2 is pulled low by the I2C device, the sink current of the I2C device  $I_{sink} = I_{pass} + I_2 = I_1 + I_2$ . The same thing will happen when I2C master pull low the I2C bus.

The I<sub>sink</sub> should be limited to not larger than the tolerance of the I2C devices.

(2) V<sub>IL</sub>, V<sub>OL</sub> of the external drive and V<sub>OL</sub> of PI6ULS5V9306

In normal application, the V<sub>IL</sub> of external devices should always be larger than the V<sub>OL</sub> of PI6ULS5V9306.

The value of PI6ULS5V9306's V<sub>OL</sub> is determined by the pass through current and the low voltage added on the SDA, SCL pins. The  $V_{OL\_9306} = V_{IN\_L} + V_{UP}$  (V<sub>UP</sub> is mainly determined by the I<sub>pass</sub>, it always less than 0.35V.)

(3) Low VREF application

The PI6ULS5V9306 can support very low Vref1 application in theory, but we recommend not lower than 0.9V. Because when VREF1 is less than 1.8V, the V<sub>OL</sub> of REF1 side is a concern in system.

For example, in figure 6, if VREF1=0.9V, V<sub>DPU</sub>=3.3V the V<sub>IL</sub> of the REF1 side I2C master is normally  $0.3 * V_{REF1} = 0.25V$ , but the V<sub>OL</sub> of REF2 side can up to  $0.1 * V_{DPU} = 0.36V$  sometimes.

The system designer must make sure this situation doesn't happen. A limit for the V<sub>OL</sub> of REF2 side devices is required then.

The bellow table shows the requirement for  $V_{OL}$  of VREF2 side devices when using PI6ULS5V9306 (Requirement for  $V_{OL\_DEVICE}$  in figure 6)

The $V_{OL}$ requirement of $V_{REF2}$ side external devices (Temp=25 °C, Assume the $V_{IL}$ of $V_{REF1}$ side devices is $0.3 \cdot V_{REF1}$ )			
$V_{REF1}$ \ $I_{pass}$	$\leq 3mA$	10mA	15mA
0.9V	$\leq 0.15V$	$\leq 0.1V$	Not Recommended
1.2V	$\leq 0.2V$	$\leq 0.15V$	Not Recommended
1.5V	$\leq 0.3V$	$\leq 0.25V$	$\leq 0.2V$
1.8V	$\leq 0.4V$	$\leq 0.35V$	$\leq 0.3V$

### Pull-up resistors and minimum values

Sizing the pull-up resistor on an open-drain bus is specific to the individual application and is dependent on the following driver characteristics:

- The driver sink current
- The  $V_{OL}$  of driver
- The  $V_{OL}$  of the PI6ULS5V9306
- The  $V_{IL}$  of the driver
- Frequency of operation

The following tables can be used to estimate the pull-up resistor value in different use cases so that the minimum resistance for the pull-up resistor can be found.

Tables in bellow contain suggested minimum values of pull-up resistors for the PI6UULS5V9306 with typical voltage translation levels and drive currents.

The calculated values assume that both drive currents are the same.

$V_{OL} = V_{IL} = 0.1 \cdot V_{CC}$  and accounts for a 5 % VCC tolerance of the supplies, 1 % resistor values. It should be noted that the resistor chosen in the final application should be equal to or larger than the values shown in the table to ensure that the pass voltage is less than 10 % of the VCC voltage, and the external driver should be able to sink the total current from both pull-up resistors.

Pull-up resistor minimum values, 3 mA driver sink current for PI6ULS5V9306

A Side	B side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.9V	$R_{PU(A)} = 845\Omega$ $R_{PU(B)} = 845\Omega$	$R_{PU(A)} = 976\Omega$ $R_{PU(B)} = 976\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 887\Omega$ Or both 1.2k $\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 1.18k\Omega$ Or both 1.5k $\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 1.82k\Omega$ Or both 2.15k $\Omega$
1.2V		$R_{PU(A)} = 1.02k\Omega$ $R_{PU(B)} = 1.02k\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 887\Omega$ Or both 1.3k $\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 1.18k\Omega$ Or both 1.5k $\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 1.82k\Omega$ Or both 2.25k $\Omega$
1.5V			$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 866\Omega$ Or both 1.38k $\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 1.18k\Omega$ Or both 1.5k $\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 1.78k\Omega$ Or both 2.31k $\Omega$
1.8V			$R_{PU(A)} = 1.47k\Omega$ $R_{PU(B)} = 1.47k\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 1.15k\Omega$ Or both 1.5k $\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 1.78k\Omega$ Or both 2.42k $\Omega$
2.5V				$R_{PU(A)} = 1.96k\Omega$ $R_{PU(B)} = 1.96k\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 1.78k\Omega$ Or both 2.67k $\Omega$
3.3V					$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 1.74k\Omega$ Or both 2.95k $\Omega$



Pull-up resistor minimum values, 10 mA driver sink current for PI6ULS5V9306

A Side	B side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.9V	$R_{PU(A)} = 255\Omega$ $R_{PU(B)} = 255\Omega$	$R_{PU(A)} = 287\Omega$ $R_{PU(B)} = 287\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 267\Omega$ Or both 363Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 357\Omega$ Or both 449Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 549\Omega$ Or both 648Ω
1.2V		$R_{PU(A)} = 309\Omega$ $R_{PU(B)} = 309\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 267\Omega$ Or both 395Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 357\Omega$ Or both 481Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 549\Omega$ Or both 681Ω
1.5V			$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 261\Omega$ Or both 427Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 348\Omega$ Or both 506Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 536\Omega$ Or both 697Ω
1.8V			$R_{PU(A)} = 442\Omega$ $R_{PU(B)} = 442\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 348\Omega$ Or both 538Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 536\Omega$ Or both 729Ω
2.5V				$R_{PU(A)} = 590\Omega$ $R_{PU(B)} = 590\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 521\Omega$ Or both 782Ω
3.3V					$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 521\Omega$ Or both 865Ω

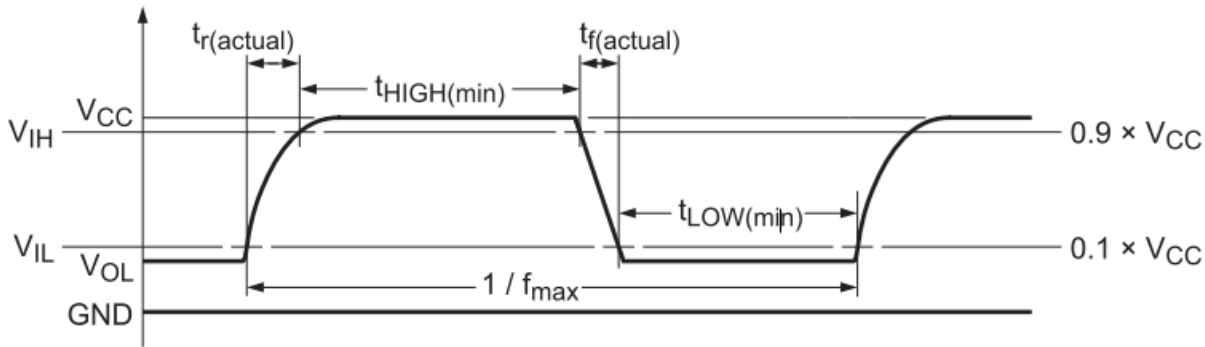
Pull-up resistor minimum values, 15 mA driver sink current for PI6ULS5V9306

A Side	B side				
	1.5V	1.8V	2.5V	3.3V	5.0V
0.9V	$R_{PU(A)} = 169\Omega$ $R_{PU(B)} = 169\Omega$	$R_{PU(A)} = 191\Omega$ $R_{PU(B)} = 191\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 178\Omega$ Or both 242Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 237\Omega$ Or both 302Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 365\Omega$ Or both 431Ω
1.2V		$R_{PU(A)} = 205\Omega$ $R_{PU(B)} = 205\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 178\Omega$ Or both 263Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 237\Omega$ Or both 323Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 365\Omega$ Or both 453Ω
1.5V			$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 174\Omega$ Or both 278Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 232\Omega$ Or both 337Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 464\Omega$ Or both 697Ω
1.8V			$R_{PU(A)} = 294\Omega$ $R_{PU(B)} = 294\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 232\Omega$ Or both 359Ω	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 486\Omega$ Or both 729Ω
2.5V				$R_{PU(A)} = 392\Omega$ $R_{PU(B)} = 392\Omega$	$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 536\Omega$ Or both 782Ω
3.3V					$R_{PU(A)} = \text{none}$ $R_{PU(B)} = 348\Omega$ Or both 578Ω

**Max Frequency Application**

The maximum frequency is limited by the minimum pulse width LOW and HIGH as well as rise time and fall time.

$$f(\text{max}) = \frac{1}{t_{\text{LOW}}(\text{min}) + t_{\text{HIGH}}(\text{min}) + t_{\text{r}}(\text{actual}) + t_{\text{f}}(\text{actual})}$$



The rise and fall times are dependent upon translation voltages, the drive strength, the total node capacitance (CL) and the pull-up resistors (RPU) that are present on the bus. The node capacitance is the addition of the PCB trace capacitance and the device capacitance that exists on the bus.

Because of the dependency of the external components, PCB layout and the different device operating states the calculation of rise and fall times is complex and has several inflection points along the curve.

The main component of the rise and fall times is the RC time constant of the bus line when the device is in its two primary operating states: when device is in the ON state and it is low-impedance, the other is when the device is OFF isolating the A-side from the B-side.

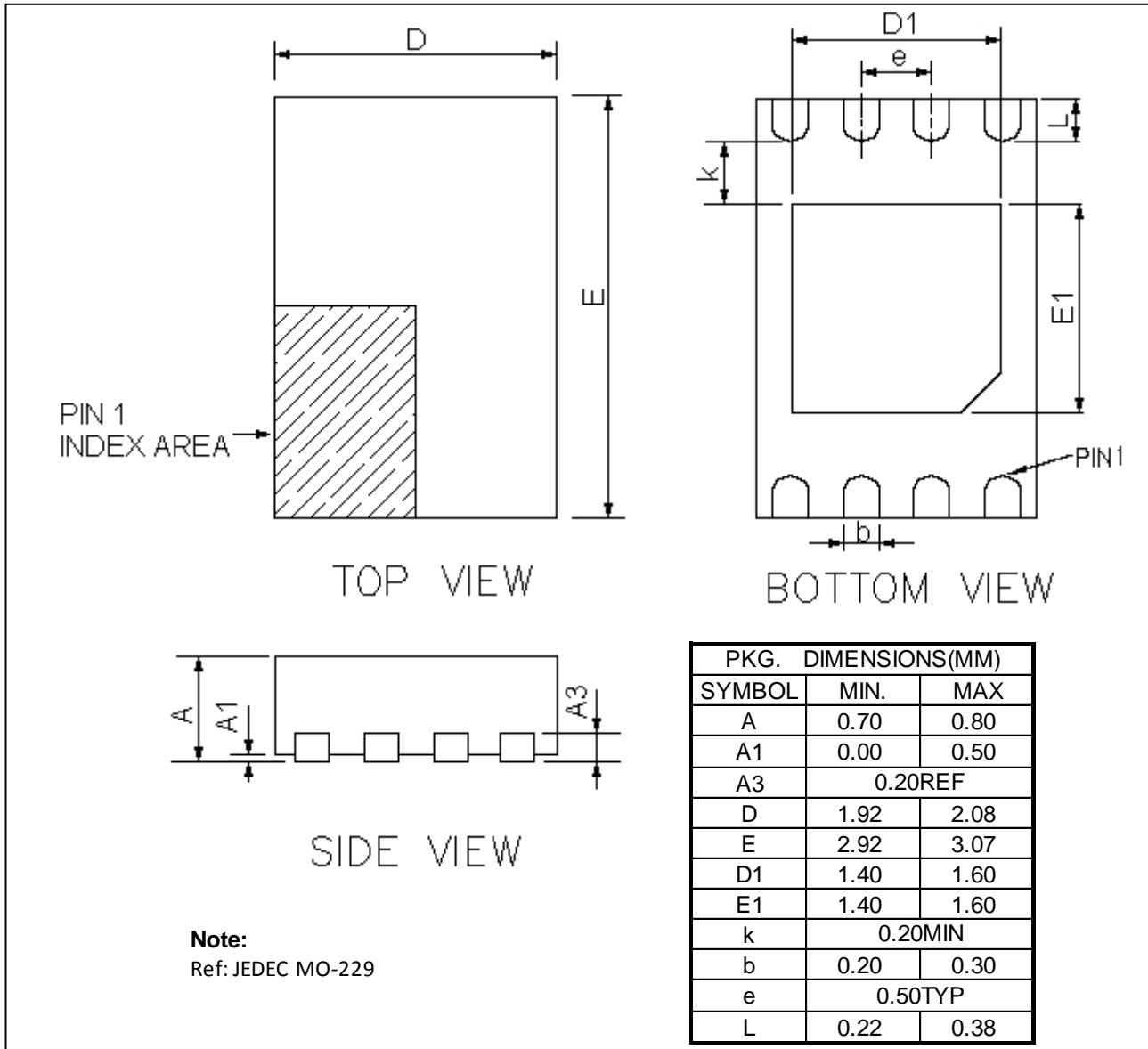
There are some basic guidelines to follow that will help maximize the performance of the device:

- Keep trace length to a minimum by placing the PI6ULS5V9306 close to the processor.
- The signal round trip time on trace should be shorter than the rise or fall time of signal to reduce reflections.
- The faster the edge of the signal, the higher the chance for ringing.
- The higher drive strength controlled by the pull-up resistor (up to 15 mA), the higher the frequency the device can use.

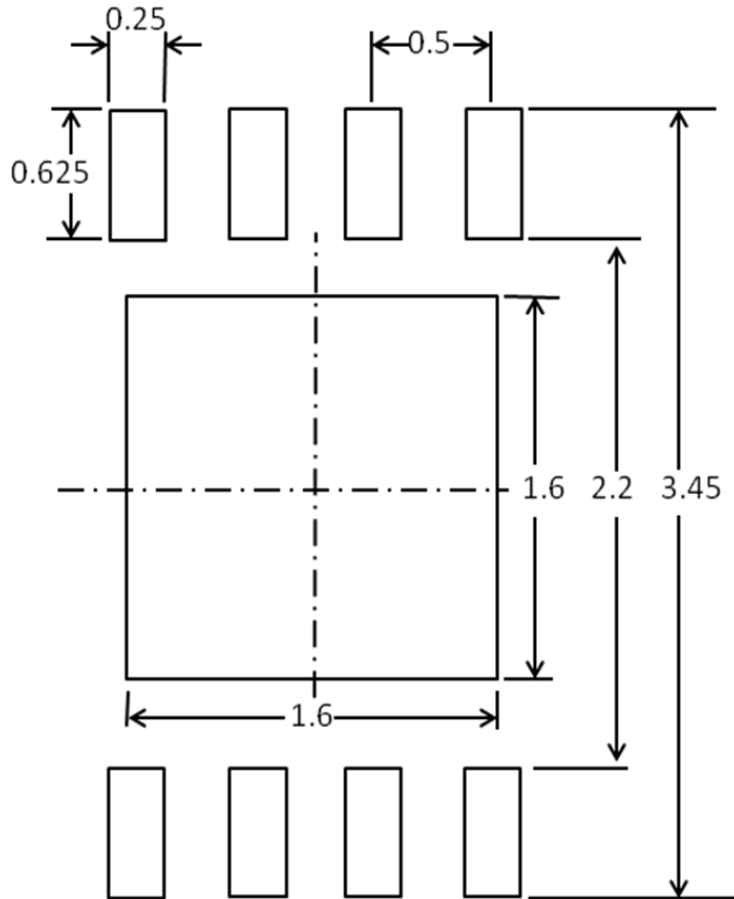
The system designer must design the pull-up resistor value based on external current drive strength and limit the node capacitance (minimize the wire, stub, connector and trace length) to get the desired operation frequency result.

### Mechanical Information

TDFN2x3-8(ZE)

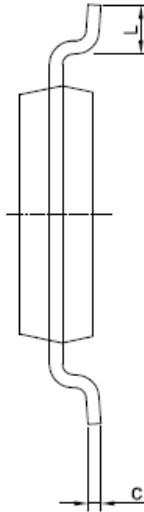
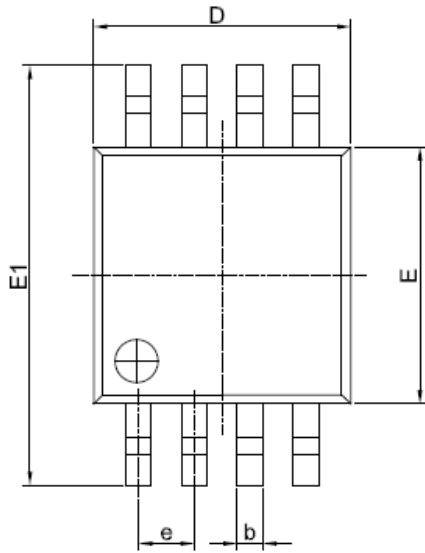


Recommended Land pattern for TDFN2x3-8L

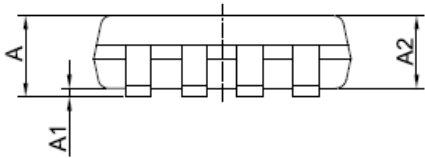


Note:  
All linear dimensions are in millimeters

MSOP-8(U)



PKG. DIMENSIONS(MM)		
SYMBOL	Min.	Max.
A	-	1.10
A1	0.00	0.15
A2	0.75	0.95
b	0.22	0.38
c	0.08	0.23
D	2.90	3.10
E	2.90	3.10
E1	4.65	5.15
e	0.65 BSC	
L	0.40	0.80
θ	0°	8°



NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. REFER JEDEC MO-187E/AA
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR.



DATE: 10/20/14

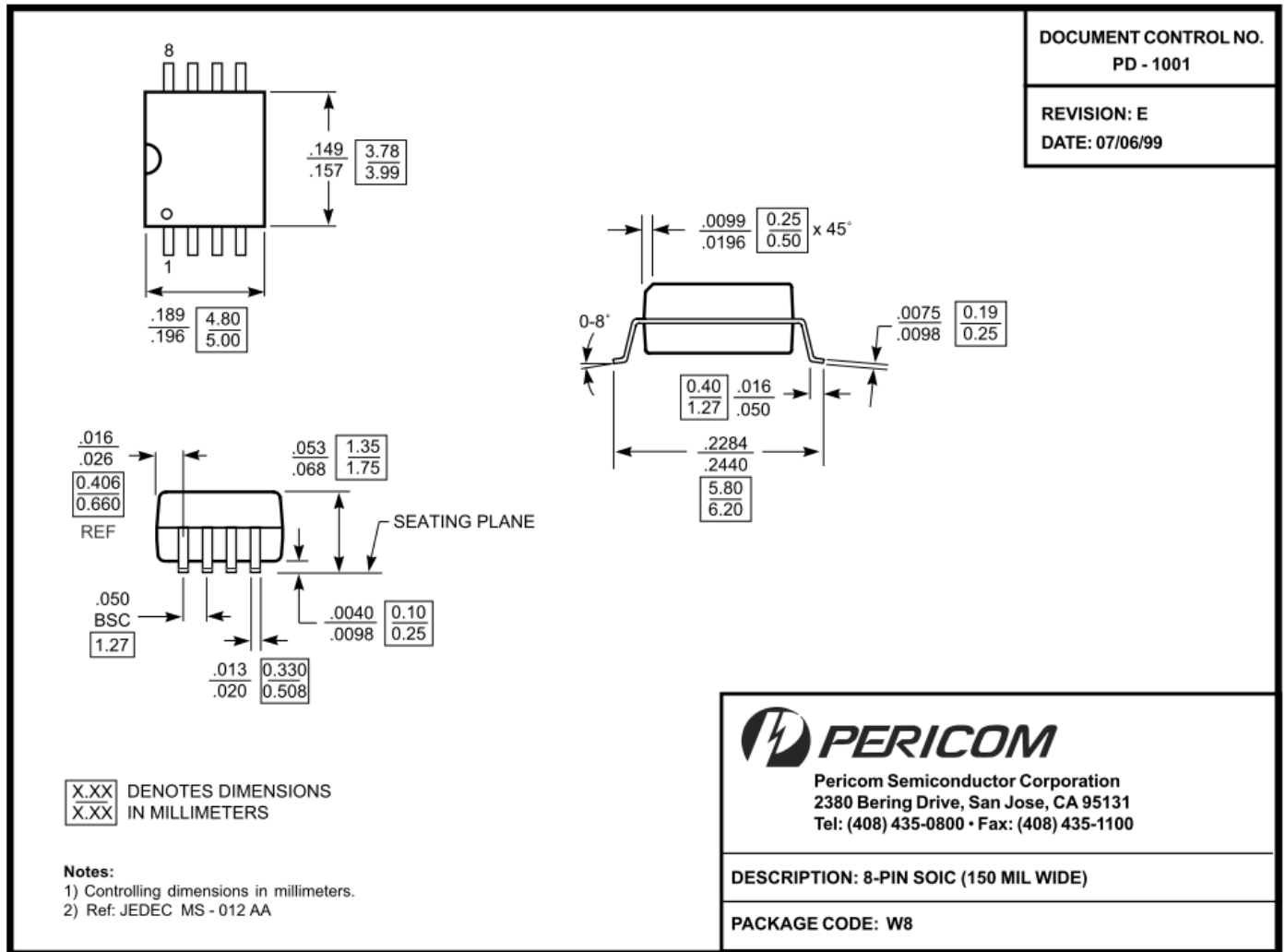
DESCRIPTION: 8-Pin, Mini Small Outline Package, MSOP

PACKAGE CODE: U (U8)

DOCUMENT CONTROL #: PD-1261

REVISION: E

SOIC-8(W)



### Ordering Information

Part No.	Package Code	Package
PI6ULS5V9306ZEEX	ZE	Lead free and Green TDFN2x3-8L,Tape & Reel
PI6ULS5V9306UE	U	Lead free and Green MSOP-8L
PI6ULS5V9306UEX	U	Lead free and Green MSOP-8L,Tape & Reel
PI6ULS5V9306WE	W	8-Pin,150 mil Wide SOIC
PI6ULS5V9306WEX	W	8-Pin,150 mil Wide SOIC, Tape & Reel

**Note:**

- E = Pb-free and Green
- Adding X Suffix= Tape/Reel

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