**CY2CP1504**

# 1:4 LVCMOS to LVPECL Fanout Buffer with Selectable Clock Input

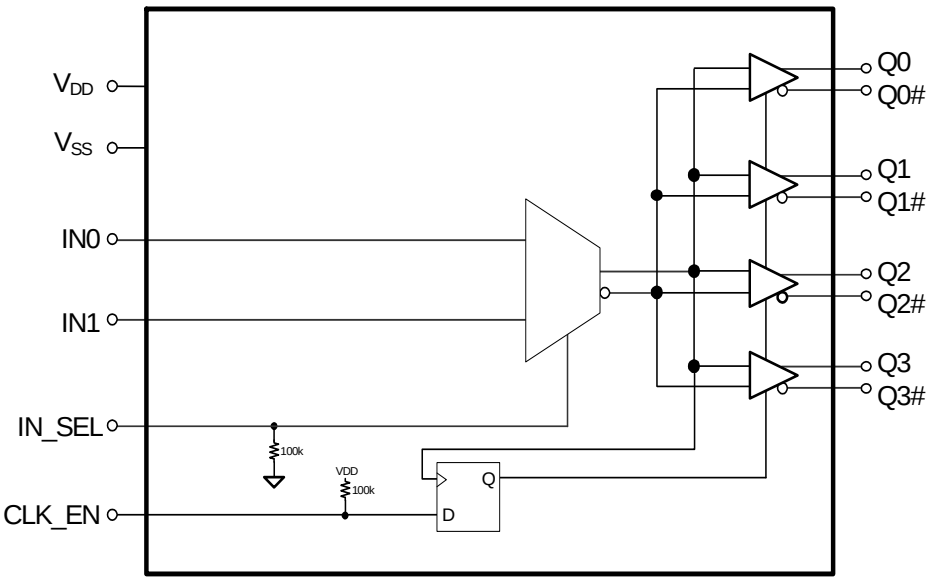
## Features

- Select one of two low-voltage complementary metal oxide semiconductor (LVCMOS) inputs to distribute to four low-voltage positive emitter-coupled logic (LVPECL) output pairs
- 30-ps maximum output-to-output skew
- 480-ps maximum propagation delay
- 0.15-ps maximum additive RMS phase jitter at 156.25 MHz (12-kHz to 20-MHz offset)
- Up to 250 MHz operation
- Synchronous clock enable function
- 20-Pin thin shrunk small outline package (TSSOP) package
- 2.5-V or 3.3-V operating voltage[1]
- Commercial and industrial operating temperature range

## Functional Description

The CY2CP1504 is an ultra-low noise, low-skew, low-propagation delay 1:4 LVCMOS to LVPECL fanout buffer targeted to meet the requirements of high-speed clock distribution applications. The CY2CP1504 can select between two separate LVCMOS input clocks using the IN_SEL pin. The synchronous clock enable function ensures glitch-free output transitions during enable and disable periods. The device has a fully differential internal architecture that is optimized to achieve low additive jitter and low skew at operating frequencies of up to 250 MHz.

## Logic Block Diagram




**Note**
1. Input AC-coupling capacitors are required for voltage-translation applications.

## Contents

## Pinouts

**Figure 1. Pin Diagram – 20-Pin TSSOP Package**

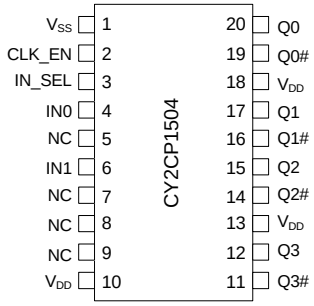



**Table 1. Pin Definitions**

| Pin No. | Pin Name | Pin Type | Description |
|---|---|---|---|
| 1 | $V_{SS}$ | Power | Ground |
| 2 | CLK_EN | Input | Synchronous clock enable. LVCMOS/low-voltage transistor-transistor logic (LVTTL).<br>When CLK_EN = Low, Q(0:3) outputs are held low and Q(0:3)# outputs are held high |
| 3 | IN_SEL | Input | Input clock select pin. LVCMOS/LVTTL;<br>When IN_SEL = Low, input IN0 is active<br>When IN_SEL = High, input IN1 is active |
| 4 | IN0 | Input | LVCMOS input clock. Active when IN_SEL = Low |
| 5,7,8,9 | NC | | No connection |
| 6 | IN1 | Input | LVCMOS input clock. Active when IN_SEL = High |
| 10,13,18 | $V_{DD}$ | Power | Power supply |
| 11,14,16,19 | Q(0:3)# | Output | LVPECL complementary output clocks |
| 12,15,17,20 | Q(0:3) | Output | LVPECL output clocks |

## Absolute Maximum Ratings

| Parameter | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | Nonfunctional | –0.5 | 4.6 | V |
| $V_{IN}$[2] | Input voltage, relative to $V_{SS}$ | Nonfunctional | –0.5 | lesser of 4.0 or $V_{DD}$ + 0.4 | V |
| $V_{OUT}$[2] | DC output or I/O voltage, relative to $V_{SS}$ | Nonfunctional | –0.5 | lesser of 4.0 or $V_{DD}$ + 0.4 | V |
| $T_S$ | Storage temperature | Nonfunctional | –55 | 150 | °C |
| $ESD_{HBM}$ | Electrostatic discharge (ESD) protection (Human body model) | JEDEC STD 22-A114-B | 2000 | – | V |
| $L_U$ | Latch up | | Meets or exceeds JEDEC Spec JESD78B IC Latchup Test | | |
| UL–94 | Flammability rating | At 1/8 in | V-0 | | |
| MSL | Moisture sensitivity level | | 3 | | |

## Operating Conditions

| Parameter | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 2.5-V supply | 2.375 | 2.625 | V |
| | | 3.3-V supply | 3.135 | 3.465 | V |
| $T_A$ | Ambient operating temperature | Commercial | 0 | 70 | °C |
| | | Industrial | –40 | 85 | °C |
| $t_{PU}$ | Power ramp time | Power-up time for $V_{DD}$ to reach minimum specified voltage (power ramp must be monotonic) | 0.05 | 500 | ms |

**Note**
2. The voltage on any I/O pin cannot exceed the power pin during power up. Power supply sequencing is not required.

## DC Electrical Specifications

($V_{DD}$ = 3.3 V ± 5% or 2.5 V ± 5%; $T_A$ = 0 °C to 70 °C (Commercial) or –40 °C to 85 °C (Industrial))

| Parameter | Description | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{DD}$ | Operating supply current | All LVPECL outputs floating (internal $I_{DD}$) | – | 61 | mA |
| $V_{IH1}$ | Input high voltage, All inputs | $V_{DD}$ = 3.3 V | 2.0 | $V_{DD}$ + 0.3 | V |
| $V_{IL1}$ | Input low voltage, All inputs | $V_{DD}$ = 3.3 V | –0.3 | 0.8 | V |
| $V_{IH2}$ | Input high voltage, All inputs | $V_{DD}$ = 2.5 V | 1.7 | $V_{DD}$ + 0.3 | V |
| $V_{IL2}$ | Input low voltage, All inputs | $V_{DD}$ = 2.5 V | –0.3 | 0.7 | V |
| $I_{IH}$ | Input high current, All inputs | Input = $V_{DD}$[3] | – | 150 | µA |
| $I_{IL}$ | Input low current, All inputs | Input = $V_{SS}$[3] | –150 | – | µA |
| $V_{OH}$ | LVPECL output high voltage | Terminated with 50 Ω to $V_{DD}$ – 2.0[4] | $V_{DD}$ – 1.20 | $V_{DD}$ – 0.70 | V |
| $V_{OL}$ | LVPECL output low voltage | Terminated with 50 Ω to $V_{DD}$ – 2.0[4] | $V_{DD}$ – 2.0 | $V_{DD}$ – 1.63 | V |
| $R_P$ | Internal pull-up/pull-down resistance | CLK_EN has pull-up only<br>IN_SEL has pull-down only | 60 | 140 | kΩ |
| $C_{IN}$ | Input capacitance | Measured at 10 MHz; per pin | – | 3 | pF |

**Notes**
3. Positive current flows into the input pin, negative current flows out of the input pin.
4. Refer to Figure 2 on page 7.

## AC Electrical Specifications

($V_{DD}$ = 3.3 V ± 5% or 2.5 V ± 5%; $T_A$ = 0 °C to 70 °C (Commercial) or –40 °C to 85°C (Industrial))

| Parameter | Description | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $F_{IN}$ | Input frequency | | DC | – | 250 | MHz |
| $F_{OUT}$ | Output frequency | $F_{OUT} = F_{IN}$ | DC | – | 250 | MHz |
| $V_{PP}$ | LVPECL differential output voltage peak- to-peak, single-ended. Terminated with 50 Ω to $V_{DD}$ – 2.0[4] | Fout = DC to 150 MHz | 600 | – | – | mV |
| | | Fout = >150 MHz to 250 MHz | 400 | – | – | mV |
| $t_{PD}$[5] | Propagation delay input to output pair | Input rise/fall time < 1.5 ns (20% to 80%) | – | – | 480 | ps |
| $t_{ODC}$[6] | Output duty cycle | Rail-to-rail input swing, 50% input DTCY measured at Vdd/2 | 45 | – | 55 | % |
| $t_{SK1}$[7] | Output-to-output skew | Any output to any output, with same load conditions at DUT | – | – | 30 | ps |
| $t_{SK1\ D}$[7] | Device-to-device output skew | Any output to any output between two or more devices. Devices must have the same input and have the same output load. | – | – | 150 | ps |
| $PN_{ADD}$ | Additive RMS phase noise 156.25-MHz Input Rise/fall time < 150 ps (20% to 80%) $V_{ID}$ > 400 mV | Offset = 1 kHz | – | – | –120 | dBc/Hz |
| | | Offset = 10 kHz | – | – | –130 | dBc/Hz |
| | | Offset = 100 kHz | – | – | –135 | dBc/Hz |
| | | Offset = 1 MHz | – | – | –150 | dBc/Hz |
| | | Offset = 10 MHz | – | – | –150 | dBc/Hz |
| | | Offset = 20 MHz | – | – | –150 | dBc/Hz |
| $t_{JIT}$[8] | Additive RMS phase jitter (Random) | 156.25 MHz sinewave, 12 kHz to 20 MHz offset; input swing = 2.2V, $V_{bias} = V_{DD}/2$ | – | – | 0.15 | ps |
| $t_R$, $t_F$[9] | Output rise/fall time | 50% duty cycle at input, 20% to 80% of full swing ($V_{OL}$ to $V_{OH}$) Input rise/fall time < 1.5 ns (20% to 80%) | – | – | 300 | ps |
| $t_{SOD}$ | Time from clock edge to outputs disabled | Synchronous clock enable (CLK_EN) switched Low | – | – | 700 | ps |
| $t_{SOE}$ | Time from clock edge to outputs enabled | Synchronous clock enable (CLK_EN) switched high | – | – | 700 | ps |

**Notes**
5. Refer to Figure 3 on page 7.
6. Refer to Figure 4 on page 7.
7. Refer to Figure 5 on page 7.
8. Refer to Figure 6 on page 8.
9. Refer to Figure 7 on page 8.

**Figure 2. Output Differential Voltage**

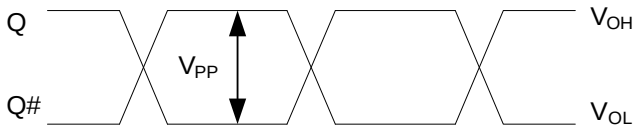



**Figure 3. Input to Any Output Pair Propagation Delay**

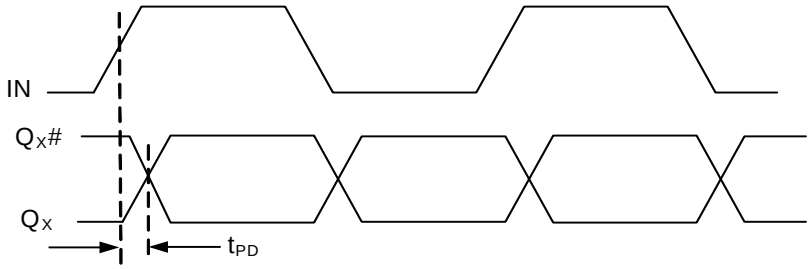



**Figure 4. Output Duty Cycle**

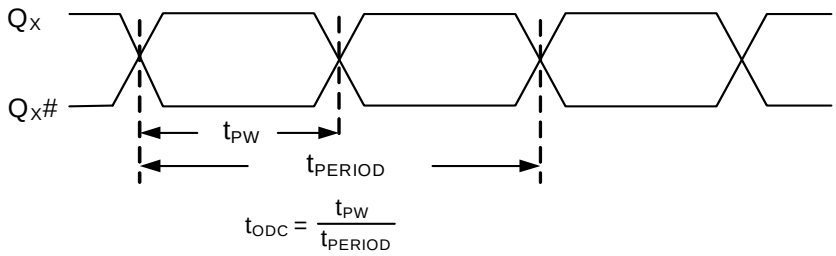



**Figure 5. Output-to-Output and Device-to-Device Skew**

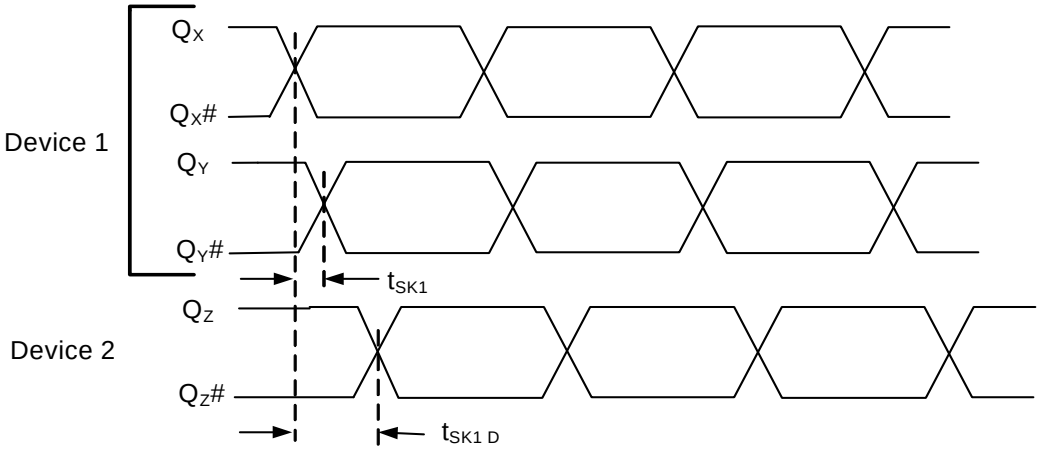


**Figure 6. RMS Phase Jitter**

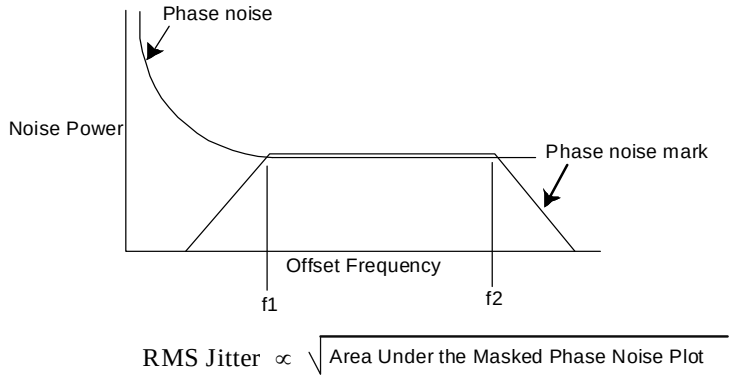



**Figure 7. Output Rise/Fall Time**

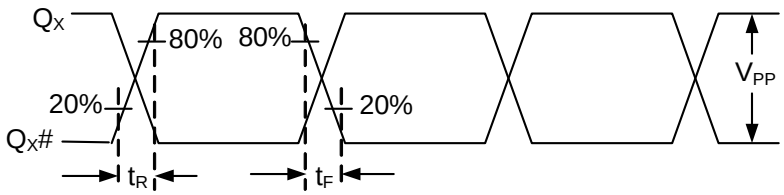
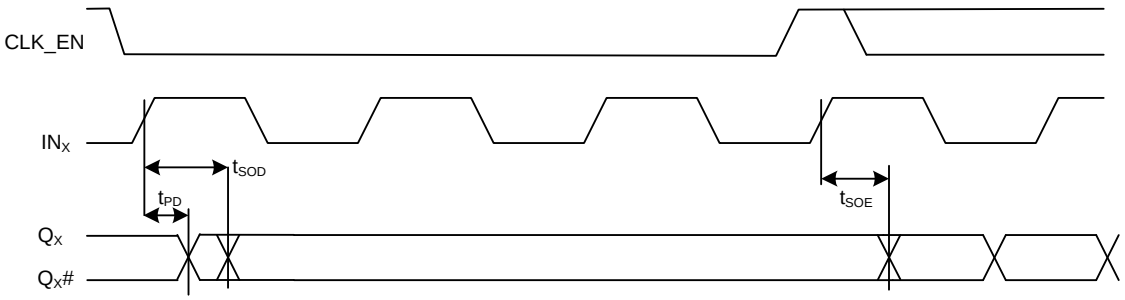


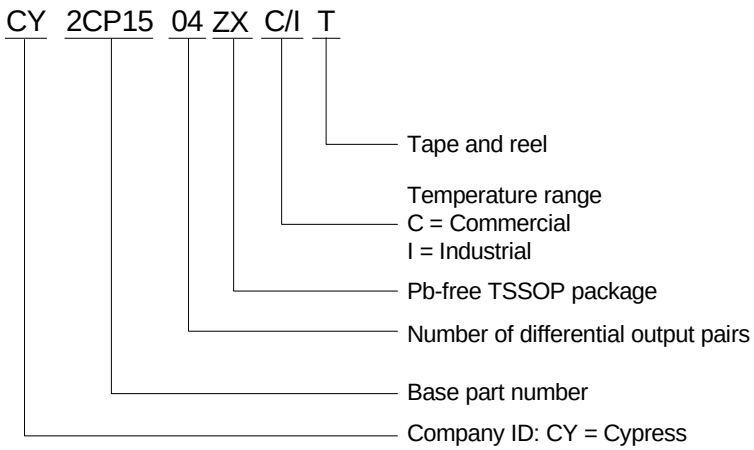

**Figure 8. Synchronous Clock Enable Timing**



## Ordering Information

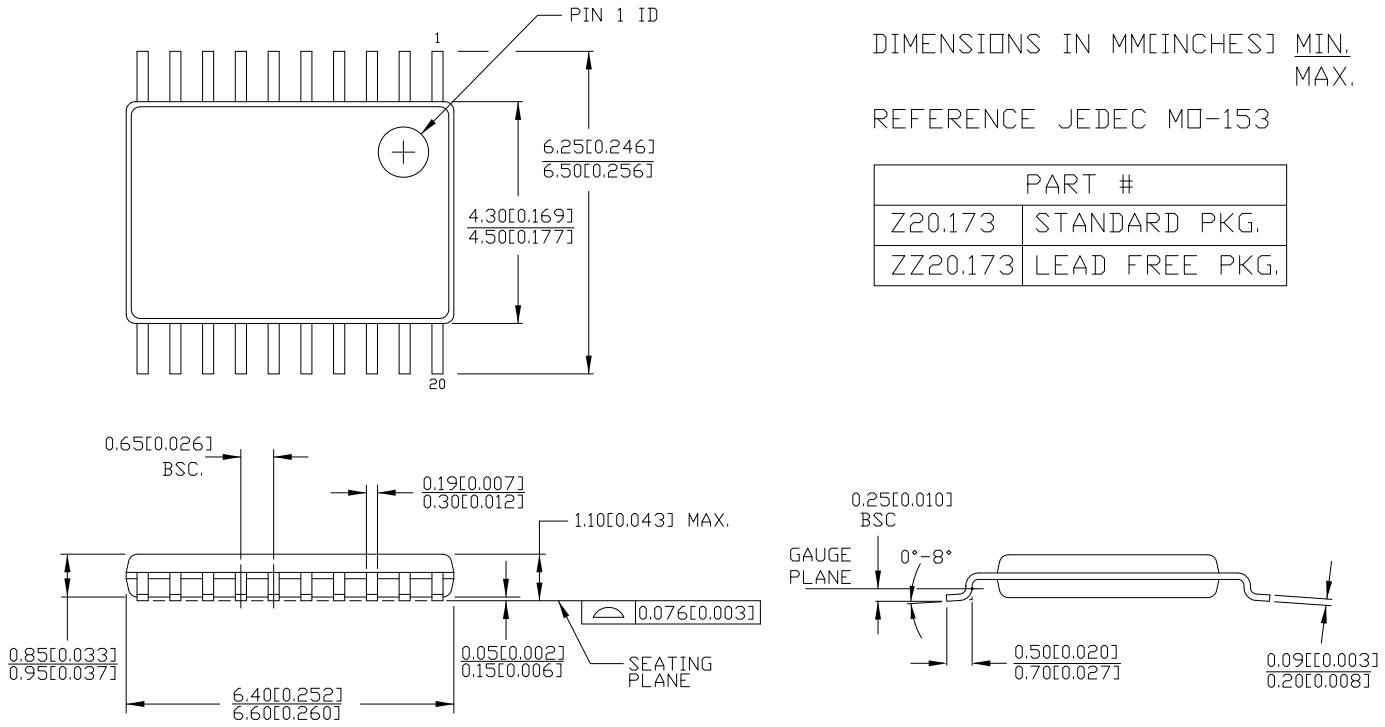
| Part Number | Type | Production Flow |
|---|---|---|
| **Pb-free** | | |
| CY2CP1504ZXC | 20-Pin TSSOP | Commercial, 0 °C to 70 °C |
| CY2CP1504ZXCT | 20-Pin TSSOP tape and reel | Commercial, 0 °C to 70 °C |
| CY2CP1504ZXI | 20-Pin TSSOP | Industrial, –40 °C to 85 °C |
| CY2CP1504ZXIT | 20-Pin TSSOP tape and reel | Industrial, –40 °C to 85 °C |

### Ordering Code Definition



## Package Dimension

**Figure 9. 20-Pin Thin Shrunk Small Outline Package (4.40-mm Body) ZZ20**




51-85118 *C

## Acronyms

**Table 2. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| ESD | electrostatic discharge |
| HBM | human body model |
| JEDEC | Joint electron devices engineering council |
| LVDS | low-voltage differential signal |
| LVCMOS | low-voltage complementary metal oxide semiconductor |
| LVPECL | low-voltage positive emitter-coupled logic |
| LVTTL | low-voltage transistor-transistor logic |
| OE | Output enable |
| RMS | root mean square |
| TSSOP | thin shrunk small outline package |

## Document Conventions

**Table 3. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| dBc | decibels relative to the carrier |
| GHz | giga hertz |
| Hz | hertz |
| kΩ | kilo ohm |
| µA | microamperes |
| µF | micro Farad |
| µs | microsecond |
| mA | milliamperes |
| ms | millisecond |
| mV | millivolt |
| MHz | megahertz |
| ns | nanosecond |
| Ω | ohm |
| pF | pico Farad |
| ps | pico second |
| V | volts |
| W | watts |

## Document History Page

| Document Title: CY2CP1504 1:4 LVCMOS to LVPECL Fanout Buffer with Selectable Clock Input<br>Document Number: 001-56313 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 2782891 | CXQ | 10/09/09 | New Datasheet |
| *A | 2838916 | CXQ | 05/01/2010 | Changed status from “ADVANCE” to “PRELIMINARY”.<br>Changed from 0.34 ps to 0.25 ps maximum additive jitter in “Features” on page 1 and in $t_{JIT}$ in the AC Electrical Specs table on page 5.<br>Added $t_{PU}$ spec to the Operating Conditions table on page 3.<br>Changed max $I_{DD}$ spec in the DC Electrical Specs table on page 4 from 60 mA to 61 mA.<br>Changed $V_{OH}$ in the DC Electrical Specs table on page 4: minimum from $V_{DD}$ - 1.15V to $V_{DD}$ - 1.20V; maximum from $V_{DD}$ - 0.75V to $V_{DD}$ - 0.70V.<br>Removed $V_{OD}$ spec from the DC Electrical Specs table on page 4.<br>Added $R_P$ spec in the DC Electrical Specs table on page 4. Min = 60 kΩ, Max = 140 kΩ.<br>Added a measurement definition for $C_{IN}$ in the DC Electrical Specs table on page 4.<br>Added $V_{PP}$ spec to the AC Electrical Specs table on page 5. $V_{PP}$ min = 600 mV for DC - 150 MHz and min = 400 mV for 150 MHz to 250 MHz.<br>Changed letter case and some names of all the timing parameters in the AC Electrical Specs table on page 5 to be consistent with EROS.<br>Lowered all additive phase noise mask specs by 3 dB in the AC Electrical Specs table on page 5.<br>Added condition to $t_R$ and $t_F$ specs in the AC Electrical specs table on page 5 that input rise/fall time must be less than 1.5 ns (20% to 80%).<br>Changed letter case and some names of all the timing parameters in Figures 2, 3, 4, 5 and 7, to be consistent with EROS. |
| *B | 3011766 | CXQ | 08/20/2010 | Changed from 0.25 ps to 0.15 ps maximum additive jitter in “Features” on page 1 and in $t_{JIT}$ in the AC Electrical Specs table on page 6.<br>Added note 2 to describe $I_{IH}$ and $I_{IL}$ specs.<br>Removed reference to data distribution from “Functional Description”.<br>Updated phase noise specs for 1 k/10 k/100 k/1 M/10 M/20 MHz offset to -120/-130/-135/-150/-150/-150dBc/Hz, respectively, in the AC Electrical Specs table.<br>Updated package diagram.<br>Added Acronyms and Ordering Code Definition. |
| *C | 3017258 | CXQ | 08/27/2010 | Corrected Output Rise/Fall time diagram. |
| *D | 3100234 | CXQ | 11/18/2010 | Changed $V_{IN}$ and $V_{OUT}$ specs from 4.0V to “lesser of 4.0 or $V_{DD}$ + 0.4”<br>Removed 200mA min LU spec, replaced with “Meets or exceeds JEDEC Spec JESD78B IC Latchup Test”<br>Changed $C_{IN}$ condition to “Measured at 10 MHz”.<br>Removed $t_R$ and $t_F$ input specs from AC specs table.<br>Changed $t_{ODC}$ from 48/52% to 45/55%, changed condition to “Rail-to-rail input swing, 50% input duty cycle measured at Vdd/2”.<br>Changed phase jitter condition to “156.25 MHz sinewave, 12 kHz to 20 MHz offset; input swing = 2.2V, $V_{bias}$ = $V_{DD}$/2 “<br>Removed $t_S$ and $t_H$ specs from AC specs table. |
| *E | 3137726 | CXQ | 01/13/2011 | Removed “Preliminary” status heading.<br>Removed resistors from IN0/IN1 in Logic Block Diagram.<br>Added Figure 8 to describe $T_{SOE}$ and $T_{SOD}$. |
| *F | 3182321 | CXQ | 02/25/11 | Post to external web. |

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