## 74C925
## 4-Digit Counters with Multiplexed
## 7-Segment Output Drivers

### General Description

These CMOS counters consist of a 4-digit counter, an internal output latch, NPN output sourcing drivers for a 7-segment display, and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free-running oscillator, and requires no external clock. The counters advance on negative edge of clock. A high signal on the Reset input will reset the counter to zero, and reset the carry-out low. A low signal on the Latch Enable input will latch the number in the counters into the internal output latches. A high signal on Display Select input will select the number in the counter to be displayed; a low level signal on the Display Select will select the number in the output latch to be displayed.
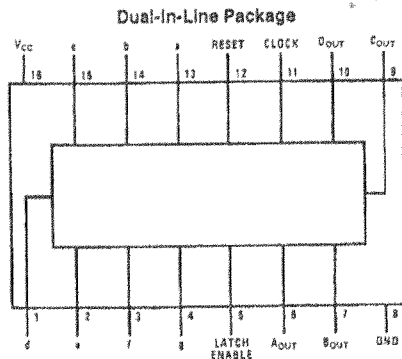
The 74C925 is a 4-decade counter and has Latch Enable, Clock and Reset inputs.

The 74C926 is like the 74C925 except that it has a display select and a carry-out used for cascading counters. The carry-out signal goes high at 6000, goes back low at 0000.
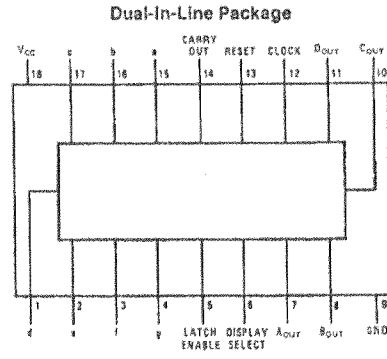
The 74C927 is like the 74C926 except the second most significant digit divides by 6 rather than 10. Thus, if the clock input frequency is 10 Hz, the display would read tenths of seconds and minutes (i.e., 9:59.9).

The 74C928 is like the 74C926 except the most significant digit divides by 2 rather than 10 and the carry-out is an overflow indicator which is high at 2000, and it goes back low only when the counter is reset. Thus, this is a 3½-digit counter.

### Connection Diagrams

#### Dual-In-Line Package
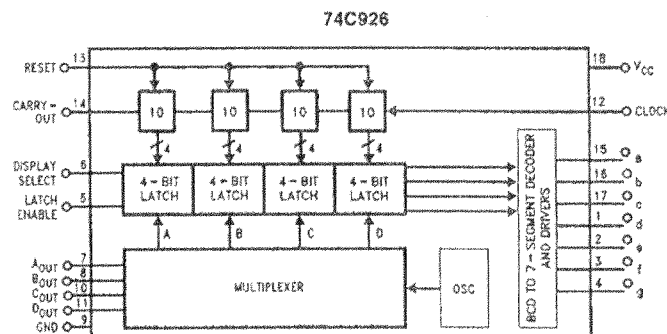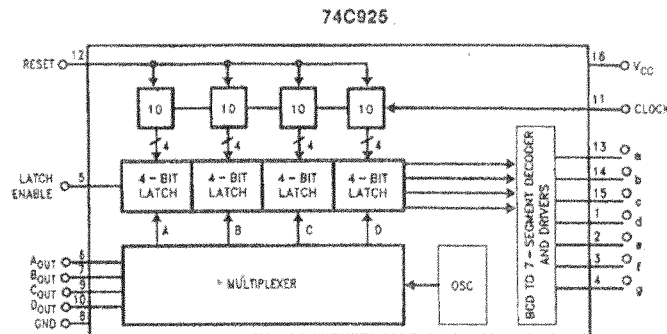


Top View
74C925

#### Dual-In-Line Package



Top View
74C926

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## Absolute Maximum Ratings (Note 1)

Voltage at Any Output Pin    GND − 0.3V to $V_{CC}$ + 0.3V
Voltage at Any Input Pin    GND − 0.3V to +15V
Operating Temperature
Range ($T_A$)    −40°C to +85°C

Storage Temperature Range    −65°C to +150°C
Power Dissipation ($P_D$)    Refer to $P_{D(MAX)}$ vs $T_A$ Graph
Operating $V_{CC}$ Range    3V to 6V
$V_{CC}$    6.5V
Lead Temperature
(Soldering, 10 seconds)    260°C

## DC Electrical Characteristics Min/Max limits apply at −40°C ≤ $T_j$ ≤ +85°C, unless otherwise noted

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CMOS TO CMOS** | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC}$ = 5V | 3.5 | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC}$ = 5V | | | 1.5 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage (Carry-Out and Digit Output Only) | $V_{CC}$ = 5V, $I_O$ = −10 μA | 4.5 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC}$ = 5V, $I_O$ = 10 μA | | | 0.5 | V |
| $I_{IN(1)}$ | Logical "1" Input Current | $V_{CC}$ = 5V, $V_{IN}$ = 15V | | 0.005 | 1 | μA |
| $I_{IN(0)}$ | Logical "0" Input Current | $V_{CC}$ = 5V, $V_{IN}$ = 0V | −1 | −0.005 | | μA |
| $I_{CC}$ | Supply Current | $V_{CC}$ = 5V, Outputs Open Circuit, $V_{IN}$ = 0V or 5V | | 20 | 1000 | μA |
| **CMOS/LPTTL INTERFACE** | | | | | | |
| $V_{IN(1)}$ | Logical "1" Input Voltage | $V_{CC}$ = 4.75V | $V_{CC}$ − 2 | | | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | $V_{CC}$ = 4.75V | | | 0.8 | V |
| $V_{OUT(1)}$ | Logical "1" Output Voltage (Carry-Out and Digit Output Only) | $V_{CC}$ = 4.75V, $I_O$ = −360 μA | 2.4 | | | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $V_{CC}$ = 4.75V, $I_O$ = 360 μA | | | 0.4 | V |

74C925



74C926



## Functional Description

Reset — Asynchronous, active high

Display Select — High, displays output of counter
Low, displays output of latch

Latch Enable — High, flow through condition
Low, latch condition

Clock — Negative edge sensitive

Segment Output — Current sourcing with 40 mA @$V_{OUT}$ = $V_{CC}$ − 1.6V (typ.) Also, sink capability = 2 LTTL loads

Digit Output — Current sourcing with 1 mA @$V_{OUT}$ = 1.75V. Also, sink capability = 2 LTTL loads

Carry-Out — 2 LTTL loads. See carry-out waveforms.