XR33152/56/58

±60V Fault Tolerant 3.0V to 5.5V TIA-485/TIA-422 Transceivers

Description

The XR33152, XR33156 and XR33158 family of high performance TIA-485/TIA-422 devices are designed for improved performance in noisy industrial environments and increased tolerance to system faults.

The analog bus pins can withstand direct shorts up to ±60V and are protected against ESD events up to ±15kV HBM. An extended ±25V common mode operating range allows for more reliable operation in noisy environments.

The receivers include full fail-safe circuitry, guaranteeing a logic high receiver output when the receiver inputs are open, shorted or undriven. The XR33152 receiver input impedance is at least 120kΩ (1/10 unit load), allowing more than 320 devices on the bus. The XR33156/58 receiver input impedance is at least 30kΩ (1/2.5 unit load), allowing more than 80 devices on the bus.

The drivers are protected by short circuit detection as well as thermal shutdown and maintain high impedance in shutdown or when powered off. The XR33152 driver is slew limited for reduced EMI and error-free communication over long or unterminated data cables.

The XR33152/56/58 family of high performance TIA-485/TIA-422 devices are designed for improved performance in noisy industrial environments and increased tolerance to system faults.

The devices with DE and $\overline{RE}$ pins include hot swap circuitry to prevent false transitions on the bus during power up or live insertion and can enter a 1nA low current shutdown mode for extreme power savings.

FEATURES

- 3.0V to 5.5V operation
- ±60V fault tolerance on analog bus pins
- Extended ±25V common mode operation
- Robust ESD protection:
  - ±15kV HBM (bus pins)
  - ± 4kV HBM (non-bus pins)
- 1.65V to 5.5V logic Interface VL pin (full-duplex package option)
- Invert control to correct for reversed bus pins
- Enhanced receiver fail-safe protection for open, shorted or terminated but idle data lines
- Hot swap glitch protection on DE and $\overline{RE}$ pins
- Driver short-circuit current limit and thermal shutdown for overload protection
- Reduced unit loads allows up to 320 devices on bus
- Industry standard 8 and 14-pin NSOIC packages
- -40°C to 85°C ambient operating temperature range

APPLICATIONS

- Industrial control networks
- HVAC networks
- Building and process automation
- Remote utility meter reading
- Energy monitoring and control
- Long or unterminated transmission lines

Typical Application

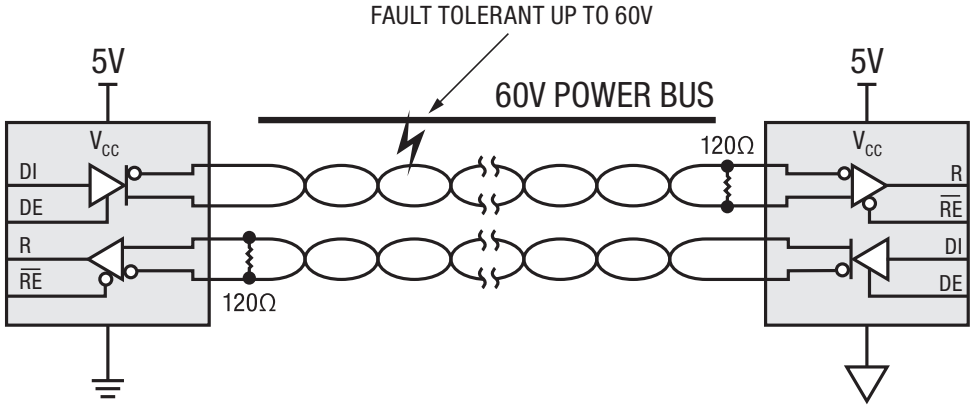


Figure 1. Typical Application

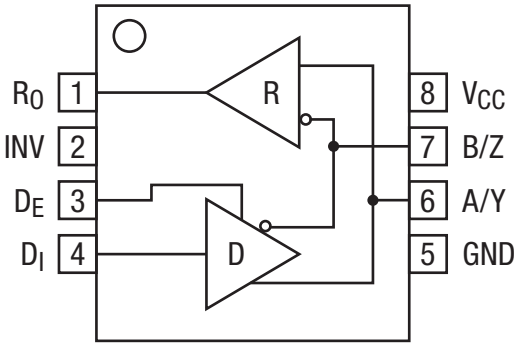
Absolute Maximum Ratings

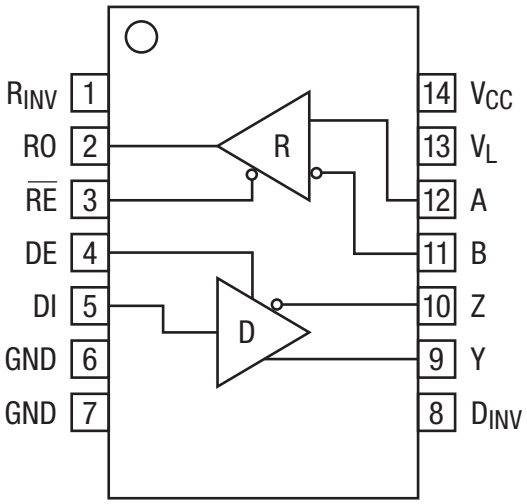
These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections to the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

V_{CC}	-0.3V to 7.0V
V_L	$V_L \le V_{CC}$
Input voltage at control and driver input (DE, DI and INV) XR33152/58	-0.3V to (V_{CC} + 0.3V)
Receiver output voltage (RO) XR33152/58	-0.3V to (V_{CC} + 0.3V)
Input voltage at control ($\overline{RE}$) XR33156	-0.3V to (V_L + 0.3V)
Input voltage at control and driver input (DE, DI, R_{INV}, D_{INV}, and INV) XR33156	-0.3V to 7.0V
Receiver output voltage (RO) XR33156	-0.3V to (V_L + 0.3V)
Driver output voltage (A, B, Y and Z)	±60V
Receiver input voltage (A and B, half or full duplex)	±60V
Transient voltage pulse, through 100Ω (Figure 7)	±100V
Driver output current	±250mA
Storage temperature range	-65°C to 150°C
Lead temperature (soldering, 10s)	300°C
Package power dissipation 8-pin NSOIC θ_{JA} = 128.4°C/W 14-pin NSOIC θ_{JA} = 86°C/W	Maximum junction temperature = 150°C

CAUTION:
ESD-sensitive (electrostatic discharge) device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. Personnel should be properly grounded prior to handling this device. The protective foam should be discharged to the destination socket before devices are removed.

Pin Configuration





Pin Functions

Half Duplex	Full Duplex	Pin Name	Type	Pin Function
XR33152	XR33156			
XR33158				
Pin Number				
-	1	R_{INV}	In	Receiver invert control (active high). When enabled, the polarity of the receiver bus pins (A & B) is reversed: A = inverting and B = non-inverting. When disabled, the receiver bus pins (A & B) operate normally: A = non-inverting and B = inverting. The R_{INV} pin has a 150KΩ pull-down resistor.
1	2	RO	Out	Receiver output, when $\overline{RE}$ is low and if (A-B) ≥ 200mV, RO is high. If (A-B) ≤ -200mV, RO is low If inputs are left floating, shorted together or terminated and undriven for more than 2µs the output is high.
2	-	INV	In	Driver and receiver invert control (active high). When enabled, the polarity of the driver input and receiver input bus pins is inverted. When disabled, the driver input and receiver inputs operate normally: A = non-inverting and B = inverting. The INV pin has a 150kΩ pull-down resistor.
-	3	$\overline{RE}$	In	Receiver output enable (hot swap). When $\overline{RE}$ is low, RO is enabled. When $\overline{RE}$ is high, RO is high impedance. $\overline{RE}$ should be high and DE should be low to enter shutdown mode.
3	4	DE	In	Driver output enable (hot swap). When DE is high, outputs are enabled. When DE is low, outputs are high impedance. DE should be low and $\overline{RE}$ should be high to enter shutdown mode.
4	5	DI	In	Driver input. With DE high, a low level on DI forces non-inverting output low and inverting output high. Similarly, a high level on DI forces non-inverting output high and inverting output low.
5	6, 7	GND	Power	Ground.
6	-	A/Y	I/O	Non-inverting receiver input and non-Inverting driver output.
7	-	B/Z	I/O	Inverting receiver input and Inverting driver output.

Pin Functions

Half Duplex	Full Duplex	Pin Name	Type	Pin Function
XR33152	XR33156			
XR33158				
Pin Number				
8	14	V_{CC}	Power	3.0V to 5.5V power supply input bypass to ground with 0.1µF capacitor.
-	12	A	In	Non inverting receiver input.
-	11	B	In	Inverting receiver input.
-	9	Y	Out	Non-inverting driver output.
-	10	Z	Out	Inverting driver output.
-	8	D_{INV}	In	Driver invert control (active high). When enabled, the polarity of the driver input pin is inverted causing the driver output (Y & Z) polarities to be inverted. When disabled, the driver bus pins (Y & Z) operate normally: Y = non-inverting and Z = inverting. The D_{INV} pin has a 150kΩ pull-down resistor.
-	13	V_L	Power	Logic interface power supply.

Pin Functions

XR33156 (Full Duplex - 14 Pins)

Transmitting					
Inputs				Outputs	
D_{INV}	$\overline{RE}$	DE	DI	Y	Z
0	X	1	1	1	0
0	X	1	0	0	1
1	X	1	1	0	1
1	X	1	0	1	0
X	0	0	X	High-Z	
X	1	0	X	High-Z (shutdown)	

XR33156 (Full Duplex - 14 Pins)

Receiving				
Inputs				Output
R_{INV}	$\overline{RE}$	DE	V_A - V_B	RO
0	0	X	≥ 200mV	1
0	0	X	≤ -200mV	0
0	0	X	Open/shorted	1
1	0	X	≥ 200mV	0
1	0	X	≤ -200mV	1
1	0	X	Open/shorted	1
X	1	1	X	High-Z
X	1	0	X	High-Z (shutdown)

XR33152 and XR33158 (Half Duplex - 8 Pins)

Transmitting				
Inputs			Outputs	
INV	DE	DI	A/Y	B/Z
0	1	1	1	0
0	1	0	0	1
1	1	1	0	1
1	1	0	1	0
X	0	X	High-Z	

XR33152 and XR33158 (Half Duplex - 8 Pins)

Receiving			
Inputs			Output
INV	DE	V_A - V_B	RO
0	0	≥ 200mV	1
0	0	≤ -200mV	0
1	0	Open/shorted	1
1	0	≥ +200mV	0
1	0	≤ -200mV	1
1	0	Open/shorted	1

Electrical Characteristics

Unless otherwise noted: V_{CC} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
		Driver DC Characteristics				
V_{CC}	Supply voltage range		3.0		5.5	V
V_L	I/O logic supply voltage range	$V_L \le V_{CC}$	1.65		5.5	V
V_{OD}	Differential driver output, 4.5V ≤ V_{CC} ≤ 5.5V	R_L = 100Ω (TIA-422), Figure 4	2		V_{CC}	V
		R_L = 54Ω (TIA-485), Figure 4	1.5		V_{CC}	V
		-25V ≤ V_{CM} ≤ 25V, Figure 5	1.5		V_{CC}	V
V_{OD}	Differential driver output, 3.0V ≤ V_{CC} ≤ 4.5V	R_L = 100Ω (TIA-422), Figure 4	0.85		V_{CC}	V
		R_L = 54Ω (TIA-485), Figure 4	0.65		V_{CC}	V
ΔV_{OD}	Change in magnitude of differential output voltage, Note 1	RL = 100Ω (TIA-422) or RL = 54Ω (TIA-485), Figure 4			±0.2	V
V_{CM}	Driver common-mode output voltage (steady state)		1		3	V
ΔV_{CM}	Change in magnitude of common-mode output voltage, Note 1				±0.2	V
V_{IH}	Logic high input thresholds (DI, DE and INV)	V_{CC} = 3.3V, for XR33152/58	2.0			V
		V_{CC} = 5.0V, for XR33152/58	2.4			V
V_{IL}	Logic low input thresholds (DI, DE and INV)	For XR33152/58			0.8	V
V_{IH}	Logic high input thresholds (DI, DE, $\overline{RE}$, D_{INV} and R_{INV})	$V_L \le V_{CC}$, for XR33156	(2/3)V_L			V
V_{IL}	Logic low input thresholds (DI, DE, $\overline{RE}$, D_{INV} and R_{INV})	$V_L \le V_{CC}$, for XR33156			(1/3)V_L	V
V_{HYS}	Input hysteresis (DI, DE, $\overline{RE}$, D_{INV}, R_{INV} and INV)			100		mV
I_{IN}	Logic input current (DI, DE and $\overline{RE}$)	0V ≤ V_{IN} ≤ V_{CC}, for XR33152/58 After first transition, Note 2			±1	µA
	Logic input current (INV)	V_{IN} = V_{CC} = 5.5V, for XR33152/58	25	33	55	µA
	Logic input current (DI, DE and $\overline{RE}$)	0V ≤ V_{IN} ≤ V_L = V_{CC} = 5.5V, for XR33156 After first transition, Note 2			±1	µA
	Logic input current (D_{INV} and R_{INV})	V_{IN} = V_L = V_{CC} = 5.5V, for XR33156	25	33	55	µA
I_{INHS}	Logic input current hot swap (DE and $\overline{RE}$)	Until first transition, Note 2		100	±200	µA
$I_{A, B}$	Input current (A and B)	V_{CC} = 0V or 5.5V, V_{OUT} = 12V, DE = 0V, for XR33152			100	µA
		V_{CC} = 0V or 5.5V, V_{OUT} = -7V, DE = 0V, for XR33152	-80			µA
		V_{OUT} = 12V, DE = 0V, V_{CC} = 0V or 5.5V, for XR33156/58			400	µA
		V_{OUT} = -7V, DE = 0V, V_{CC} = 0V or 5.5V, for XR33156/58	-320			µA

NOTES:

1. Change in magnitude of differential output voltage and change in magnitude of common mode output voltage are the changes in output voltage when DI input changes state.
2. The hot swap feature disables the DE and $\overline{RE}$ inputs for the first 10µs after power is applied. Following this time period, these inputs are weakly pulled to their disabled state (low for DE, high for $\overline{RE}$) until the first transition, after which they become high impedance inputs.

Electrical Characteristics

Unless otherwise noted: V_{CC} = 3.0V to 5.5V, T_A = T_{MIN} to T_{MAX}. Typical values are at V_{CC} = 5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{OL}	Output leakage (Y and Z) Full duplex	V_{OUT} = 12V, DE = 0V, V_{CC} = 0V or 5.5V			100	µA
		V_{OUT} = -7V, DE = 0V, V_{CC} = 0V or 5.5V	-80			µA
I_{OSD}	Driver short-circuit output current	-60V ≤ V_{OUT} ≤ 60V, Figure 6			±250	µA
Driver Thermal Characteristics						
T_{TS}	Thermal shutdown temperature	Junction temperature, Note 1		175		°C
T_{TSH}	Thermal shutdown hysteresis	Note 1		15		°C
Receiver DC Characteristics						
V_{STH}	Receiver differential input signal threshold voltage (V_A - V_B)	-25V ≤ V_{OUT} ≤ 25V		±85	±200	mV
ΔV_{STH}	Receiver differential input signal hysteresis			170		mV
V_{FSTH-}	Negative going receiver differential input failsafe threshold voltage (V_A - V_B)	-25V ≤ V_{OUT} ≤ 25V	-200	-125	-40	mV
V_{FSTH+}	Positive going receiver differential input failsafe threshold voltage (V_A - V_B)	-25V ≤ V_{OUT} ≤ 25V		-100	-10	mV
ΔV_{FSTH}	Receiver differential input failsafe hysteresis			25		mV
V_{OH}	Receiver output high voltage (RO)	I_{OUT} = -4mA, for XR33152/58	V_{CC} - 0.6			V
V_{OL}	Receiver output low voltage (RO)	I_{OUT} = 4mA, for XR33152/58			0.4	V
V_{OH}	Receiver output high voltage (RO)	3.0V ≤ V_L ≤ 5.5V, I_{OUT} = -4mA, 1.6V ≤ V_L ≤ 3.0V, I_{OUT} = -1mA, for XR33156	V_L - 0.6			V
V_{OL}	Receiver output low voltage (RO)	3.0V ≤ V_L ≤ 5.5V, I_{OUT} = 4mA, 1.6V ≤ V_L ≤ 3.0V, I_{OUT} = 1mA, for XR33156			0.4	V
I_{OZR}	High-Z receiver output current	0V ≤ V_{OUT} ≤ V_{CC}, for XR33152/58 0V ≤ V_{OUT} ≤ V_L, for XR33156			±1	µA
R_{IN}	RX input resistance	-25V ≤ V_{CM} ≤ 25V, for XR33152	120			kΩ
		-25V ≤ V_{CM} ≤ 25V, for XR33156/58	30			kΩ
I_{OSC}	RX output short-circuit current	0V ≤ V_{RO} ≤ V_{CC}, for XR33152/58			110	mA
	RX output short-circuit current	0V ≤ V_{RO} ≤ V_L, for XR33156			110	mA
Supply Current						
I_{CC}	Supply current	No load, $\overline{RE}$ = 0V or V_{CC}, DE = V_{CC}, DI = 0V or V_{CC}			4	mA
I_{SHDN}	Supply current in shutdown mode	$\overline{RE}$ = V_{CC}, DE = 0V		0.001	1	µA
ESD Protection						
	ESD protection for A, B, Y, and Z	Human body model		±15		kV
	ESD protection for all other pins	Human body model		±4		kV

NOTES:
1. This spec is guaranteed by design and bench characterization.

Electrical Characteristics

Driver AC Characteristics - XR33152 (250kbps)

Unless otherwise noted: V_{CC} = 3.0V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}. Typical values are at V_{CC} = 5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DPLH}	Driver prop. delay (low to high)	C_L = 50pF, R_L = 54Ω, Figure 8	350		1500	ns
t_{DPHL}	Driver prop. delay (high to low)		350		1600	ns
$\lvert t_{DPLH}-t_{DPHL}\rvert$	Differential driver output skew			20	200	ns
t_{DR}, t_{DF}	Driver differential output rise or fall time		400		1500	ns
	Maximum data rate	$1/t_{UI}$, duty cycle 40% to 60%	250			kbps
t_{DZH}	Driver enable to output high	C_L = 50pF, R_L = 500Ω, Figure 9		200	2500	ns
t_{DZL}	Driver enable to output low			200	2500	ns
t_{DHZ}	Driver disable from output high				250	ns
t_{DLZ}	Driver disable from output low				250	ns
$t_{RZH(SHDN)}$	Driver enable from shutdown to output high	C_L = 50pF, R_L = 500Ω, Figure 9			5500	ns
$t_{RZL(SHDN)}$	Driver enable from shutdown to output low				5500	ns
t_{SHDN}	Time to shutdown	Notes 1 and 2	50	200	600	ns

Receiver AC Characteristics - XR33152 (250kbps)

Unless otherwise noted: V_{CC} = 3.0V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}. Typical values are at V_{CC} = 5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{RPLH}	Receiver prop. delay (low to high)	C_L = 15pF, V_{ID} = ±2V, V_{ID} rise and fall times < 15ns, Figure 10			200	ns
t_{RPHL}	Receiver prop. delay (high to low)				200	ns
$\lvert t_{RPLH}-t_{RPHL}\rvert$	Receiver propagation delay skew				30	ns
	Maximum data rate	$1/t_{UI}$, duty cycle 40% to 60%	250			kbps

NOTES:

1. The transceivers are put into shutdown by bringing $\overline{RE}$ high and DE low simultaneously for at least 600ns. If the control inputs are in this state for less than 50ns, the device is guaranteed to not enter shutdown. If the enable inputs are held in this state for at least 600ns, the device is ensured to be in shutdown. Note that the receiver and driver enable times increase significantly when coming out of shutdown.
2. This spec is guaranteed by design and bench characterization.

Electrical Characteristics

Driver AC Characteristics - XR33156 and XR33158 (20Mbps)

Unless otherwise noted: V_{CC} = 3.0V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}. Typical values are at V_{CC} = 5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{DPLH}	Driver prop. delay (low to high)	C_L = 50pF, R_L = 54Ω, Figure 8			25	ns
t_{DPHL}	Driver prop. delay (high to low)				25	ns
$\lvert t_{DPLH}-t_{DPHL}\rvert$	Differential driver output skew				5	ns
t_{DR}, t_{DF}	Driver differential output rise or fall time				15	ns
	Maximum data rate	$1/t_{UI}$, duty cycle 40% to 60%	20			Mbps
t_{DZH}	Driver enable to output high	C_L = 50pF, R_L = 500Ω, Figure 9			60	ns
t_{DZL}	Driver enable to output low				60	ns
t_{DHZ}	Driver disable from output high				250	ns
t_{DLZ}	Driver disable from output low				250	ns
$t_{DZH(SHDN)}$	Driver enable from shutdown to output high	C_L = 50pF, R_L = 500Ω, Figure 9			2200	ns
$t_{DZL(SHDN)}$	Driver enable from shutdown to output low				2200	ns
t_{SHDN}	Time to shutdown	Notes 1 and 2	50	200	600	ns

Receiver AC Characteristics - XR33156 and XR33158 (20Mbps)

Unless otherwise noted: V_{CC} = 3.0V to 5.5V, $T_A = T_{MIN}$ to T_{MAX}. Typical values are at V_{CC} = 5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{RPLH}	Receiver prop. delay (low to high)	C_L = 15pF, V_{ID} = ±2V, V_{ID} rise and fall times < 15ns, Figure 10			60	ns
t_{RPHL}	Receiver prop. delay (high to low)				60	ns
$\lvert t_{RPLH}-t_{RPHL}\rvert$	Receiver propagation delay skew				5	ns
	Maximum data rate	$1/t_{UI}$, duty cycle 40% to 60%	20			Mbps
t_{RZH}	Receiver enable to output high	C_L = 15pF, R_L = 1kΩ, Figure 11, for XR33156			50	ns
t_{RZL}	Receiver enable to output low				50	ns
t_{RHZ}	Receiver disable from output high				50	ns
t_{RLZ}	Receiver disable from output low				50	ns
$t_{RZH(SHDN)}$	Receiver enable from shutdown to output high	C_L = 15pF, R_L = 1kΩ, Figure 11, for XR33156			2200	ns
$t_{RZL(SHDN)}$	Receiver enable from shutdown to output low				2200	ns
t_{SHDN}	Time to shutdown	Notes 1 and 2, for XR33156	50	200	600	ns

NOTES:

1. The transceivers are put into shutdown by bringing $\overline{RE}$ high and DE low simultaneously for at least 600ns. If the control inputs are in this state for less than 50ns, the device is guaranteed to not enter shutdown. If the enable inputs are held in this state for at least 600ns, the device is ensured to be in shutdown. Note that the receiver and driver enable times increase significantly when coming out of shutdown.
2. This spec is guaranteed by design and bench characterization.

Applications Information

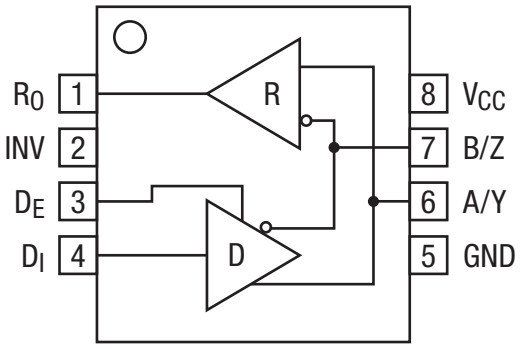


Figure 2. Half Duplex (XR33152, and XR33158)

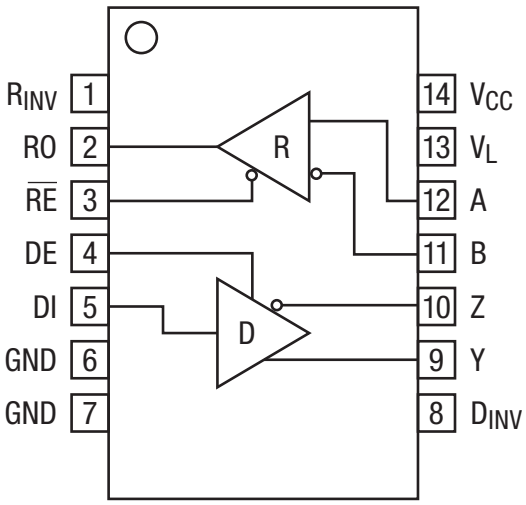


Figure 3. Full Duplex (XR33156)

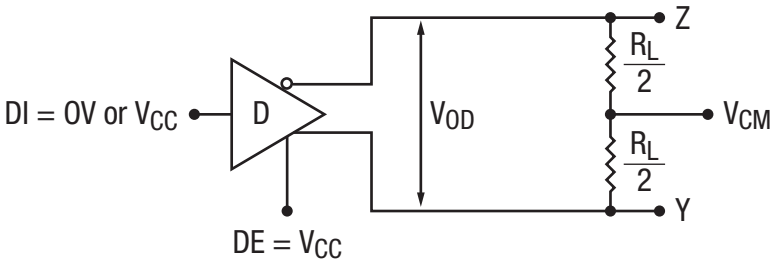


Figure 4. Differential Driver Output Voltage

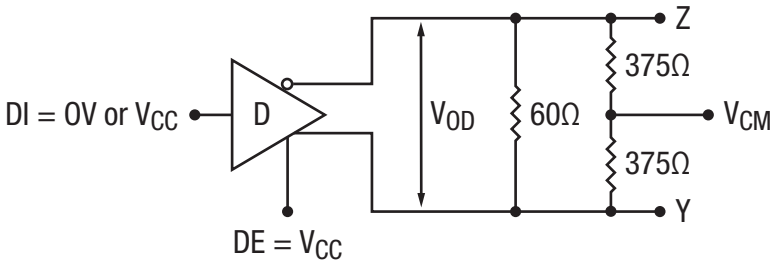


Figure 5. Differential Driver Output Voltage Over Common Mode

Applications Information

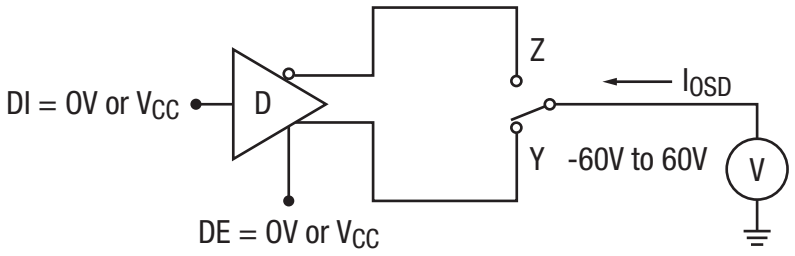


Figure 6. Driver Output Short Circuit Current

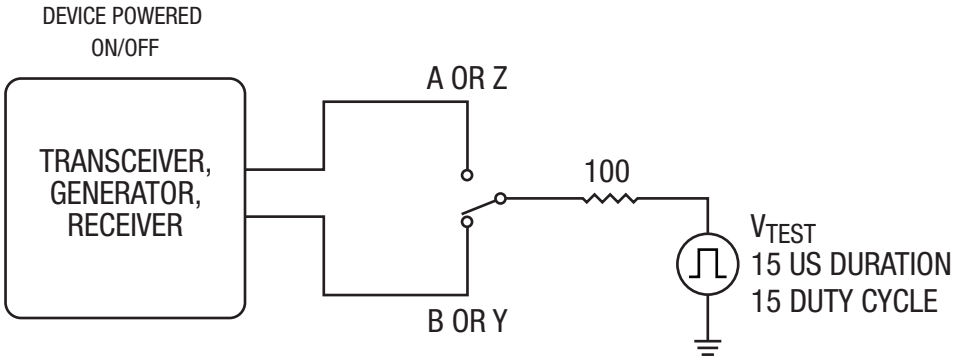


Figure 7. Transient Overvoltage Test Circuit

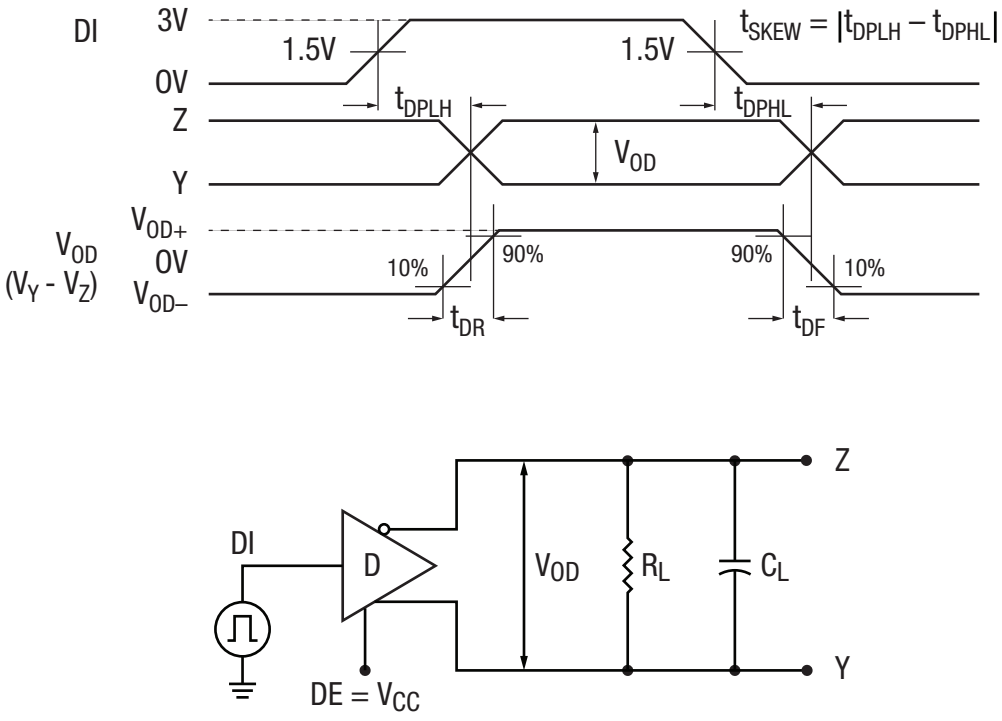


Figure 8. Driver Propagation Delay Test Circuit and Timing Diagram

Applications Information

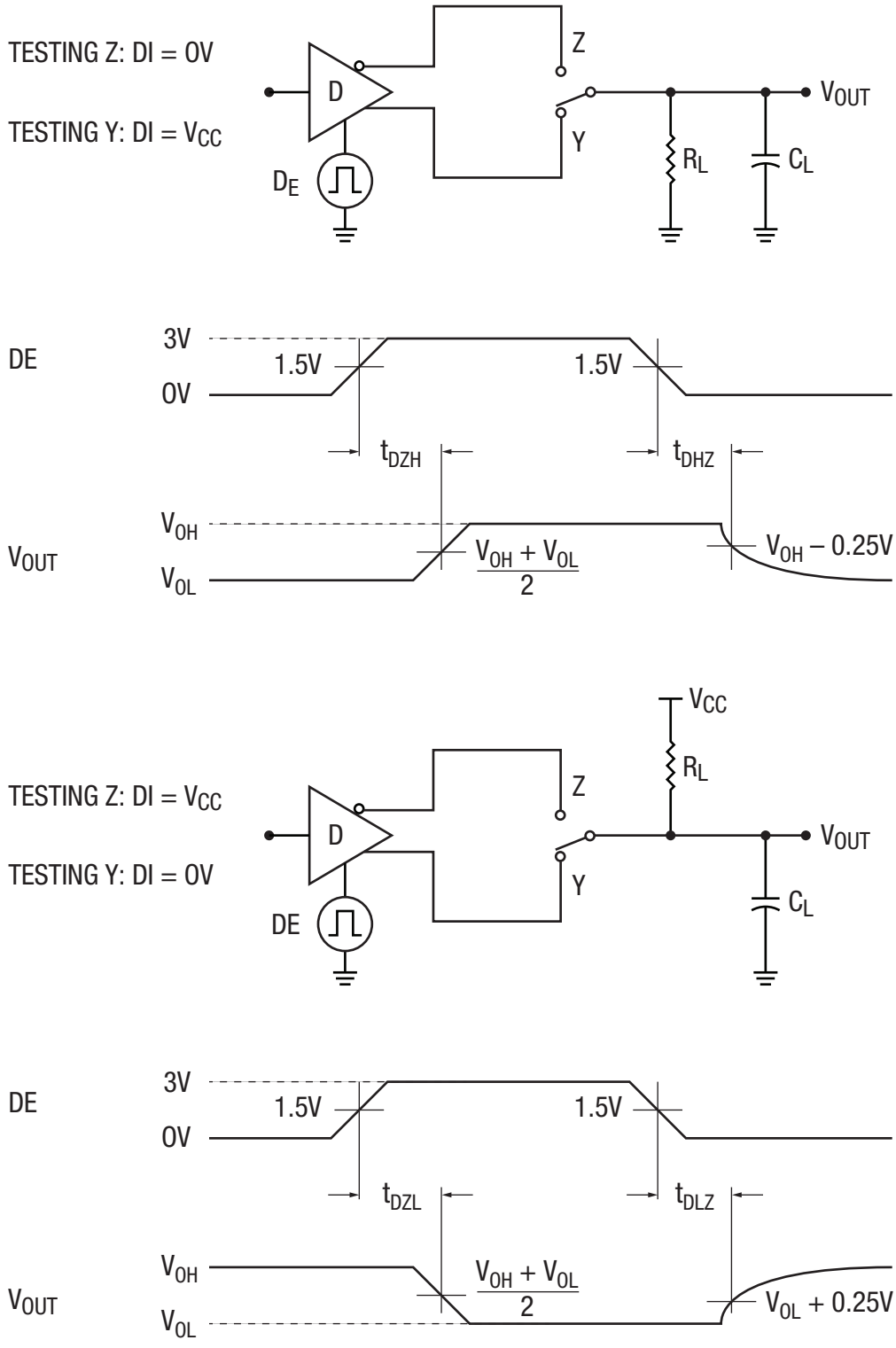


Figure 9. Driver Enable and Disable Timing Test Circuits and Timing Diagrams

Applications Information

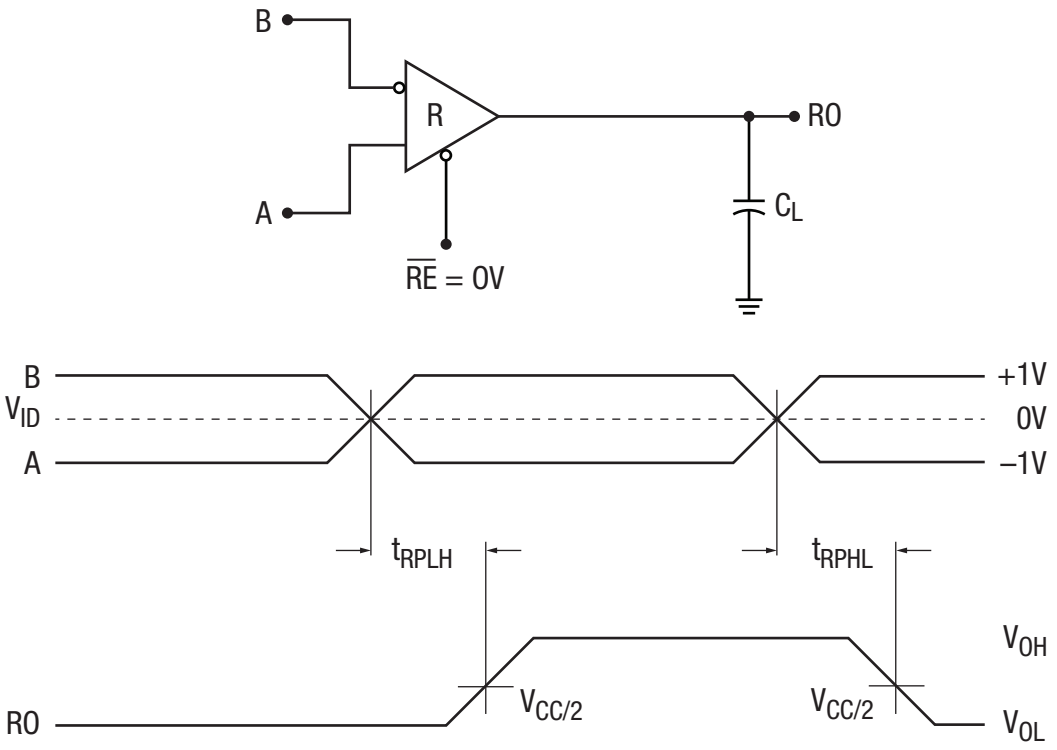


Figure 10. Receiver Propagation Delay Test Circuit and Timing Diagram

Applications Information

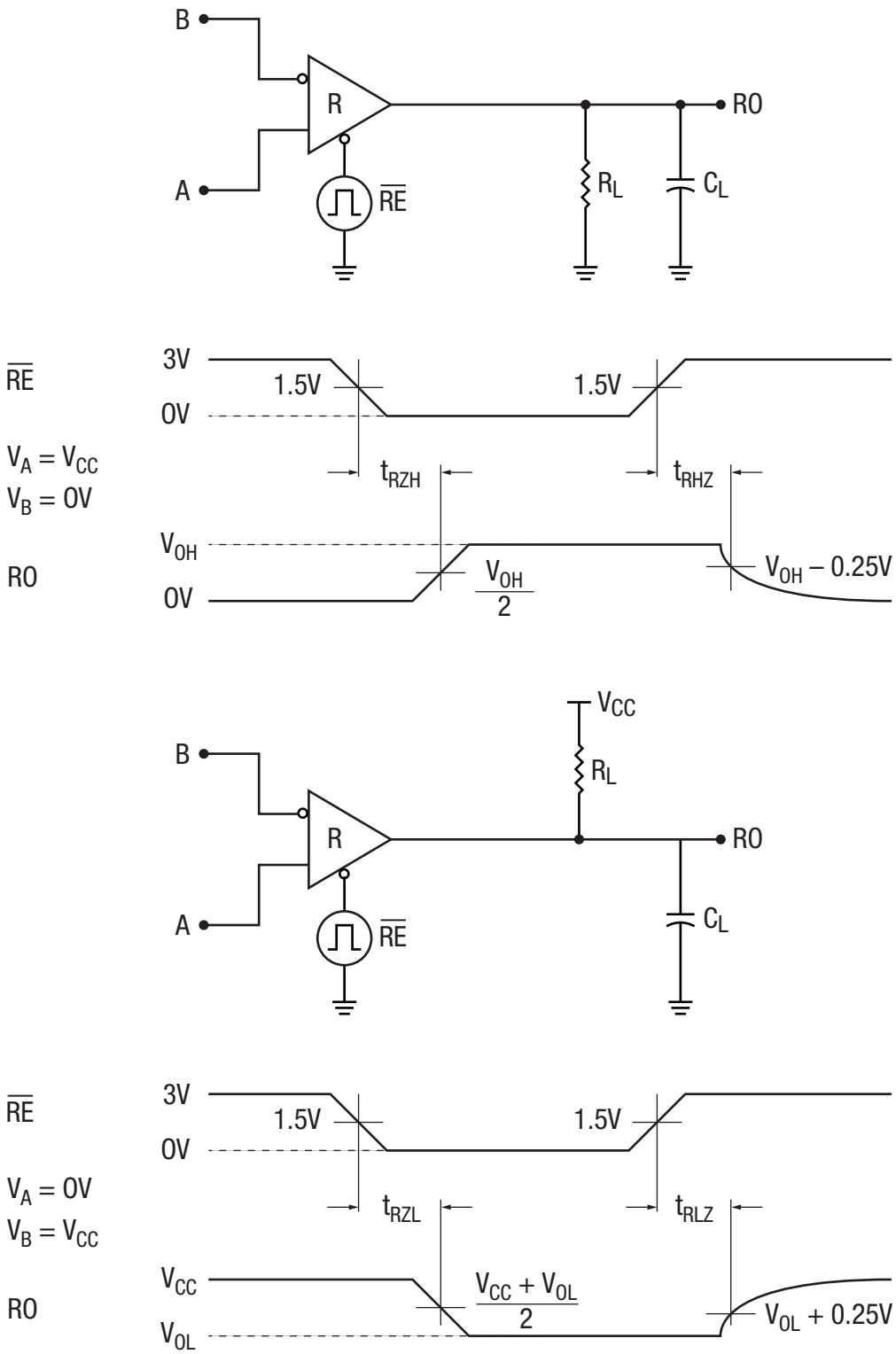


Figure 11. Receiver Enable and Disable Test Circuits and Timing Diagrams

Applications Information

The XR33152/56/58 TIA-485/TIA-422 devices are part of Exar's high performance serial interface product line. The analog bus pins can survive direct shorts up to ±60V and are protected against ESD events up to ±15kV.

Enhanced Failsafe

Ordinary TIA-485 differential receivers will be in an indeterminate state whenever the data bus is not being actively driven. The enhanced failsafe feature of the XR33152/56/58 family guarantees a logic-high receiver output when the receiver inputs are open, shorted or when they are connected to a terminated transmission line with all drivers disabled. In a terminated bus with all transmitters disabled, the receivers' differential input voltage is pulled to 0V by the termination. The XR33152/56/58 family interprets 0V differential as a logic high with a minimum 50mV noise margin while maintaining compliance with the TIA-485 standard of ±200mV. Although the XR33152/56/58 family does not need failsafe biasing resistors, it can operate without issue if biasing is used.

Receiver Input Filtering

The XR33152 receivers incorporate internal filtering in addition to input hysteresis. This filtering enhances noise immunity by ignoring signals that do not meet a minimum pulse width of 30ns. Receiver propagation delay increases slightly due to this filtering. The high speed XR33156 and XR33158 devices do not have this input filtering.

Hot Swap Capability

When V_{CC} is first applied the XR33152/56/58 family holds the driver enable and receiver enable inactive for approximately 10µs. During power ramp-up, other system ICs may drive unpredictable values or tristated lines may be influenced by stray capacitance. The hot swap feature prevents the XR33152/56/58 family from driving any output signal until power has stabilized. After the initial 10µs, the driver and receiver enable pins are weakly pulled to their disabled states (low for DE and high for $\overline{RE}$) until the first transition. After the first transition, the DE and $\overline{RE}$ pins operate as high impedance inputs.

If circuit boards are inserted into an energized backplane (commonly called "live insertion" or "hot swap") power may suddenly be applied to all circuits. Without the hot swap capability, this situation could improperly enable the transceiver's driver or receiver, driving invalid data onto shared buses and possibly causing driver contention or device damage.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. First, a driver current limit on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. Second, a thermal shutdown circuit forces the driver outputs into a high impedance state if junction temperature becomes excessive.

Line Length

The TIA-485/TIA-422 standard covers line lengths up to 4000ft. Maximum achievable line length is a function of signal attenuation and noise. Termination prevents signal reflections by eliminating the impedance mismatches on a transmission line. Line termination is generally used if rise and fall times are shorter than the round trip signal propagation time. Higher output drivers may allow longer cables to be used.

±15kV ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver outputs and receiver inputs of the XR33152/56/58 family has extra protection against static electricity. Exar uses state-of-the-art structures to protect these pins against ESD of ±15kV without damage. The ESD structures withstand high ESD in all states: normal operation, shutdown and powered down. After an ESD event, the XR33152/56/58 keep operating without latch up or damage.

ESD protection can be tested in various ways. The transmitter outputs and receiver inputs of the XR33152/56/58 are characterized for protection to the following limits:

- ±15kV using the Human Body Model, TIA-485 bus pins
- ±4kV using the Human Body Model, all other pins

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Exar for a reliability report that documents test setup, methodology and results.

Maximum Number of Transceivers on the Bus

The standard TIA-485 receiver input impedance is 12kΩ (1 unit load). A standard driver can drive up to 32 unit loads. The XR33152 transceiver has a 1/10th unit load receiver input impedance of 120kΩ, allowing up to 320 transceivers to be connected in parallel on a communication line. The XR33156/58 transceivers have a 1/2.5 unit load receiver input impedance of 30kΩ, allowing up to 80 transceivers to be connected in parallel on a communication line. Any combination of these devices and other TIA-485 transceivers up to a total of 32 unit loads may be connected to the line.

Applications Information

Low Power Shutdown Mode

The XR33156 has a low-power shutdown mode that is initiated by bringing both $\overline{RE}$ high and DE low simultaneously. While in shutdown the XR33156 draws less than 1µA of supply current. DE and $\overline{RE}$ may be tied together and driven by a single control signal. Devices are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts will enter shutdown.

XR33156 enable times, t_{ZH} and t_{ZL}, apply when the part is not in low power shutdown state. Enable times, $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ apply when the part is shutdown. The driver and receiver take longer to become enabled from low power shutdown $t_{ZH(SHDN)}$ and $t_{ZL(SHDN)}$ than from driver or receiver disable mode (t_{ZH} and t_{ZL}).

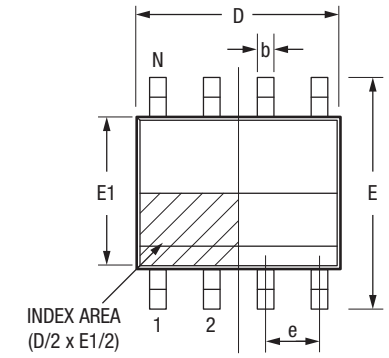
Product Selector Guide

Part Number	Operation	Data Rate	Shutdown	Receiver/Driver Enable	Nodes On Bus	Footprint
XR33152	Half duplex	250kbps	No	No/Yes	320	8-NSOIC
XR33156	Full duplex	20Mbps	Yes	Yes/Yes	80	14-NSOIC
XR33158	Half duplex		No	No/Yes	80	8-NSOIC

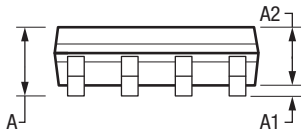
Package Description

8-Pin NSOIC Package

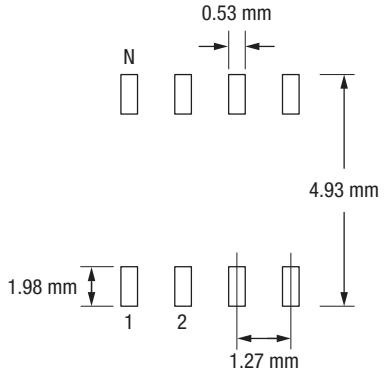
TOP VIEW



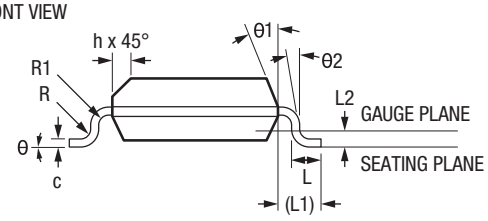
SIDE VIEW



RECOMMENDED PCB LAND PATTERN



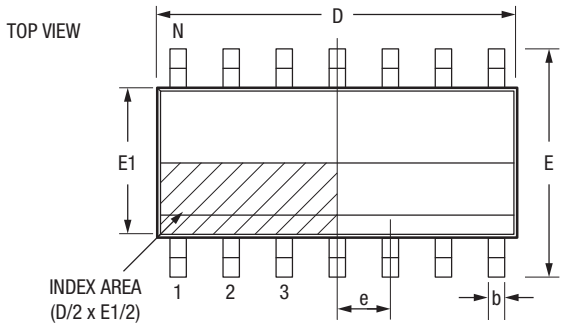
FRONT VIEW

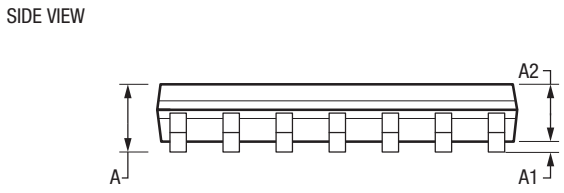


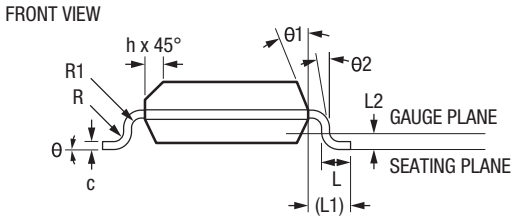
8-Pin NSOIC (JEDEC MS-012)						
Symbols	Dimension in mm (Control unit)			Dimension in inches (Reference unit)		
	Min	Nom	Max	Min	Nom	Max
A	1.35	-	1.75	0.053	-	0.069
A1	0.10	-	0.25	0.004	-	0.010
A2	1.25	-	1.65	0.049	-	0.065
b	0.31	-	0.51	0.012	-	0.020
c	0.17	-	0.25	0.007	-	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	-	0.50	0.010	-	0.020
L	0.40	-	1.27	0.016	-	0.050
L1	1.04 Ref			0.041 Ref		
L2	0.25 BSC			0.010 BSC		
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
θ	0°	-	8°	0°	-	8°
θ1	5°	-	15°	5°	-	15°
θ2	0°	-	-	0°	-	-
D	4.90 BSC			0.193 BSC		
N	8			8		

Package Description

14-Pin NSOIC Package







14-Pin NSOIC (JEDEC MS-012)						
Symbols	Dimension in mm (Control unit)			Dimension in inches (Reference unit)		
	Min	Nom	Max	Min	Nom	Max
A	1.35	-	1.75	0.053	-	0.069
A1	0.10	-	0.25	0.004	-	0.010
A2	1.25	-	1.65	0.049	-	0.065
b	0.31	-	0.51	0.012	-	0.020
c	0.17	-	0.25	0.007	-	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	-	0.50	0.010	-	0.020
L	0.40	-	1.27	0.016	-	0.050
L1	1.04 Ref			0.041 Ref		
L2	0.25 BSC			0.010 BSC		
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
θ	0°	-	8°	0°	-	8°
θ1	5°	-	15°	5°	-	15°
θ2	0°	-	-	0°	-	-
D	8.65 BSC			0.341 BSC		
N	14			14		

Order Information

Part Number	Operation	Data Rate	Package	Environmental Rating	Operating Temperature Range
XR33152ID-F	Half duplex	250kbps	8-pin SOIC	Green/RoHS	-40°C to 85°C
XR33152IDTR-F					
XR33156ID-F	Full duplex	20Mbps	14-pin SOIC		
XR33156IDTR-F					
XR33158ID-F	Half duplex		8-pin SOIC		
XR33158IDTR-F					

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