BL6810

Power Line Communication

Microcontroller

Datasheet

Catalog

1 Overview

The BL6810 is a fully integrated narrow-band power line communication chip. It supports four channels' BPSK/DSSS modulation/demodulation and has multi-frequency, multi-rate features, supports adaptive signal receiving. The BL6810 integrated 51mcu core and compatible with EIA709.2 and DL/T-645, can be used in low-voltage power line carrier automatic meter reading (AMR), smart home control, remote streetlight monitoring, industrial control and other applications.

1.1   BL6810 Features

- Operating Voltage：5V
- Integrated 8051 core, compatible with the 8051 instruction set and bus structure
- Modulation mode: BPSK/DSSS
- Three communication rates: 5.48k/365bps(DSSS15)/87bps(DSSS63) adaptive receiving
- Four channels: 131.58k/263.16k/312.5k/416.67kHz adaptive receiving
- Support phase detection
- On-chip analog band pass filter
- On-chip high-performance digital narrowband filter
- On-chip 66dB low noise AGC
- On-chip RS hardware codec, with forward error correction capabilities
- Hardware CRC16
- Received signal strength indication, SNR indication, support for routing algorithm

1.2   BL6810 Block Diagram
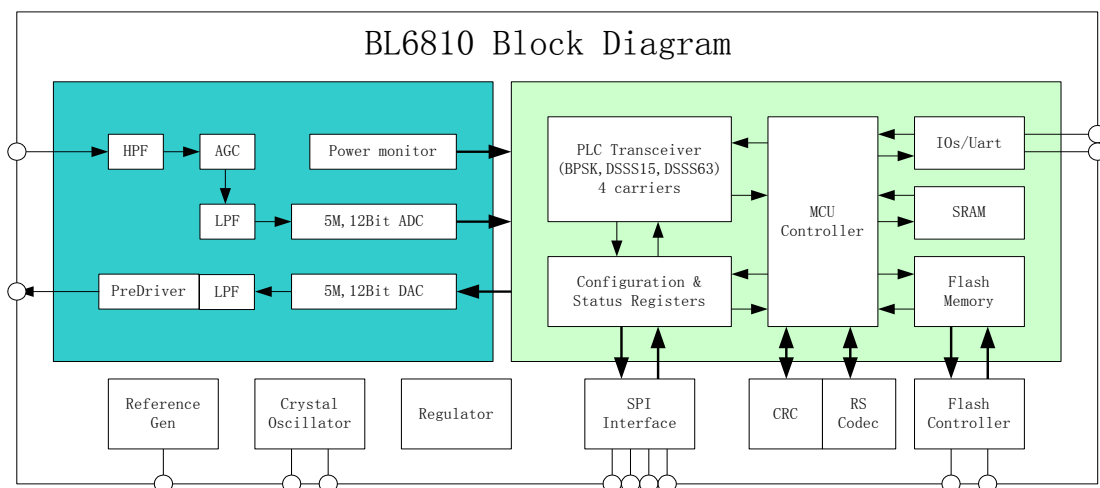
1.3   Applications

- Automatic meter reading
- Smart home
- Street lighting control
- Intelligent building control
- Industrial automation control
- Solar control

1.4   BL6810 Microcontroller

1.4.1   Fully Compatible with the 8051

BL6810 core is fully compatible with MCS-51TM's instruction set. You can use the standard 803x / 805x assemblers and compilers for software development. It has a standard 8052 peripheral component, including three 16-bit counter/timers, a full-duplex UART with enhanced baud rate configuration, 3840 Bytes SRAM, 28KBytes Flash and 512 Bytes user Flash.

1.4.2   High Speed

The instruction execution speed of BL6810 is greatly improved with pipeline structure. In the 8051, all instructions cost 12 or 24 system clock cycles except for MUL and DIV, and the maximum system clock frequency is 12-24MHz. For BL6810 core, most single-byte instruction execution time is just one system clock cycle.

1.4.3   On-chip Memory

BL6810 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, of which the upper 128 bytes is dual-mapped. The upper 128 bytes of RAM can be accessed by indirect addressing, but the 128 bytes' SFR can be accessed by direct addressing. The lower 128 bytes of RAM can be accessed by both indirect and direct addressing. The first 32 bytes is served for four general register banks, and the next 16 bytes can be either addressable by byte or by bit.

External data memory is 3840 Bytes, program memory contains 28K Bytes of FLASH.

1.4.4 Carrier Communication

Carrier communication unit use 12bit ADC and DAC (sampling frequency of 5MHz) that integrates with low-noise 66dB gain-adjustable automatic gain controller and achieves industry leading sensitivity as high as 0.5 u V. It can supports adaptively four carrier frequencies: 131.58k, 263.16k, 312.5k, 416.67 kHz; also three communication data rate: 5.48kbps, 365bps, and 87bps.

1.4.5 UART

BL6810 has a full duplex UART with enhanced baud rate configuration. Serial bus only needs very little CPU intervention for it is all implemented by hardware and also can be interrupted.

2 Electrical Characteristics

2.1 Limit Parameter

Parameter	Min.	Max.	Units
Environment Temperature	-55	125	℃
Storage Temperature	-55	150	℃
The voltage of any port I/O pins or RST pin relative to GND	-0.3	Vdd+0.3	V
The voltage of VDD pin relative to DGND	-0.3	6.0	V
Maximum current of VDD to GND		500	mA
Maximum output current of I/O		100	mA

Note: Exceeding the limit parameters listed above may cause permanent damage to the device. The reliability will be reduced under the conditions of the maximum allowable value or above the maximum allowable value for a long time.

2.2 Operating Parameters

Symbol	Parameter Description	Condition				Units
			Min.	Typ.	Max.	
BWbpf	Receiving band pass Filter bandwidth	Spectrum Analyzer Sweep		110-550		KHz
VINmin	Input Sensitivity	Differential Input			5	uV
VINmax	Maximum input amplitude	Differential Input			400	mV
AGC_range	AGC range		0		66	dB
AGC_step	AGC minimum step			2.2		dB
Voffs_RX_in	Input Bias	AGC=66dB			0.1	mV
Voffs_RX_in	Input Bias	AGC=0dB			20	mV
Voutmax	Output amplitude	Load=1MΩ		±1.5		V
HD2	Second harmonic	Fc=131.58kHz			40	dB
		263.16kHz				
		312.5kHz				
		416.67kHz				
HD3	Third harmonic	Fc=131.58kHz			40	dB
		263.16kHz				
		312.5kHz				
		416.67kHz				
CLTX_OUT	Output capacitive load				400	pF
RLTX_OUT	Output resistive load			200		Ω
Fc	Carrier Frequency			131.58		KHz
				263.16		
				312.5		
				416.67		
Data Rate	Data Rate	BPSK		5480		bps
		DS15		365		
		DS63		87		

2.3 DC Electrical Characteristics

Parameter	Symbol	Specification			Units
		Min.	Typ.	Max.	
Supply Voltage	V_{DD}	4.5	5	5.5	V
Operating Frequency	F		20		MHz
Operating Temperature	T_A	-40		+85	°C
Operating Current	I		35		mA

3 Package and Pin Configuration

3.1 Pin Diagrams

3.2   Package Outlines

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	—	0.20
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.32	—	0.43
b1	0.31	0.35	0.39
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	—	8.25
e	0.80BSC		
L	0.40	—	0.65
L1	1.00BSC		
θ	0°	—	7°
L/F载体尺寸 (mil)	150*150		
	205*205		

DETAIL: F

BASE METAL

WITH PLATING
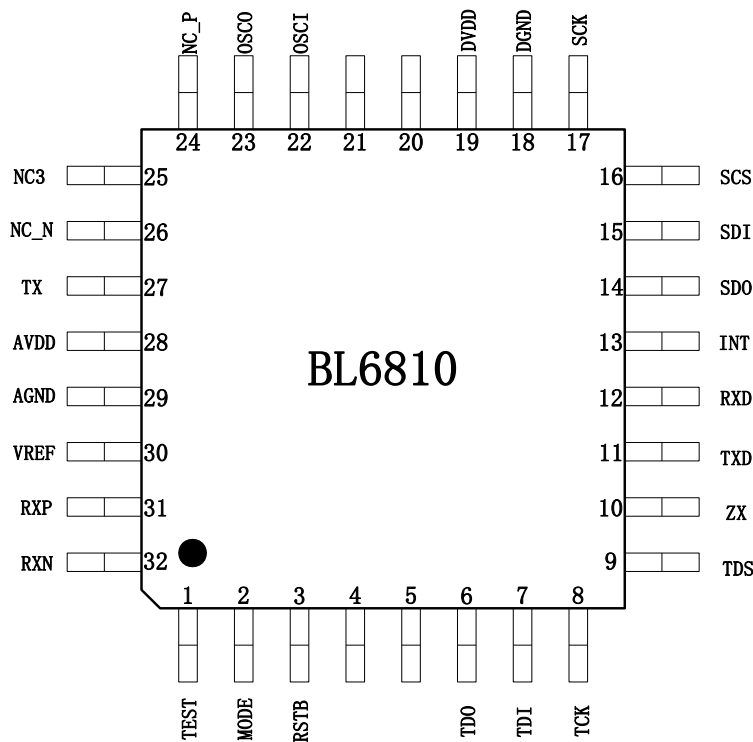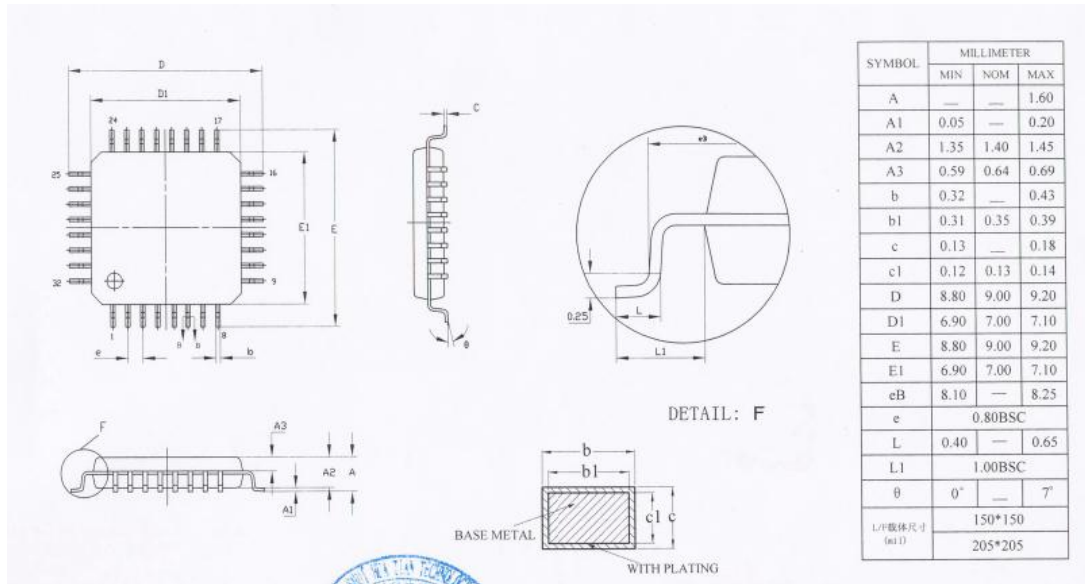
3.3   Pin Configuration

BL6810 is packaged with LQPF32.

Pin No.	Pin Name	Pin Type	Description
1	NC		Not used
2	MODE	I	0: device mode, 1: SOC mode
3	RSTB	I	Driving this pin low resets the MCU
6	TDO	IO	SOC mode: Flash programming Interface，cannot be used for GPIO Device mode: NC
7	TDI	IO	SOC mode: Flash programming Interface，cannot be used for GPIO Device mode: NC
8	TCK	IO	SOC mode: Flash programming Interface，cannot be used for GPIO Device mode: NC
9	TDS	O	SOC mode: Flash programming Interface，can be used as P37（only for output） Device mode: NC
10	ZX	IO	Zero detect input
11	TXD	IO	UART output，can be used as P31
12	RXD	IO	UART input，can be used as P30
13	INT	IO	SOC：P36 Device mode：Usually high level, output low level after receiving power line data.
14	SDO	IO	SOC mode：P35； Device mode：SPI output
15	SDI	IO	SOC mode：P34； Device mode：SPI input
16	SCS	IO	SOC mode：P33； Device mode：SPI chip select
17	SCK	IO	SOC mode：P32； Device mode：SPI clock

18	DGND	IO	Digital GND
19	DVDD	IO	Digital VDD
22	OSCI	I	Oscillator Input
23	OSCO	O	Oscillator Output
24	NC	IO	Not connected
25	NC	IO	Not connected
26	NC	IO	Not connected
27	TX	O	Carrier Output
28	AVDD	IO	Analog VDD
29	AGND	IO	Analog GND
30	VREF	IO	The reference voltage. This pin provides the required bias current for internal circuit by connecting an external 180k ohm resistor to ground.
31	RXP	I	PLC signal input（Positive Differential terminal）
32	RXN	I	PLC signal input（Negative Differential terminal）

Note：All the output pins are Open-drain，which requires 4.7kΩ pull-up resistor.

4 Microcontroller

MCU core is enhanced 8051 microcontroller and compatible with MCS-51TM instruction set, you can use the standard 803x / 805x assemblers and compilers for software development. The series MCU has all the standard 8051 MCU peripherals.

BL6810 microcontroller core has the organizational structure and peripherals with standard 8051, In addition to increased custom peripherals and functions. It greatly enhances its handling capacity. BL6810 core has the following characteristics:

- Fully compatible with MCS-51 instruction set
- 10MHz clock frequency
- 3840 Bytes SRAM
- 28K Bytes Flash
- Expanded interrupt processing system

4.1 Instruction Set

BL6810 controller instruction set is fully compatible with the standard MCS-51TM instruction set. You can use standard development tools to develop BL6810 8051 software. All BL6810 instructions are similar with MCS-51TM products on the binary code and functions, including opcode, addressing modes and effect on PSW flags.

4.2 Memory Organization

BL6810 memory organization is similar with standard 8051 memory organization. There are two separate memory spaces: program memory and data memory. Program memory size is 28KB. RAM data memory including internal and external (on-chip) RAM, the internal RAM size is 256B, external (on-chip) RAM size is 3584B. At the same time, the chip also includes a user 512Bytes Flash, the user can store the data.

BL6810 have a group dedicated expansion register for power line carrier communications.

0x6FFF	
	Program
	Memory
	(28KB)
0x0000	

Internal Data Memory		
(256B)		
0xFF	Upper 128 Bytes	SFR Memory
0x80		
0x7F	Lower 128 Bytes	
0x00		

4.2.1 Program Memory

BL6810 supports 28KB program memory and allocated addresses 0x0000 to 0x6FFF.

4.2.2　Data Memory

BL6810 have 256 bytes internal RAM and allocated 0x00 to 0xFF. The lower 128 bytes use for general register and temp register, it can be accessed by direct or indirect addressing modes. Four general register bank are allocated addresses 0x00 to 0x1F, there are eight 8-bits registers in each bank. The following 16 bytes can be accessed by byte or bit from 0x20 to 0x2F.

Upper 128 bytes can only be accessed by indirect addressing. The storage bank and the Special Function Registers (SFR) occupy the same address space, but physically separate from SFR space. When addressing above 0x7F, addressing mode determines if the CPU access the upper 128 bytes data memory or access SFR. Using direct addressing mode instructions will access the SFR space, using instruction indirect addressing above 0x7F address will access the upper 128 bytes data memory.

4.2.3　General Purpose Registers

The lower 32 bytes data memory from address 0x00 to 0x1F can be use for four general-purpose registers. Each bank has eight 8-bit registers, called R0 - R7. Only one of them can be selected at the same time. PSW.3 and PSW.4 bits are used to select the active register bank. Fast switching is allowed when entering subroutines or interrupt service routine. Indirect addressing mode uses R0 and R1 as indirect address register.

In addition to the data memory accessed by bytes, 16 data memory data units from 0x20 to 0x2F can be accessed by bits. Each bit has a bit address from 0x00 to 0x7F. The byte at address 0x20 Bit-0 allocated 0x00, bit-7 allocated 0x07. The byte at address 0x2F Bit-7 allocated 0x7F. If it is bit addressing or byte addressing can be decided by instruction type.

Bank 0		Bank 1		Bank 2		Bank 3	
Address	Register	Address	Register	Address	Register	Address	Register
00H	R0	08H	R0	10H	R0	18H	R0
01H	R1	09H	R1	11H	R1	19H	R1
02H	R2	0AH	R2	12H	R2	1AH	R2
03H	R3	0BH	R3	13H	R3	1BH	R3
04H	R4	0CH	R4	14H	R4	1CH	R4
05H	R5	0DH	R5	15H	R5	1DH	R5
06H	R6	0EH	R6	16H	R6	1EH	R6
07H	R7	0FH	R7	17H	R7	1FH	R7

4.2.4　Stack

Stack can be located in the 256-byte data memory and specified by the stack pointer（SP，0x81）. SP points to the location last used. Next data will be stored in the SP + 1, then SP is incremented. After resetting the stack pointer is initialized to address 0x07, therefore the first data pushed into the stack will be stored in the address 0x08, which is also the first register (R0) on bank 1. If you use more than one register bank, SP should be initialized to location data memory which is not used for data storage. Stack depth up to 256 bytes.

4.2.5 Special Function Registers

Directly addressable memory space from 0x80 to 0xFF is called the special function registers (SFR). SFR can control the resources and peripheral of BL6810 and data exchange with these resources and peripherals. BL6810 has all SFR of standard 8051, also added some SFR used for configuring and accessing proprietary subsystem. This allows the instruction set is compatible with MCS - 51 tm under the premise of adding new functionality.

Anytime the 0x80 ~ 0xFF memory space accessing by the direct addressing mode is for SFR. Addresses ending in 0x0 or 0x8 SFR (e.g. P0, TCON, P1, SCON, IE, etc.) as well as byte addressable or bit addressable, others SFR byte-addressable only.

SFR Memory Map

Address	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F
F8	SSC_DAT	SSC_ADR						
F0	B							
E8		MD0	MD1	MD2	MD3	MD4	MD5	ARCON
E	ACC							
D8	EXT_DAT	EXT_ADR	DATA_BUF		ADCON			
D0	PSW							
C8	T2CON	T2MOD			TL2	TH2		
C0								
B8	IP0		S0RELH					
B0	P3							
A8	IEN0		S0RELL					
A0	P2							
98	S0CON	S0BUF						
90	P1		DPS			WDTCON	WDTDATA	
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL	DPH	DPL1	DPH1		PCON

SFR

Register	Address	Reset	Description
P0	80h	FFH	Port 0
SP	81H	07H	Stack Point
DPL	82H	00H	Data Pointer Low
DPH	83H	00H	Data Pointer High

DPL1	84H	00H	Data Pointer Low 1
DPH1	85H	00H	Data Pointer High 1
PCON	87H	00H	Power Control Register
TCON	88H	00H	Counter / Timer control register
TMOD	89H	00H	Counter / Timer mode register
TL0	8AH	00H	Counter / Timer0 Low
TL1	8BH	00H	Counter / Timer1 Low
TH0	8CH	00H	Counter / Timer0 High
TH1	8DH	00H	Counter / Timer1 High
CKCON	8EH	01H	CPU external data bus delay control
P1	90H	FFH	Port 1
DPS	92H	00H	Data Pointer Select Register DPS.0 = "0": for DPTR DPS.0 = "1": for DPTR1
WDTCON	95H	00H	Watchdog control register
WDTREL	96H	00H	Watchdog data register
S0CON	98H	00H	UART0 control register
S0BUF	99H	00H	UART0 data buffer
P2	A0H	00H	Port 2
IEN0	A8H	00H	Interrupt Enable register
S0RELL	AAH	00H	UART0 baud register low
P3	B0H	FFH	Port 3
IP0	B8H	00H	Interrupt priority register
S0RELH	BAH	00H	UART0 baud register high
PSW	D0H	00H	Program Status Word
EXT_DAT	D8H	00H	Extended register data
EXT_ADR	D9H	00H	Extended register address
DATA_BUF	DAH	00H	PLC send data buffer (SOC mode)
ADCON	DCH	00H	UART0 baud control register
ACC	E0H	00H	Accumulator
MD0	E9H	00H	Multiplication and division register 0
MD1	EAH	00H	Multiplication and division register1
MD2	EBH	00H	Multiplication and division register 2
MD3	ECH	00H	Multiplication and division register 3

MD4	EDH	00H	Multiplication and division register 4
MD5	EEH	00H	Multiplication and division register 5
ARCON	EFH	00H	Arithmetic Control Register
B	F0H	00H	B register
SSC_DAT	F8H	00H	User FLASH Data
SSC_ADR	F9H	00H	User FLASH Address

4.3　Multiplication and Division Unit（MDU）

MDU can significantly increase the speed of an unsigned 16-bit multiplication and 32 division, shifting operating. The following table shows the implementation of the characteristics of these operations. MDU does not contain state flag of operation completed. With a NOP delay for waiting necessary operation time in order to define the operation end time is the most effective way to use MDU, calculating the clock starts from the last data written.

Operations	Result	Reminder	Clock Time
32-bits divided by 16-bits	32bit	16bit	17
16-bits divided by 16-bits	16bit	16bit	9
16-bits multiplied by 16-bits	16bit		10
32-bits normalized			3-20
32-bits Shift			3-18

MDU work by accessing operands and operating results of MD0-MD5 and ARCON.

R	R	R/W	R/W	R/W	R/W	R/W	R/W
MDEF	MDOV	SLR	SC4	SC3	SC2	SC1	SC0

ARCON：Arithmetic Control Register

Reset：00000000

SFR Address：0xEF

位 7：MDEF（MDU Error Flag）

MDU error flag, indicates an operation error execution (when one of the new arithmetic operation is interrupted or restart).

位 6：MDOV（MDU Overflow flag）

When divisor is zero or multiplication result exceeds 0x0000FFFFh, MDOV bit is set to 1.

位 5：SLR　（Shift direction control bit）

0：Left Shift

1：Right Shift

位 4-0：SC4-0　（Shift Count）

SC[4:0] = 0，Normalization function

SC[4:0] ≠ 0，Shift function

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

MD0-MD5：Multiplication and division data register

Reset： 00000000

SFR Address： 0xE9-0xEE

5 FLASH Memory

A 28K Bytes internal Flash is provided primarily for storing and executing 8051 MCU code. It can be programmed to programming interface.

We provide the programming tools "Flash Programming Utility" too, code programming through custom programming interface. More detail please refer to "Programming Guide".

6 Clock

A 20MHz external oscillator input is provided to hook to an external crystal. Internal oscillator time base signal is provided by the internal oscillator circuit and external quartz crystal, after an internal divide, MCU work at 10MHz.

7 Interrupt

BL6810 includes an extended interrupt system supporting five interrupt sources, including the three timer interrupts; an UART interrupt and a PLC receive interrupt (external interrupt 1). Each interrupt source hold one or more interrupt flag in an SFR. When a peripheral or external source meets a valid interrupt condition, the corresponding interrupt flag is set to logic 1.

If an interrupt source is enabled, the interrupt will generate when interrupt flag is set. Once the current instruction is executed, CPU generates an LCALL to a predetermined address to begin execution of an interrupt service routine (ISR). Each ISR must end with RETI instruction and return to the next instruction before executing the interrupt. If the interrupt is not enabled, the hardware interrupt flag will be ignored, and program is to continue. If interrupt flag is set or not will not be effected by interrupt enable or disable.

Each interrupt source can be enabled or disabled by an SFR (IEN0) relevant interrupt enable bit , but EA bit (IEN0.7) must be set to '1', to ensure that each individual interrupt enable bits are valid. Regardless of each interrupt enable bit setting, clearing EA bit will disable all interrupts.

Some interrupt flag is automatically cleared when the CPU enters ISR, but most of the interrupt flag is not cleared by hardware and must be cleared before the ISR return by software. If an interrupt flag still remains set after the CPU completed the return from interrupt (RETI) instruction, it will immediately generate a new interrupt request, CPU will re-enter the ISR after executing the next instruction.

7.1 Interrupt Source and Vector

MCU supports 16 interrupt sources. Software can simulate an interrupt by any one interrupt flag is set to logic 1. If the interrupt flag is enabled, the system will generate an interrupt request, CPU interrupt flag will jump to the corresponding ISR address. The following table lists BL6810 interruption.

Source	Vector	No.	Flag	Enable
Timer 0 overflow	000BH	1	TF0 (TCON.5)	ET0 (IEN0.1)
PLC Receive Interrupt	0013H	2	IE1 (TCON.3)	EX1 (IEN0.2)
Timer 1 overflow	001BH	3	TF1 (TCON.7)	ET1 (IEN0.3)
UART0	0023H	4	RI0 (SCON0.0)	ES (IEN0.4)
			TI0 (SCON0.1)	
Timer 2 overflow	0033H	6	TF2H (T2CON.7)	ET2 (IEN0.6)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
EA	ET2		ES0	ET1	EX1	ET0	

IEN0：Interrupt Enable Register

Reset：00000000

SFR Address：0xA8

All bits：0（Disable）1（Enable）

位 7：EA　（Enable all the Interrupts）

位 6：ET2　（Timer2 Interrupt Enable）

位 5：NC

位 4：ES0　（UART0 Interrupt Enable）

位 3：ET1　（Timer1 Interrupt Enable）

位 2：EX1　（PLC Receive Interrupt Enable）

位 1：ET0　（Timer0 Interrupt Enable）

位 0：NC

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	PT2		PS0	PT1	PX1	PT0	

IP0：Interrupt priority register

Reset：00000000

SFR Address：0xB8

All bits：0（low priority）1（high priority）

位 7：NC

位 6：PT2　（Timer2 interrupt priority）

位 5：NC

位 4：PS0　（UART0 interrupt priority）

位 3：PT1　（Timer1 interrupt priority）

位 2：PX1　（PLC interrupt priority）

位 1：PT0　（Timer0 interrupt priority）

位 0：NC

8 UART

BL6810 provides an asynchronous, full duplex UART. It supports standard 8051 model 0,1,2,3 with an enhanced baud rate generator circuit. Multiple clock sources can be used to generate standard baud rates. Receive data buffer mechanism allows UART0 start to receive the second byte before read the first byte. UART0 has two related SFRs: Serial Control Register (SCON0) and Serial Data Buffer (SBUF0). SBUF0 can be accessed for sending and receiving. To write SBUF0 will automatically access the transmit register and to read SBUF0 will automatic access to the receive register.

If the UART0 interrupt is enabled, the Interrupt will be occurred when sending was completed (SCON0 TI0 is set in '1') or receives data bytes (SCON0 RI0 is set in '1'). Hardware will not clear the interrupt flag when MCU jump to the interrupt service routine. The interrupt flag must be cleared by software.

8.1   UART0 Mode

UART0 supports four operating modes (one synchronous mode and three asynchronous modes) by setting S0CON register. Four modes provide different communication protocols and baud rates.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SM0	SM1	SM2	REN	TB8	RB8	TI0	RI0

S0CON：UART0 Control Register
Reset：00000000
SFR Address：0x98
位 7：SM0（URAT0 Operating Mode Select）
位 6：SM1（URAT0 Operating Mode Select）
位 5：SM2（Multiprocessor Communication Enable）
      Mode0：SM2=0
      Mode1：SM2=0，Ignore stop bit
            SM2=1，stop bit=1，RI0 activated
      Mode2/3：
            SM2=0，Ignore bit8
            SM2=1，bit8=1，RI0 activated
位 4：REN（Receive Enable）
      0：UART0 Disable
      1：UART0 Enable
位 3：TB8（bit8 transmit bit）
      This bit is assigned to bit8 of Modes 2 and 3 and set or cleared by software.
位 2：RB8（bit8 receive bit）

This bit is assigned to bit8 of Modes 2 and 3. At Mode0, this bit will be set to the receiving stop bit.

位 1：TI0（Transmit Interrupt Flag）

When UART0 transmitted one byte (send bit7 at mode0, send stop bit at others modes), this bit is set by hardware. If UART0 interrupt is enabled, the location of an MCU will jump to UART0 interrupt service routine when this bit was set to 1. This bit must be manually cleared by software.

位 0：RI0（Receive Interrupt Flag）

When UART0 received one byte, this bit is set by hardware. If UART0 interrupt is enabled, the location of an MCU will jump to UART0 interrupt service routine when this bit was set to 1. This bit must be manually cleared by software.

SM0	SM1	Mode	Baud Rate
0	0	Mode 0：shift register	fclk/12
0	1	Mode 1：Asynchronous 8bit	Based on Bd（ADCON.7) and smod（PCON.7）
1	0	Mode 2：Asynchronous 9bit	Based on smod（PCON.7）
1	1	Mode 3：Asynchronous 9bit	Based on Bd（ADCON.7)和 smod（PCON.7）

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BD							

ADCON：UART0 Baud Rate Control Register

Reset：00000000

SFR Address：0xDC

位 7：BD（URAT0 Variable baud rate selection bits）

  0：UART0 Select the baud rate by S0REL register

  1：UART0 Select the baud rate by Timer1

位 6-0：NC

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
					BIT2	BIT1	BIT0

S0RELH：UART0 Baud Rate High Register

Reset：00000000

SFR Address：0xBA

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0

S0RELL：UART0 Baud Rate Low Register

Reset：00000000

SFR Address：0xAA

8.2　Mode0

Mode0 provides synchronous, half-duplex communication. Transmit and receive data on RX0 pin, TX0 pin provides transmit and receive shift clock.

Data transmission begins when performing a write S0BUF register instructions. Transmit and receive data are 8-bits, LSB first, the interrupt flag TI0 will be set at the end of the eighth bit. The data will be received when the receive enable bit REN is set to 1 and receive interrupt flag RI0 is cleared. RI0 flag is set after the eighth bit being shifted and the receiving process stops, until software clears RI0. An interruption will be occurred after TI0 or RI0 is set if the interrupt is enable.

Mode0 baud rate calculation formula:：

Baud Rate = fclk/12

8.3　Mode1

Mode1 provides a standard asynchronous, full duplex communication. Each data byte using 10 bits: 1 start bit, 8 data bits (LSB first) and a stop bit. Data transmits from TX0 pin and receives at RX0 pin. 8 data bits stored in S0BUF, stop bit put in RB8.

Transmission starts after executed a command to write a byte to S0BUF register. When sending end, TI0 interrupt flag is set. Data reception can begin when REN Receive Enable bit is set to 1. the data byte will be loaded into the receiving register S0BUF after receiving the stop bit if meet the following conditions: RI0 is 0, and stop bit is 1 when SM2 is 1. That means the last time reception was done and interrupt was cleared, the shift has been moved to the stop bit.

Then the 8-bits data is stored in S0BUF, stop bit is stored in RB8, RI0 flag is set. At the same time, if interrupts are enabled, the interrupt occurred when TI0 or RI0 was set.

Mode1 baud rate calculation formula:

adcon.7=0: baud rate $= \dfrac{2^{smod} * t1ov}{32}$ 　（Timer1 must be set to Mode2）

adcon.7=1: baud rate $= \dfrac{2^{smod} * fclk}{64 * (2^{10} - s0rel)}$

$$t1ov = \dfrac{12^{smod2} * fclk}{12 * (256 - th1)}$$

For example, using 20M crystal oscillator (internal default divided to 10M), each baud rate configuration as follows:

Baud Rate	1200	2400	4800	9600	19200	38400
TH1	0xEA	0xF5	0xF5	0xBF	0xDF	0xF0
PCON	0x00	0x00	0x80	0x88	0x88	0x88

8.4　Mode2

Mode 2 provides asynchronous, full duplex communication. Each data byte using 11 bits: 1 start bit, 8 data bits (LSB first), a programmable bit (bit8) and one stop bit. Mode2 supports multiprocessor communications and hardware address recognition. When sending, bit8 that determined by the TB8 values can be assigned to the parity symbol P, or used for multiprocessor communications. When receiving, bit8 is put in RB8, the stop bit is ignored.

Transmission starts after executed a command to write a byte to S0BUF register. When sending end, TI0 interrupt flag is set. Data reception can begin when REN Receive Enable bit is set to 1. The data byte will be loaded into the receiving register S0BUF after receiving the stop bit if RI0 is 1 and meet the following conditions:

1. SM2 is 0, means 8-bits data received, bit8 is 0 or bit8 is parity bit.
2. SM2 is 1, bit8 is 1 and the address received matches the address of UART0.

Then the 8-bits data is stored in S0BUF, stop bit is stored in RB8, RI0 flag is set. At the same time, if interrupts are enabled, the interrupt occurred when TI0 or RI0 was set.

Mode2 baud rate calculation formula:
smod(PCON.7) = 0 :　baud rate = fclk/64;
smod(PCON.7) = 1 :　baud rate = fclk/32

8.5　Mode3

Model3 uses transport protocol of Mode2, baud rate is the same as the model1. Each data byte using 11 bits: 1 start bit, 8 data bits (LSB first), a programmable bit (bit8) and one stop bit

The baud rate calculation formula of Mode3 is the same as Mode1.

9 Timer

BL6810 supports 3 16-bits timer/counter. Two of them are compatible with the standard 8051 counter / timers, the other one is a 16-bits auto-reload timer can be used as a general purpose timer. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer0 and Timer1 are nearly identical, there are four operating modes. Timer2 can be used as a 16 or two 8-bit auto-reload timer.

9.1　　Timer0 and Timer1

Each counter/timer is a 16-bit register being accessed in the form of two bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). Counter/timer control register (TCON) can enable Timer0 and Timer1 and show theirs state. By setting IEN register ET0 to 1 to enable the timer0 interrupt and setting ET1 position to 1 to enable the Timer1 interrupt. These two counter/timers have four operating modes, by setting the mode select bits in counter/timer mode (TMOD) register to select the operating mode, each timer can be configured independently. Four modes of operation are identical to the standard 8051.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

TCON：Timer control register
Reset： 00000000
SFR Address：　0x88
位 7：TF1　（Timer1 overflow flag）
　　　0：Timer1 does not overflow
　　　1：Timer1 overflow
　　　Cleared by hardware when processor vectors to interrupt routine. Set by hardware on timer/counter overflow, when the timer 1 register overflows.
位 6：TR1　（Timer1 Run Control bit）
　　　0：Disable Timer1
　　　1：Enable Timer1
位 5：TF0　（Timer0 overflow flag）
　　　0：Timer0 does not overflow
　　　1：Timer0 overflow
　　　Cleared by hardware when processor vectors to interrupt routine. Set by hardware on timer/counter overflow, when the timer 0 register overflows.
位 4：TR0　（Timer0 Run Control bit）
　　　0：Disable Timer0
　　　1：Enable Timer0

位 3：IE1　（Interrupt 1 Edge Flag）

    Cleared by hardware when interrupt is processed if edge-triggered (see IT1).Set by hardware when external interrupt is detected on INT1# pin.

位 2：IT1　（Interrupt 1 Type Control Bit）

    Clear to select low level active (level triggered) for external interrupt 1 (INT1#).Set to select falling edge active (edge triggered) for external interrupt 1.

    0：/INT1 level triggered

    1：/INT1 edge triggered

位 1：IE0　（Interrupt 0 Edge Flag）

    Cleared by hardware when interrupt is processed if edge-triggered (see IT0).Set by hardware when external interrupt is detected on INT0# pin.

位 0：IT0　（Interrupt 0 Type Control Bit）

    Clear to select low level active (level triggered) for external interrupt 0 (INT0#).Set to select falling edge active (edge triggered) for external interrupt 0.

    0：/INT0 level triggered

    1：/INT0 edge triggered

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0

TMOD：Timer/Counter 0 and 1 Modes

Reset：00000000

SFR Address：　0x89

位 7：GATE1（Timer 1 Gating Control Bit）

    0: enable timer 1 whenever the TR1 bit is set.

    1: enable timer 1 only while the INT1# pin is high and TR1 bit is set.

位 6：C/T1　（Timer 1 Counter/Timer Select Bit）

    0: timer operation: timer 1 counts the divided-down system clock.

    1: Counter operation: timer 1 counts negative transitions on external pin T1.

位 5：T1M1（Timer 1 Mode Select Bits）

位 4：T1M0（Timer 1 Mode Select Bits）

T1M1	T1M0	Mode
0	0	Mode 0: 8-bit timer/counter (TH1) with 5-bit presale (TL1).
0	1	Mode 1: 16-bit timer/counter.
1	0	Mode 2: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow.
1	1	Mode 3: timer 1 halted. Retains count.

位 3：GATE0（Timer 0 Gating Control Bit）

    0: enable timer 0 whenever the TR0 bit is set.

1: enable timer 0 only while the INT0# pin is high and TR0 bit is set.

位 2：C/T0 （Timer 0 Counter/Timer Select Bit）

    0: timer operation: timer 0 counts the divided-down system clock.

    1: Counter operation: timer 0 counts negative transitions on external pin T0.

位 1：T0M1 （Timer 0 Mode Select Bits）

位 0：T0M0 （Timer 0 Mode Select Bits）

T0M1	T01M0	Mode
0	0	Mode 0: 8-bit timer/counter (TH0) with 5-bit presale (TL0).
0	1	Mode 1: 16-bit timer/counter.
1	0	Mode 2: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow.
1	1	Mode 3: TL0 is an 8-bit timer/counter.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SMOD				SMOD2			

PCON：Power Configuration Register

Reset：01111111

SFR Address：0x87

位 7：SMOD （UART baud rate select bit）

位 6：NC

位 5：NC

位 4：NC

位 3：SMOD2 （Timer 1 clock select）

    0：fclk/12

    1：fclk

位 2：NC

位 1：NC

位 0：NC

9.2 Timer2

It is a 16-bit timer/counter: the count is maintained by two 8-bit timer registers: TH2 and TL2.
Timer 2 includes the following enhancements:

Auto-reload mode (up or down counter)

Programmable clock-output

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		TF2	TR2				

TCON2：Timer 2 Control Register
Reset：00000000
SFR Address：   0xC8
位 7：NC
位 6：NC
位 5：TF2   （Timer 2 Overflow Flag）
    0：Timer 2 does not overflow
    1：Timer 2 overflow
    Must be cleared by software.
    Set by hardware on timer 2 overflow.
位 4：TR2   （Timer 2 Run Control bit）
    0：Disable Timer 2
    1：Enable Timer 2
位 3：NC
位 2：NC
位 1：NC
位 0：NC

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
				GATE2	C/T2	T2M1	T2M0

TMOD2：Timer 2 Mode Control Register
Reset：00000000
SFR Address：   0xC9
位 7：NC
位 6：NC
位 5：NC
位 4：NC
位 3：GATE2（Timer 2 Gating Control Bit）
    0: Enable timer 2 whenever the TR2 bit is set.
    1: Invalid

位 2：C/T2 （Timer/Counter 2 Select bit）

    0: timer operation (input from internal clock system: FOSC).

    1: Invalid

位 1：T2M1（Timer 2 Mode Select Bits）

位 0：T2M0（Timer 2 Mode Select Bits）

T0M1	T01M0	Mode
0	0	Invalid
0	1	Mode 1: 16-bits counter/timer
1	0	Mode 2：8-bits auto-reload counter/timer
1	1	Invalid

Note: The function of GATE2 is identical with TR2 but opposite polarity. It means to turn off Timer 2 by GATE2=1 or TR2=0.

10 Watchdog

Watchdog can be used by configuring the WDTCON register. Watchdog maximum timeout is 104ms. If interval time of two write operating for WDTDATA register exceed the specified time, WDT will generate a reset. You can configure and enable / disable WDT by software. After system reset the watchdog is enabled.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
EWDT	RWDT				WDT2	WDT1	WDT0

WDTCON：Watchdog Control Register

Reset： 00000000

SFR Address： 0x95

位 7：EWDT（Watchdog Control bit）

    0：Watchdog disable

    1：Watchdog enable

位 6：RWDT（Watchdog Overflow Control bit）

    0：Watchdog overflow as interrupt

    1：Watchdog overflow as reset

位 5：NC

位 4：NC

位 3：NC

位 2：WDT2：（Watch Clock Select bit）

位 1：WDT1：（Watch Clock Select bit）

位 0：WDT0：（Watch Clock Select bit）

WDT2	WDT1	WDT0	Clock Select
0	0	0	fclk/32
0	0	1	fclk/64
0	1	0	fclk/128
0	1	1	fclk/256
1	0	0	fclk/512
1	0	1	fclk/1024
1	1	0	fclk/2048
1	1	1	fclk/4096

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
-	-	-	-	-	-	-	-

WDTCON：Watchdog Data Register

Reset： 00000000

SFR Address： 0x96

Used for loading into watchdog counter

11 SPI

The SPI interface is only available when the BL6810 is set to Device mode, BL6810 SPI interface only use as a slave device. SPI interface is mainly used for data transmission between concentrator modules and the host STM32.

- full-duplex serial bus
- only use as a slave device
- three-line mode
- clock is provided by the master device, the maximum clock rate is 250k
- transfer 8-bit data, high byte first

11.1 System Block
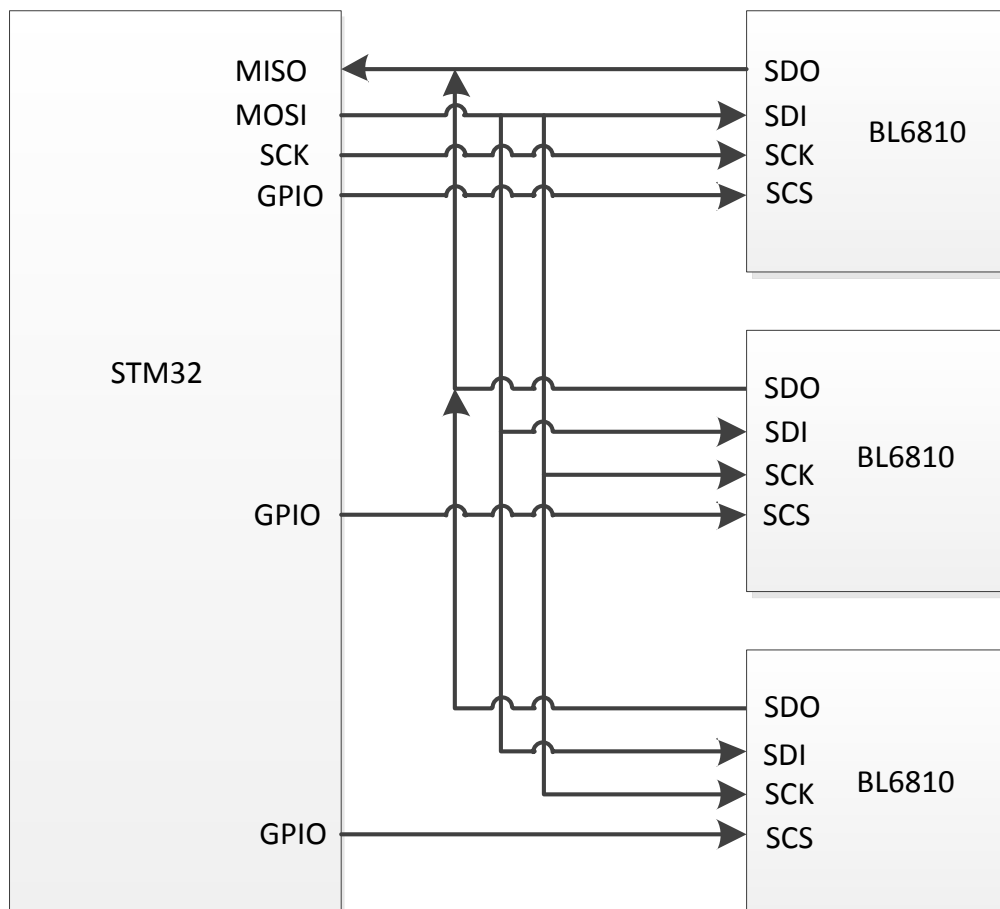
11.2   Sequence Diagram

The default configuration CPOL=1，CPHA=1，the same in STM32.

11.3   Download Processes

STM32 pull down the chip select port SCL of BL6810 for data transmission request. The data will be stored in the SPIBUF register of BL6810. Then the data in BL6810's SPIBUF 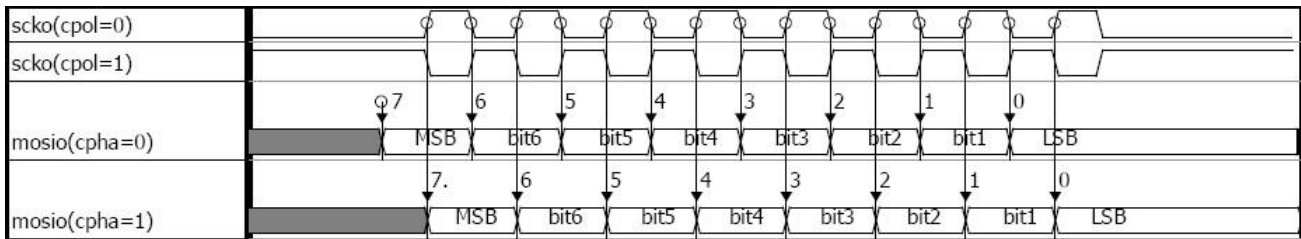transferred to the STM32 SPIBUF register too, completed the data exchange at the end. In Device mode, the data transmission from STM32 to BL6810 related with extended registers.

11.4   Upload Processes

After BL6810 received data frame transferred from power line, each byte will be stored in DATABUF register according to the order. When BL6810 got the first byte and transmitted it to SPIBUF, INT pin will output low automatic for telling STM32 it is time to take the data. STM32 should receive the data in SPIBUF immediately otherwise it will be overwritten by subsequent bytes and data frame will miss. At BPSK mode (5.48kbps), the valid time of each byte is about 1.46ms.

12 Chip Work Mode

BL6810 supports two work modes, SOC mode and Device mode.

12.1 SOC Mode

SOC mode is typically used for meter modules or II collector. We can use 8051 core for data reception and transmission process. Such as application layer data framing, parsing, routing established at the network layer, the data forwarding, and the PHY layer of the data transmission and reception processing can be completed by BL6810. Code will be written by chip programming interface.

12.2 Device Mode

Device mode is typically used for concentrator modules. Now BL6810 only used as a channel for PHY layer data transmitting and receiving and communicating with STM32 with SPI interface. The host transmits the control byte and data to expand registers of BL6810 through SPI interface. BL6810 will process this data base on control byte automatic. At this situation, no need to write any code into BL6810 and all control code for concentrator module are stored in the host computer.

13 Application Notes

13.1 Communication Block Description

The mainly analog modules in BL6810 include high-pass filter (HPF), a variable gain amplifier (VGA), low pass filter (LPF), AD converter (ADC), DA converter (DAC), the output low pass filter (TX_LPF) and ClassAB PA.

In RX section, HPF is used to filter out low frequency signals below 100 KHz, VGA provides 0-66dB voltage gain. LPF is an anti-aliasing filter, ADC quantified analog signals to 12BIT for digital module. In TX section, 12-bits digital signal provided by the transmission module is converted to analog signal by DAC. When the analog signal passed the LPF, it will be send to power line by the ClassAB driving circuit
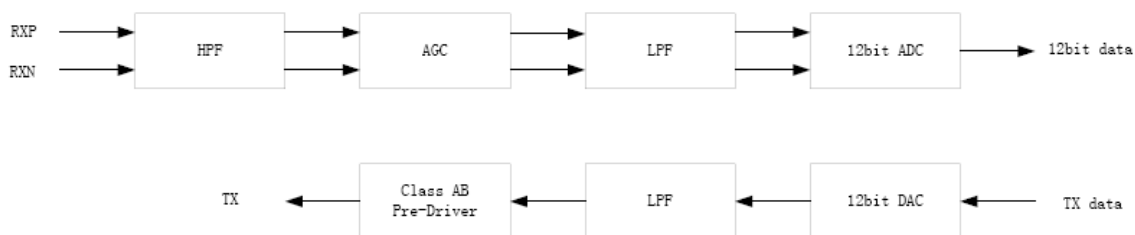
BL6810 Analog Front End

The 12-bits digital signal output from ADC passes through a high-performance band pass filter to filter out-of-band noise, the signal down-sampling, down-sampling signal and its 90-degree shift signal are put into COSTAS loop and locked. The locked signal was put into FRAME LOCK module for signal extracting after interpolating and processing by matched filter. The process of sending the signal is relatively simply, the data need to send is written to communication module and modulated at carriers, and is send to DAD after passed shaping filter. At the end the data is output after passed LPF and Pre-Driver.
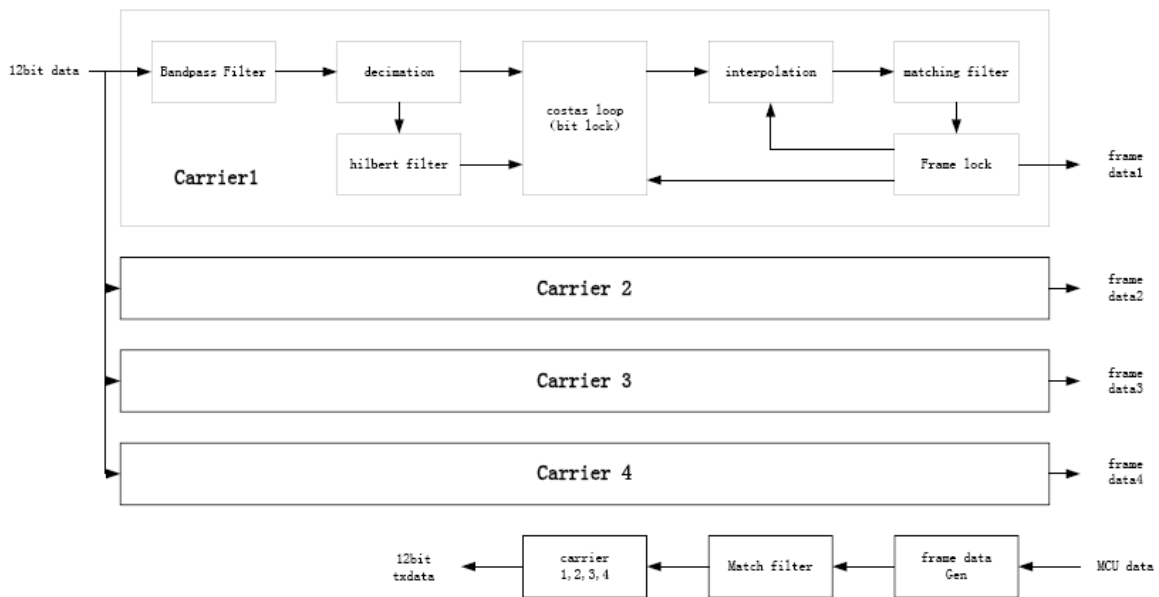
BL6810 Communication Receive Module

13.2 SPI Description

Serial Peripheral Interface (SPI) is a four-wire serial communication protocol developed by Motorola. SPI protocol is master-slave mode, this mode usually has a master device and one or more slave devices. The following diagram shows the device SPI interface.

The master device controls the data transmission by supporting shift clock and slave enable signal. The slave enable signal is an optional high and low level, it can activate the serial input and output of slave device (without clock). If slave enable signal absent, the communication between master and salve device is determined by shift clock. At this moment, the slave device must remain active throughout and only one slave device should exist.
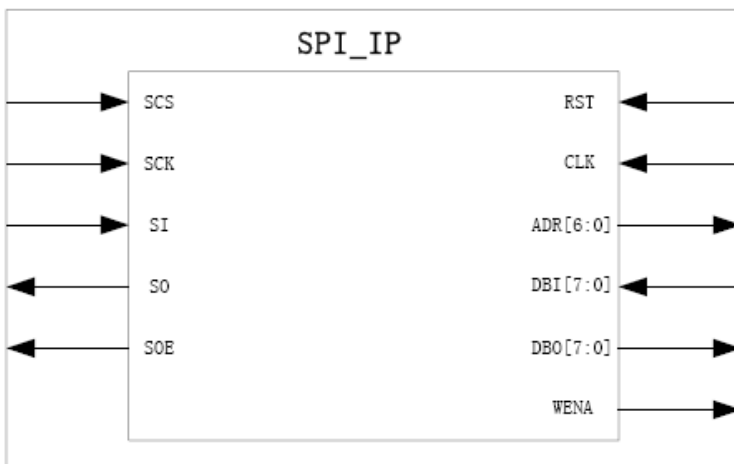
Port Name	Input/ Output	Bit side	Synchronization/ Asynchronization	Function Description
RST	IN	1	Asynchronization	Internal system reset signal
CLK	IN	1	Synchronization	Clock (10MHz)
ADR	OUT	7	Synchronization	Externally accessible register bank address bus input
DBI	IN	8	Synchronization	Externally accessible register bank data bus output
DBO	OUT	8	Synchronization	Externally accessible register bank data bus input
WENA	OUT	1	Synchronization	Externally accessible register bank synchronous write enable
SCS	IN	1	Asynchronization	SPI chip select
SCK	IN	1	Asynchronization	SPI Serial Clock Input
SI	IN	1	Asynchronization	SPI Serial data Input
SO	OUT	1	Synchronization	SPI Serial data output
SOE	OUT	1	Synchronization	SPI Serial data output enable control

Sequence Diagram：
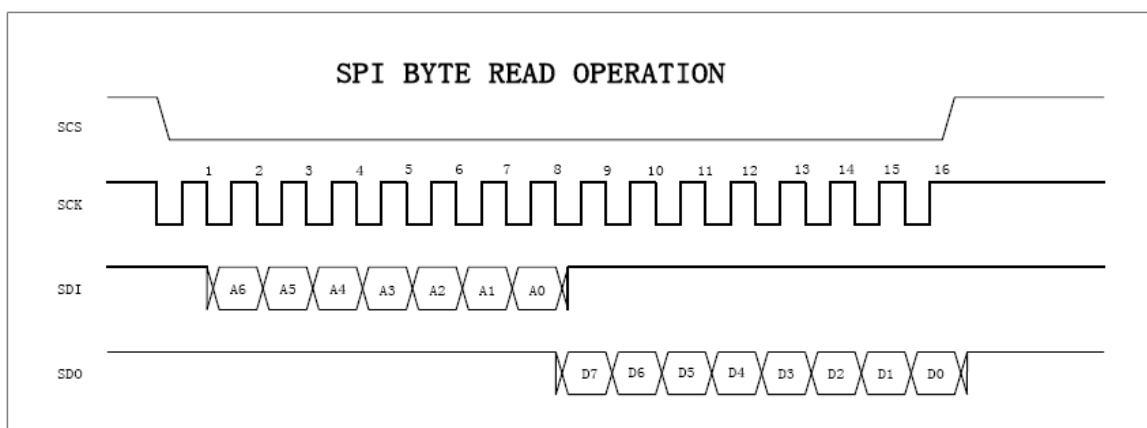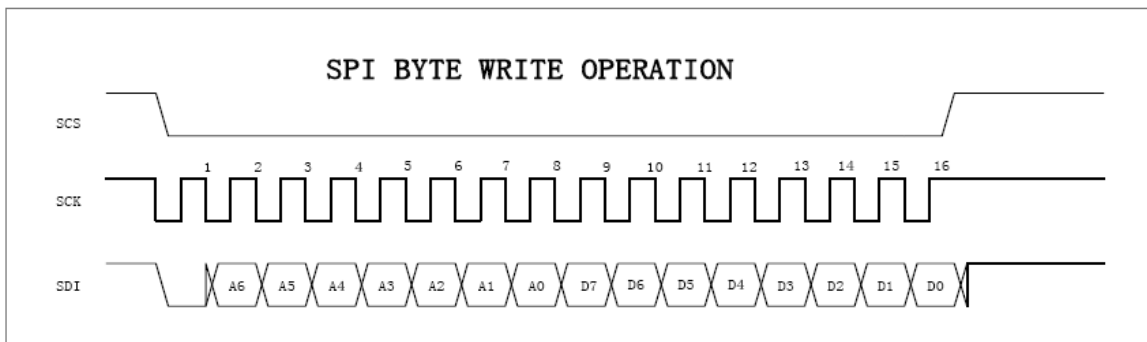
13.3　BL6810 Expand Register

In SOC mode, MCU access registers associated with communication by accessing the SFR addresses 0xd9 and 0xd8, expand registers are not directly accessible. The expand register address is stored in 0xd9, the data read or written from expand register is stored in 0xd8. In addition, the expand register is write-protected. 0xff should be written into 0xd8 and 0xd9 for releasing the write protection before write operation. If there is a request to send data, MCU should write the data to be transmitted to 0xda. At Device mode, data to be transmitted should be written to 0x13.

13.3.1　Chip ID

Name	Address	Initial value	Type	Description
Chip ID	0x00	0xa1	RO	chip ID

13.3.2　The period of line voltage

Name	Address	Initial value	Type	Description
Line period	0x02	0x00	RO	The period of line voltage，0.1ms/LSB

13.3.3　AGC Control

Name	Address	Initial value	Type	Description
AGC_CTR	0x09	0x00	RW	[4:0]: control signals for AGC [7]: manual [6:5]: reserved

13.3.4 Transmission Control

Name	Address	Initial value	Type	Description
XT_CTRL	0x10	0x00	RW	[7]: transmit/receive control 1: transmit 0: receive [6]: longhead [5:3]: reserved [2]: PD_DAC [1]: XMT_PHASE_ENA, sending by zero cross [0]: XMT_PIFP, sending fire program data

13.3.5 Frequency/Rate Select

Name	Address	Initial value	Type	Description
XT_SEL	0x11	0x10	RW	[7:4]: XMT_CH, carrier frequency selection [4]: 131.58KHz. 1: on; 0: off [5]: 263.16KHz. 1: on; 0: off [6]: 312.50KHz. 1: on; 0: off [7]: 416.67KHz. 1: on; 0: off [1:0]: XMT_RATE, data rate selection 00: 5.48Kbps 01: 783bps 10: 87bps 11: reserved

13.3.6 Transmit Power Control

Name	Address	Initial value	Type	Description
XT_AMP	0x12	0x80	RW	transmit power control 0x00: minimum 0x80: maximum

13.3.7 Sending Data

Name	Address	Initial value	Type	Description
XT_DATA	0x13	0x00	RW	Device mode，sending data

13.3.8 Sending Status

Name	Address	Initial value	Type	Description
XT_STATUS	0x14	0x00	RW	[0]: XMT_EMPTY, buffer data is being sent out, hardware set and clear [1]: XMT_EXPIRE, data sending expire, software clear [2]: XMT_SUCCESS, software clear [3]: reserved [7]: frame end enable [6:4]: reserved

13.3.9 Receive Status

Name	Address	Initial value	Type	Description
Rec_Status	0x25	0x00	RO	receive status: [7]: reserved [6]: active high for dsss63 [5]: active high for dsss15 [4]: active high for bpsk [3]: receive data interrupt status of channel3 [2]: receive data interrupt status of channel2 [1]: receive data interrupt status of channel1 [0]: receive data interrupt status of channel0

13.3.10 Carrier 1 Frame Phase

Name	Address	Initial value	Type	Description
FPHASE_Carrier1	0x26	0x00	RO	the phase at frame sync

13.3.11 Carrier 1 Interrupt Information

Name	Address	Initial value	Type	Description
INTMSG_Carrier1	0x27	0x00	RO	[7:0]: message 0: training code 1: frame head detection 2: byte receiving 3: frame end received success 4: frame head failure 5: frame end failure 6: fire update frame head detection 7: zero crossing frame head detection

13.3.12 Carrier 1 Received Data

Name	Address	Initial value	Type	Description
DATA_Carrier1	0x28	0x00	RO	received data

13.3.13 Carrier 1 Parity

Name	Address	Initial value	Type	Description
Parity_Carrier1	0x29	0x00	RO	[2:0]: received compliment data [P, 0, 1] [7:3]: reserved

13.3.14 Carrier 2 Frame Phase

Name	Address	Initial value	Type	Description
FPHASE_Carrier2	0x2a	0x00	RO	the phase at frame sync

13.3.15 Carrier 2 Interrupt Information

Name	Address	Initial value	Type	Description
INTMSG_Carrier2	0x2b	0x00	RO	[7:0]: message 0: training code 1: frame head detection 2: byte receiving 3: frame end received success 4: frame head failure 5: frame end failure 6: fire update frame head detection 7: zero crossing frame head detection

13.3.16 Carrier 2 Received Data

Name	Address	Initial value	Type	Description
DATA_Carrier2	0x2c	0x00	RO	received data

13.3.17 Carrier 2 Parity

Name	Address	Initial value	Type	Description
Parity_Carrier2	0x2d	0x00	RO	[2:0]: received compliment data [P, 0, 1] [7:3]: reserved

13.3.18 Carrier 3 Frame Phase

Name	Address	Initial value	Type	Description
FPHASE_Carrier3	0x2e	0x00	RO	the phase at frame sync

13.3.19 Carrier 3 Interrupt Information

Name	Address	Initial value	Type	Description
INTMSG_Carrier3	0x2f	0x00	RO	[7:0]: message 0: training code 1: frame head detection 2: byte receiving 3: frame end received success 4: frame head failure 5: frame end failure 6: fire update frame head detection 7: zero crossing frame head detection

13.3.20 Carrier 3 Received Data

Name	Address	Initial value	Type	Description
DATA_Carrier3	0x30	0x00	RO	received data

13.3.21 Carrier 3 Parity

Name	Address	Initial value	Type	Description
Parity_Carrier3	0x31	0x00	RO	[2:0]: received compliment data [P, 0, 1] [7:3]: reserved

13.3.22 Carrier 4 Frame Phase

Name	Address	Initial value	Type	Description
FPHASE_Carrier4	0x32	0x00	RO	the phase at frame sync

13.3.23 Carrier 4 Interrupt Information

Name	Address	Initial value	Type	Description
INTMSG_Carrier4	0x33	0x00	RO	[7:0]: message 0: training code 1: frame head detection 2: byte receiving 3: frame end received success 4: frame head failure 5: frame end failure 6: fire update frame head detection 7: zero crossing frame head detection

13.3.24 Carrier 4 Received Data

Name	Address	Initial value	Type	Description
DATA_Carrier4	0x34	0x00	RO	received data

13.3.25 Carrier 4 Parity

Name	Address	Initial value	Type	Description
Parity_Carrier2	0x35	0x00	RO	[2:0]: received compliment data [P, 0, 1] [7:3]: reserved

13.3.26 Receiving Status and Mask

Name	Address	Initial value	Type	Description
STATUS_MASK_Carrier	0x36	0x00	RW	[7]: receiving status channel 3 [6]: receiving status channel 2 [5]: receiving status channel 1 [4]: receiving status channel 0 [3]: receive channel3 mask [2]: receive channel2 mask [1]: receive channel1 mask [0]: receive channel0 mask

13.3.27 REC_INT_STATUS

Name	Address	Initial value	Type	Description
FRec_Status	0x37	0x00	RO	[7]: reserved [6]: active high for dsss63 [5]: active high for dsss15 [4]: active high for BPSK [3]: fire program interrupt status of channel3 [2]: fire program interrupt status of channel2 [1]: fire program interrupt status of channel1 [0]: fire program interrupt status of channel0

13.3.28 Receiving SNR Calc. Status

Name	Address	Initial value	Type	Description
SNRCAL_CTRL_STATUS	0x40	0x00	RW	[7]: Force_SNR_CALC. force SNR calculation [5:4]: channel select: 00: channel 0 01: channel 1 10: channel 2 11: channel 3 [3:0]: SNR_VALID. End indication of SNR calculation set to 1 by hardware, reset to 0 by software

Note: POS and PON will be generated automatic after data frame transmission ending.

13.3.29 Receiving Signal Power

Name	Address	Initial value	Type	Description
POS[15:8]	0x41	0x00	RO	power of signal
POS[7:0]	0x42	0x00	RO	power of signal

13.3.30 Receiving Signal Noise

Name	Address	Initial value	Type	Description
PON[15:8]	0x43	0x00	RO	power of noise
PON[7:0]	0x44	0x00	RO	power of noise

13.3.31 CRC Initial Register

Name	Address	Initial value	Type	Description
CRC_INIT	0x45	0x00	RW	[0]: CRC initialization [7:1]: reserved

13.3.32 CRC Input Data

Name	Address	Initial value	Type	Description
CRC_DATAIN	0x46	0x00	RW	CRC input data

13.3.33 CRC Data

Name	Address	Initial value	Type	Description
CRC_VALUE[15:8]	0x47	0x00	RO	CRC data
CRC_VALUE [7:0]	0x48	0x00	RO	CRC data

13.3.34 RS Coding Register

Name	Address	Initial value	Type	Description
RSDATA[0]	0x4a	0x00	RW	source data for RS coding
RSDATA[1]	0x4b	0x00	RW	source data for RS coding
RSDATA[2]	0x4c	0x00	RW	source data for RS coding
RSDATA[3]	0x4d	0x00	RW	source data for RS coding
RSDATA[4]	0x4e	0x00	RW	source data for RS coding
RSDATA[5]	0x4f	0x00	RW	source data for RS coding
RSDATA[6]	0x50	0x00	RW	source data for RS coding
RSDATA[7]	0x51	0x00	RW	source data for RS coding
RSDATA[8]	0x52	0x00	RW	source data for RS coding
RSDATA[9]	0x53	0x00	RW	source data for RS coding
RSDATA[10]	0x54	0x00	RW	destination data after RS coding
RSDATA[11]	0x55	0x00	RW	destination data after RS coding
RSDATA[12]	0x56	0x00	RW	destination data after RS coding
RSDATA[13]	0x57	0x00	RW	destination data after RS coding
RSDATA[14]	0x58	0x00	RW	destination data after RS coding
RSDATA[15]	0x59	0x00	RW	destination data after RS coding
RSDATA[16]	0x5a	0x00	RW	destination data after RS coding
RSDATA[17]	0x5b	0x00	RW	destination data after RS coding
RSDATA[18]	0x5c	0x00	RW	destination data after RS coding
RSDATA[19]	0x5d	0x00	RW	destination data after RS coding

13.3.35 RS Control Register

Name	Address	Initial value	Type	Description
RS_CTRL	0x5e	0x00	RW	[7]: RS_BUF_CLR [6]: CODE_ENA [5]: DECODE_ENA [4]: CODE_OVER [3]: DECODE_OVER [2]: DECODE_ERR [1:0]: reserved

Note: The source data can be form by 1-10 bytes at RS coding. But the destination data formed by 10 bytes. If source data is less than 10 bytes, RS buffer must be cleared. The source and destination data should be transmitted together.

13.3.36 User Flash Control Register

Name	Address	Initial value	Type	Description
ADR_NVR_ADDRL	0xf0	0x00	RW	Low address
ADR_NVR_ADDRH	0xf1	0x00	RW	High address
ADR_NVR_WD	0xf2	0x00	RW	Write data
ADR_NVR_RD	0xf3	0x00	RO	Read data
ADR_NVR_CTRL	0xf4	0x00	RW	Control byte "2a", page erase "10", read "01", write

1. NVR can read and write address from 0x000 to 0x1FF, total is 512 bytes
2. Low address written first, and then written high address. The whole process can't be interrupted, otherwise the operation may fail. Advised to turn off interrupts.
3. Address increase 1 automatic.
4. CPU is in suspended state when writing operation, and recovery after completed, no need to use software delay

The sample application for reading and writing a byte

```
unsigned char ifp_nvr_read(unsigned char addr_h, unsigned char addr_l) /*using 0*/
{
    SSC_ADR = ADR_NVR_ADDRL;
    SSC_DAT = addr_l;
    SSC_ADR = ADR_NVR_ADDRH;
    SSC_DAT = addr_h;
    SSC_ADR = ADR_NVR_CTRL;
    SSC_DAT = 0x10;
    SSC_ADR = ADR_NVR_RD;
    return SSC_DAT;
}
void ifp_nvr_write(unsigned char addr_h, unsigned char addr_l, unsigned char dt) /*using 0*/
{
    SSC_ADR = ADR_NVR_ADDRL;
    SSC_DAT = addr_l;
    SSC_ADR = ADR_NVR_ADDRH;
    SSC_DAT = addr_h;
    SSC_ADR = ADR_NVR_WD;
    SSC_DAT = dt;
    SSC_ADR = ADR_NVR_CTRL;
    SSC_DAT = 0x01;
}
```

13.3.37 Write Protect Register

Name	Address	Initial value	Type	Description
ADR_WPTD	0xff	0x00	RW	write 0xff to allow CSR operation

Must write 0xFF to this register before operate expand register

EXT_ADR = ADR_WPTD;
EXT_DAT = 0xFF;