19-0517; Rev 0; 6/06

EVALUATION KIT AVAILABLE

12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

MAX19692

General Description

The MAX19692 12-bit, 2.3Gsps digital-to-analog converter (DAC) enables direct digital synthesis of high-frequency and wideband signals in baseband and higher Nyquist zones. It has been optimized for wideband communications and radar applications. It has excellent spurious and noise performance and can be used for synthesis of wideband signals in the frequency range from DC to more than 2GHz. The 2.3Gsps update rate allows digital generation of signals with more than 1GHz bandwidth. The selectable frequency response enables signal output with high SNR and excellent gain flatness in the first three Nyquist zones, reducing the number of upconversion stages needed in a radio transmitter. With its unique ability to generate broadband signals over a wide frequency range, the MAX19692 enables ultra-high data rate wireless modems and multi-standard software radio transmitters.

The MAX19692 features an update rate up to 2.3Gsps, and has four 12-bit multiplexed low-voltage differential signaling (LVDS) input ports that each operate up to 575MHz. The device accepts a clock at the DAC update rate that can be either a sine wave or a square wave. The input data rate is 1/4 the DAC update rate. The MAX19692 provides an LVDS data clock output to simplify interfacing to FPGA or ASIC devices.

The MAX19692 has three frequency response output modes:

- Non-Return-to-Zero (NRZ) mode is the most common in the industry and provides highest dynamic range and output power in the 1st Nyquist zone.
- Return-to-Zero (RZ) mode trades off SNR for improved gain flatness in the 1st, 2nd, and 3rd Nyquist zones.
- Radio Frequency (RF) mode provides higher SNR and excellent dynamic performance in the 2nd and 3rd Nyquist zones.

The MAX19692 is a current-steering DAC with an integrated, self-calibrated 50Ω differential output termination to ensure optimum dynamic performance. The MAX19692 operates from 3.3V and 1.8V power supplies and consumes 760mW at 1.0Gsps.

Applications

Radar Waveform and LO Signal Synthesis

Digital IF Generation in X-Band Transmitters

Arbitrary Waveform Generators

Direct Digital Synthesis

Automatic Test Equipment

Direct Digital Generation of Wideband RF Signals Up to 2GHz

Pin Configuration appears at end of data sheet.

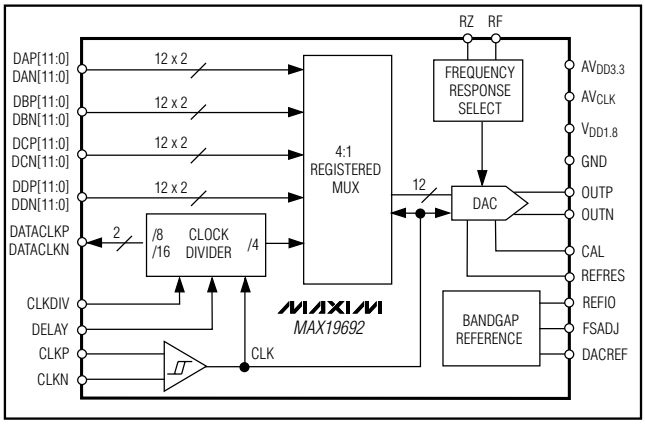
Features

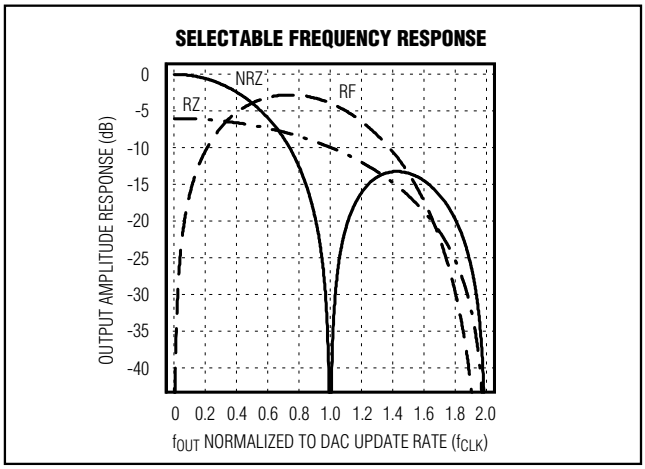
- **Industry-Leading Dynamic Performance**
  SFDR = 68dBc at f_{OUT} = 1200MHz
  Noise Density = -162dBm/Hz at 200MHz
- **1GHz Signal Bandwidth**
- **Frequency Response Modes: NRZ, RZ, RF**
- **High SNR and Exceptional Gain Flatness in Nyquist Zones 1, 2, 3**
- **4:1 Multiplexed LVDS Inputs (Up to 575MHz Each)**
- **Internal 50Ω Differential Output Termination**
- **Low Power: 760mW (f_{CLK} = 1000MHz)**
- **Compact 11mm x 11mm, 169 CSBGA Package**
- **Evaluation Kit Available (Order MAX19692EVKIT)**

Ordering Information

PART	TEMP RANGE	PACKAGE	PKG CODE
MAX19692EXW-D	-40°C to +85°C	169 CSBGA	X16911-1

Functional Diagram





For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

ABSOLUTE MAXIMUM RATINGS

$AV_{DD3.3}$ to GND, DACREF .....-0.3V to +3.9V
$V_{DD1.8}$, AV_{CLK} to GND, DACREF .....-0.3V to +2.1V
REFIO, FSADJ to GND, DACREF .....-0.3V to ($AV_{DD3.3}$ + 0.3V)
OUTP, OUTN to GND, DACREF .....-0.3V to ($AV_{DD3.3}$ + 1.0V)
CREF to GND, DACREF.....-0.3V to ($V_{DD1.8}$ + 0.3V)
DELAY, CLKDIV, RZ, RF, REFRES,
CAL to GND, DACREF.....-0.3V to ($AV_{DD3.3}$ + 0.3V)
CLKP, CLKN to GND, DACREF.....-0.3V to (AV_{CLK} + 0.3V)
DAP0–DAP11, DBP0–DBP11,
DCP0–DCP11 to GND, DACREF.....-0.3V to ($V_{DD1.8}$ + 0.3V)
DDP0–DDP11 to GND, DACREF.....-0.3V to ($V_{DD1.8}$ + 0.3V)
DAN0–DAN11, DBN0–DBN11,
DCN0–DCN11 to GND, DACREF.....-0.3V to ($V_{DD1.8}$ + 0.3V)
DDN0–DDN11 to GND, DACREF.....-0.3V to ($V_{DD1.8}$ + 0.3V)
DATACLKP, DATACLKN to GND,
DACREF .....-0.3V to ($V_{DD1.8}$ + 0.3V)
DATACLKP, DATACLKN Continuous Current 8mA
Continuous Power Dissipation (T_A = +70°C)
169-Pin CSBGA (derate 33.3mW/°C
above +70°C).....2666.7mW
Thermal Resistance θ_{JA} (Note 1).....+18°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C

Note 1: Thermal resistance based on a 4.5in x 5.5in multilayer board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($AV_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, CAL on, NRZ mode, transformer-coupled differential output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Resolution				12		Bits
Integral Nonlinearity	INL	Measured differentially		±1.3		LSB
Differential Nonlinearity	DNL	Measured differentially		±0.9		LSB
Offset Voltage Error	OS	Measured differentially, no external load resistors	-0.5	±0.1	+0.5	%FS
Offset Drift				±10		ppm/°C
Full-Scale Output Current	I_{OUT}	(Note 3)	8		20	mA
Output-Current Gain Error	GE		-4		+4	%FS
Output-Voltage Gain Drift		Internal reference		-0.003		dB/°C
		External reference		-0.0025		
Maximum Output Power	P_{OUT}	Differential, into 50Ω load		-2.6		dBm
Output Resistance	R_{OUT}	Differential, CAL ≥ 0.7 x $AV_{DD3.3}$ (Note 4)	44	48	52	Ω
DYNAMIC PERFORMANCE (Note 5)						
Minimum Output Update Rate	f_{CLK}				10	MHz
Maximum Output Update Rate	f_{CLK}	1.8V ≤ $V_{DD1.8}$ ≤ 1.9V	2300			MHz
Wideband Noise-Spectral Density		f_{CLK} = 1000MHz, f_{OUT} = 200MHz, -12dBFS		-162		dBm/Hz

ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, CAL on, NRZ mode, transformer-coupled differential output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Spurious-Free Dynamic Range within Nyquist Zone of f_{OUT}	SFDR	f_{CLK} = 500MHz	f_{OUT} = 50MHz, -6dBFS, NRZ mode		73		dBc
			f_{OUT} = 100MHz, -6dBFS, NRZ mode		74		
			f_{OUT} = 200MHz, -6dBFS, NRZ mode		70		
			f_{OUT} = 400MHz, -6dBFS, RF mode		71		
			f_{OUT} = 600MHz, -6dBFS, RF mode		73		
		f_{CLK} = 1000MHz	f_{OUT} = 200MHz, -6dBFS, NRZ mode		75		
			f_{OUT} = 409MHz, -0.1dBFS, NRZ mode, $T_A \geq$ +25°C	60	68		
			f_{OUT} = 409MHz, -0.1dBFS, NRZ mode	56	68		
			f_{OUT} = 800MHz, -6dBFS, RF mode		67		
			f_{OUT} = 1200MHz, -6dBFS, RF mode		65		
		f_{CLK} = 2000MHz, NRZ mode	f_{OUT} = 100MHz, -6dBFS		71		
			f_{OUT} = 200MHz, -6dBFS		68		
			f_{OUT} = 400MHz, -6dBFS		70		
			f_{OUT} = 800MHz, -6dBFS		58		
		f_{CLK} = 2300MHz, NRZ mode	f_{OUT} = 92MHz, 0dBFS	60	71		
2-Tone IMD	TTIMD	f_{CLK} = 1000MHz, NRZ mode	f_{OUT1} = 200MHz, -7dBFS		-72		dBc
			f_{OUT2} = 201MHz, -7dBFS				
		f_{CLK} = 1000MHz, RF mode	f_{OUT1} = 1300MHz, -7dBFS		-66		
			f_{OUT2} = 1301MHz, -7dBFS				
Minimum Output Bandwidth	BW_{-3dB}	(Note 6)			1500		MHz
REFERENCE							
Internal Reference Voltage Range	V_{REFIO}			1.1	1.2	1.3	V
Reference Input Compliance Range	$V_{REFIOCR}$			0.50		1.25	V
Reference Input Resistance	R_{REFIO}				10		kΩ
Reference Voltage Drift	TCO_{REF}				50		ppm/°C
ANALOG OUTPUT TIMING (Note 7)							
Output Fall Time	t_{FALL}	90% to 10%			270		ps
Output Rise Time	t_{RISE}	10% to 90%			270		ps
Settling Time	t_S	Settling to 0.1%			3.5		ns
		Settling to 0.025%			4.5		
Output Propagation Delay	t_{PD}	(Note 8)			0.9		ns

12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, CAL on, NRZ mode, transformer-coupled differential output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

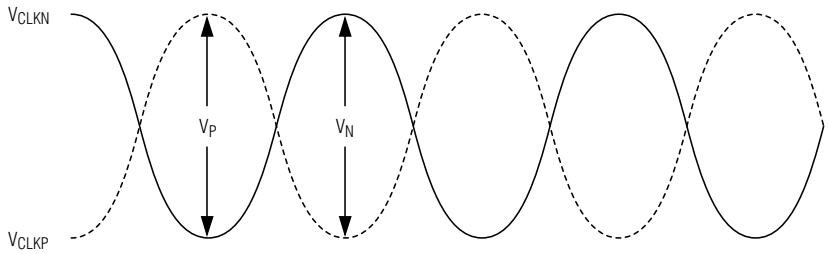
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS						
Data to Clock Setup Time	t_{SETUP}	Referenced to rising edge of data clock (Note 9)	1.6			ns
Data to Clock Hold Time	t_{HOLD}	Referenced to rising edge of data clock (Note 9)	-0.8			ns
Data Latency		(Note 10)		14		Clock cycles
LVDS LOGIC INPUTS (DAP11–DAP0, DAN11–DAN0, DBP11–DBP0, DBN11–DBN0, DCP11–DCP0, DCN11–DCN0, DDP11–DDP0, DDN11–DDN0)						
Differential Input Logic-High	V_{IH}		100			mV
Differential Input Logic-Low	V_{IL}				-100	mV
Common-Mode Voltage Range	V_{COM}		1.125		1.375	V
Differential Input Resistance	R_{IN}		85		125	Ω
Input Capacitance	C_{IN}			1.5		pF
CMOS LOGIC INPUTS (RZ, RF, CLKDIV, DELAY)						
Input Logic-High	V_{IH}		0.7 x $AV_{DD3.3}$			V
Input Logic-Low	V_{IL}				0.3 x $AV_{DD3.3}$	V
Input Leakage Current	I_{IN}		-15		+15	µA
Input Capacitance	C_{IN}			3		pF
CLOCK INPUTS (CLKP, CLKN)						
Minimum Differential Input Voltage Swing (Note 11)	V_{CLK}	f_{CLK} ≤ 1.5GHz		0.6		V_{P-P}
		f_{CLK} = 2.3GHz, see Figure 6 for dependence on f_{CLK}		2.0		
Maximum Differential Voltage Swing	V_{CLK}	(Note 11)		2.5		V_{P-P}
Differential Input Slew Rate	SR_{CLK}			6000		V/µs
Common-Mode Voltage Range	V_{COMCLK}		0.55	AV_{CLK} / 3	0.65	V
Input Resistance	R_{CLK}	Differential		100		Ω
Input Capacitance	C_{CLK}			2		pF

ELECTRICAL CHARACTERISTICS (continued)

($AV_{DD3.3}$ = 3.3V, $V_{DD1.8}$ = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, CAL on, NRZ mode, transformer-coupled differential output, I_{OUT} = 20mA, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DATA CLOCK OUTPUTS (DATACLKP, DATACLKN)						
Differential Output	V_{DCLK}	With 100Ω differential termination	±0.25	±0.35	±0.45	V
Output Rise and Fall Time	t_R, t_F	With 100Ω differential termination		0.5		ns
Common-Mode Voltage Range	V_{COM}		1.125	1.25	1.375	V
Output Resistance	R_{CLK}	Differential		100		Ω
POWER SUPPLIES						
Analog-Supply Voltage Range	$AV_{DD3.3}$		3.1	3.3	3.5	V
1.8V Supply Voltage Range	$V_{DD1.8}$	10MHz ≤ f_{CLK} < 2.0GHz (Note 9)	1.7	1.8	1.9	V
		2.0GHz ≤ f_{CLK} ≤ 2.3GHz	1.8		1.9	
Clock-Supply Voltage Range	AV_{CLK}	10MHz ≤ f_{CLK} < 2.0GHz (Note 9)	1.7	1.8	1.9	V
		2.0GHz ≤ f_{CLK} ≤ 2.3GHz	1.8		1.9	
Analog Supply Current	$I_{AVDD3.3}$	f_{CLK} = 1000MHz, f_{OUT} = 10MHz, A_{OUT} = 0dBFS		107	117	mA
Digital Supply Current	$I_{VDD1.8}$	f_{CLK} = 1000MHz, f_{OUT} = 10MHz, A_{OUT} = 0dBFS		61	76	mA
Clock Supply Current	I_{AVCLK}	f_{CLK} = 1000MHz, f_{OUT} = 10MHz, A_{OUT} = 0dBFS		164	191	mA
Total Power Dissipation	P_{DISS}	f_{CLK} = 1000MHz, f_{OUT} = 10MHz, A_{OUT} = 0dBFS		760	870	mW

Note 2: All specifications are 100% tested at T_A ≥ +25°C. Specifications at T_A < +25°C are guaranteed by design and characterization.
Note 3: Nominal full-scale current I_{OUT} = 32 x I_{REF}.
Note 4: R_{OUT} can be set to 50Ω as described in the *Output Resistor Calibration* section.
Note 5: CLK input = +10dBm, AC-coupled sine wave.
Note 6: Excludes impulse-response dependent rolloff inherent in the DAC. Measured single-ended into 50Ω termination resistor.
Note 7: Measured differentially into a 50Ω termination resistor.
Note 8: Excludes data latency.
Note 9: Guaranteed by design and characterization.
Note 10: DA_P/DA_N to DAC output.
Note 11: Differential voltage swing defined as $|V_P| + |V_N|$.

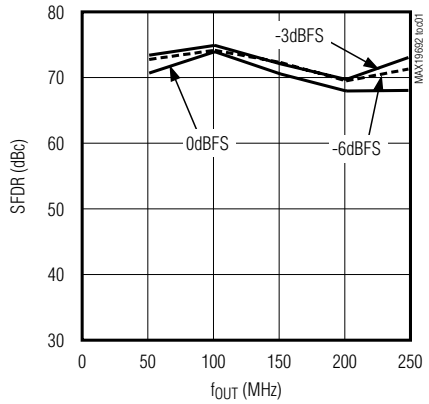


12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

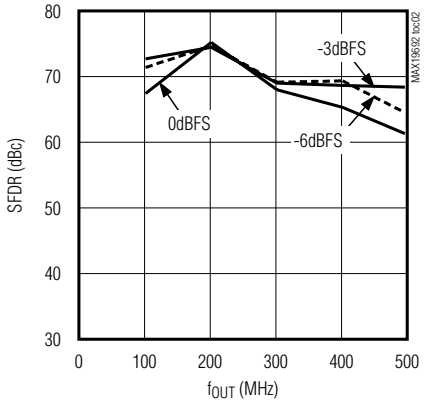
Typical Operating Characteristics

($AV_{DD3.3}$ = 3.3V, $AV_{DD1.8}$ = DV_{DD} = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, CAL on, transformer-coupled differential output, I_{OUT} = 20mA, T_A = +25°C, unless otherwise noted.)

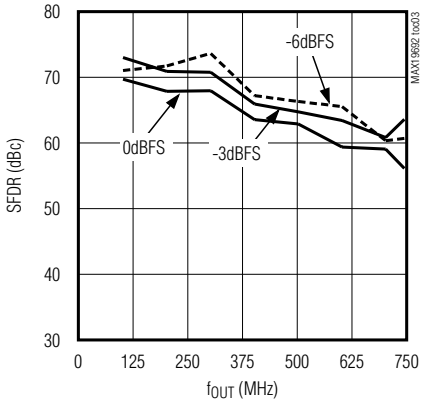
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 500MHz, NRZ MODE



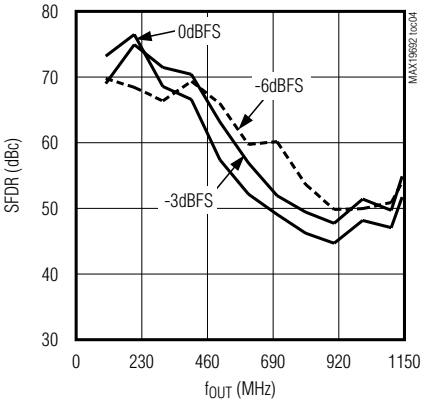
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 1000MHz, NRZ MODE



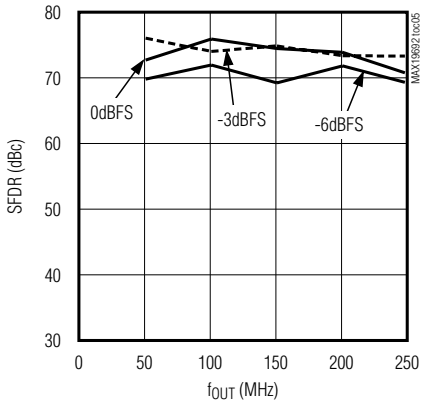
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 1500MHz, NRZ MODE



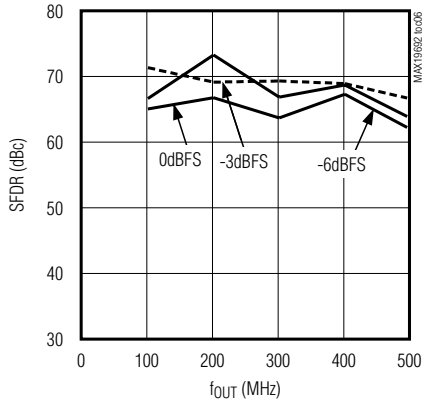
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 2300MHz, NRZ MODE



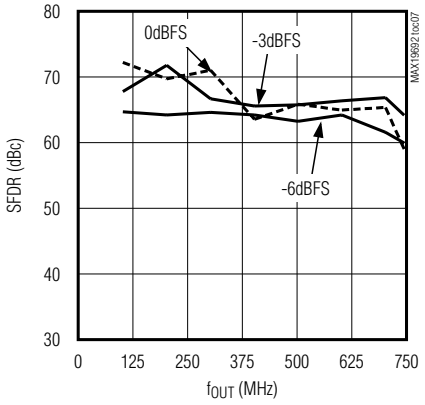
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 500MHz, RZ MODE



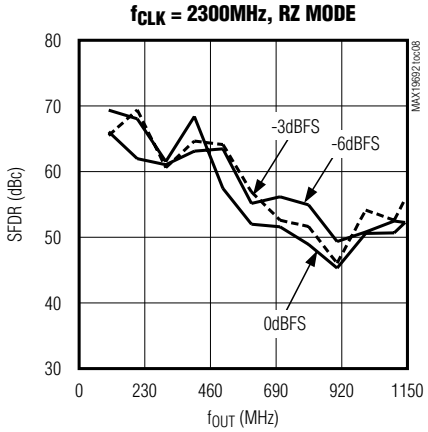
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 1000MHz, RZ MODE



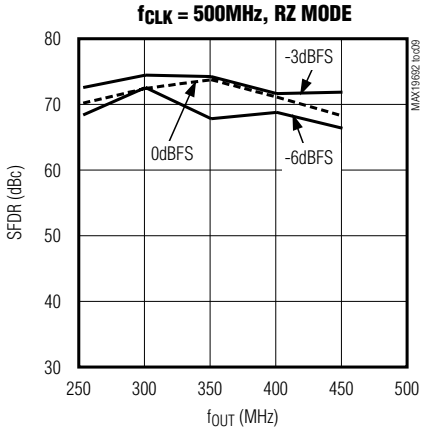
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 1500MHz, RZ MODE



SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 2300MHz, RZ MODE



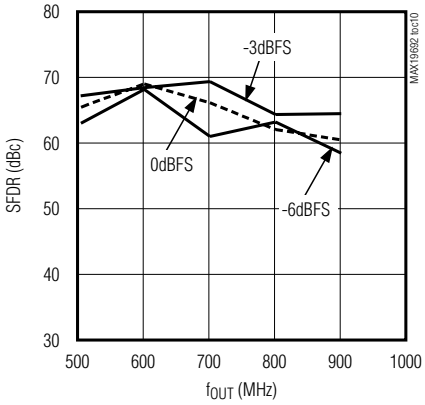
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 500MHz, RZ MODE



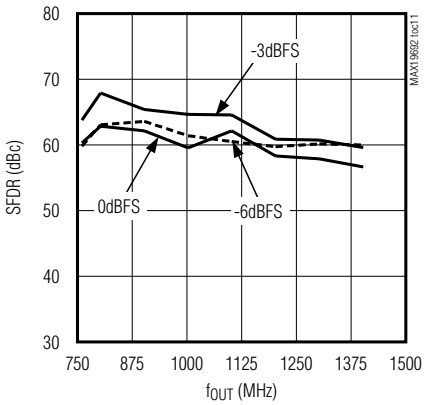
Typical Operating Characteristics (continued)

($AV_{DD3.3}$ = 3.3V, $AV_{DD1.8}$ = DV_{DD} = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, CAL on, transformer-

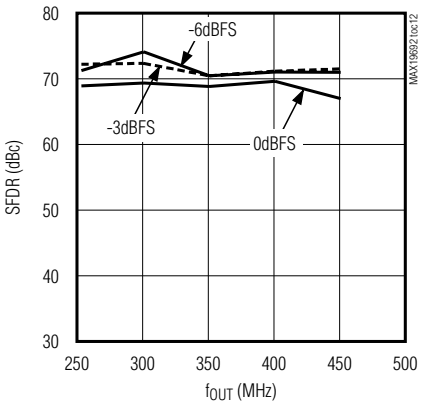
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 1000MHz, RZ MODE



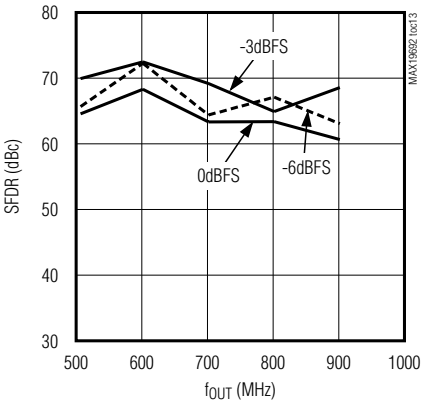
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 1500MHz, RZ MODE



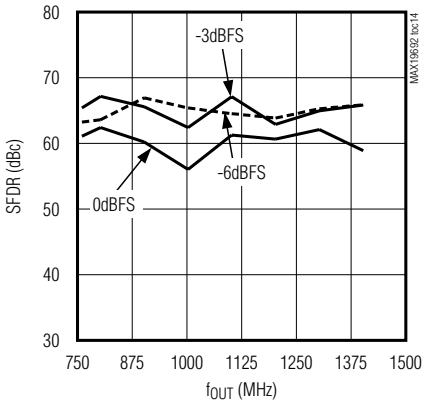
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 500MHz, RF MODE



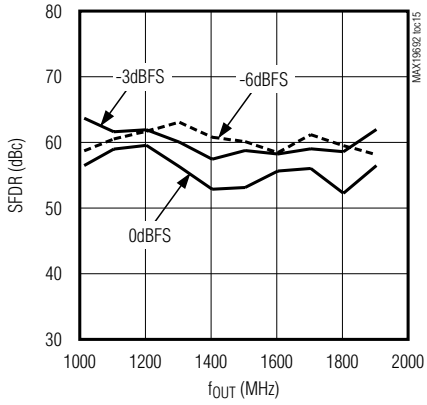
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 1000MHz, RF MODE



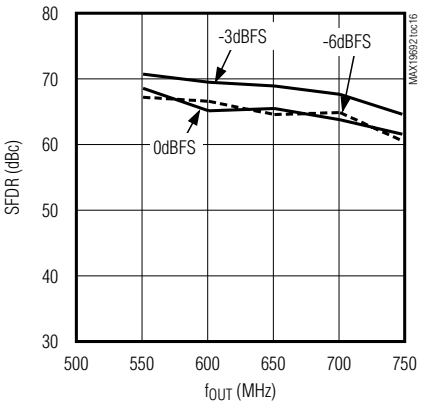
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 1500MHz, RF MODE



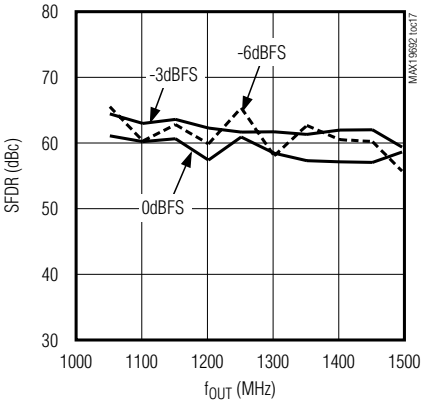
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 2000MHz, RF MODE



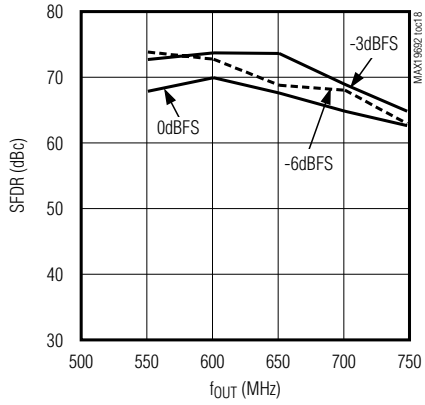
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 500MHz, RZ MODE



SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 1000MHz, RZ MODE



SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 500MHz, RF MODE

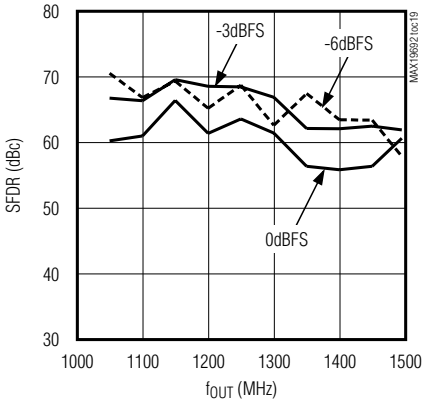


12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

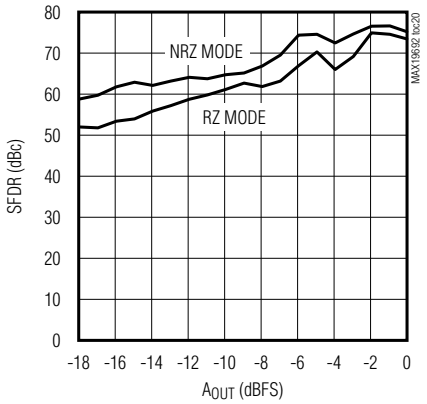
Typical Operating Characteristics (continued)

($AV_{DD3.3}$ = 3.3V, $AV_{DD1.8}$ = DV_{DD} = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, CAL on, transformer-coupled differential output, I_{OUT} = 20mA, T_A = +25°C, unless otherwise noted.)

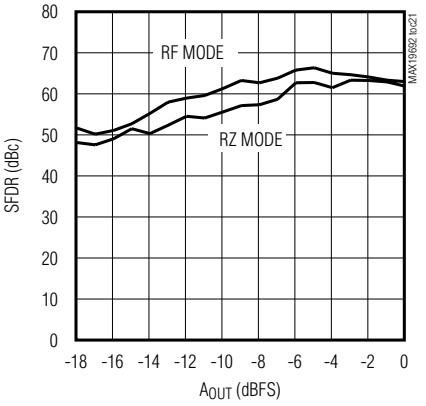
SFDR vs. OUTPUT FREQUENCY
f_{CLK} = 1000MHz, RF MODE



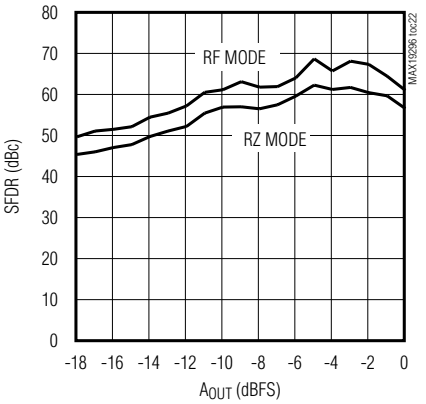
SFDR vs. OUTPUT AMPLITUDE
f_{CLK} = 1000MHz, f_{OUT} = 200MHz



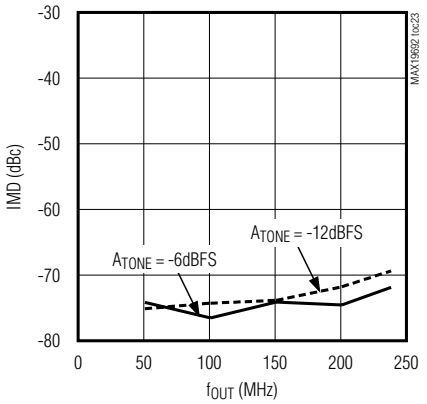
SFDR vs. OUTPUT AMPLITUDE
f_{CLK} = 1000MHz, f_{OUT} = 800MHz



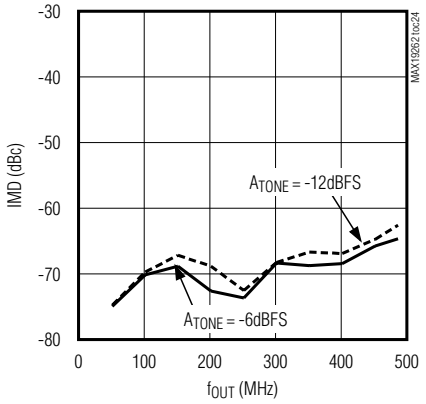
SFDR vs. OUTPUT AMPLITUDE
f_{CLK} = 1000MHz, f_{OUT} = 1200MHz



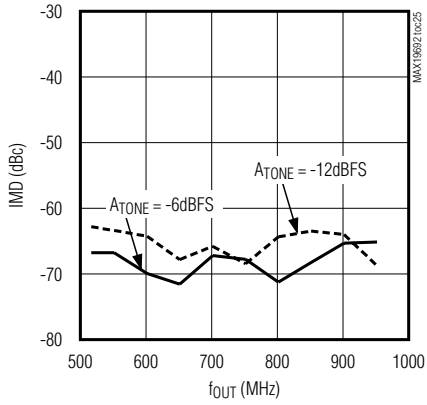
TWO-TONE IMD vs. OUTPUT FREQUENCY
f_{CLK} = 500MHz, 1MHz SPACING, NRZ MODE



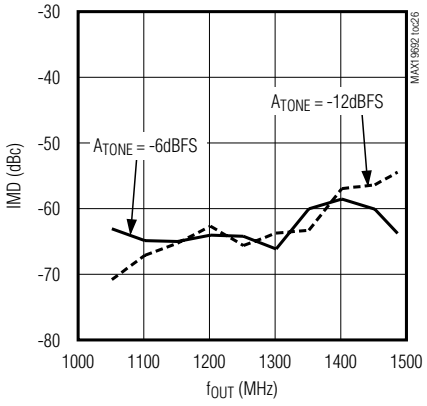
TWO-TONE IMD vs. OUTPUT FREQUENCY
f_{CLK} = 1000MHz, 1MHz SPACING, NRZ MODE



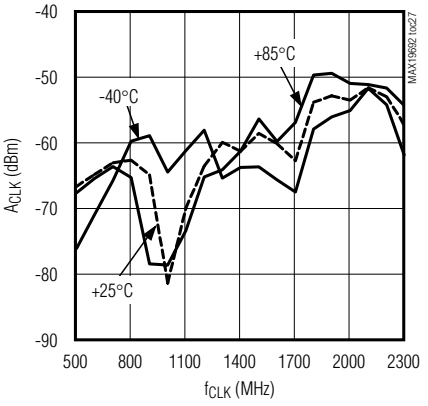
TWO-TONE IMD vs. OUTPUT FREQUENCY
f_{CLK} = 1000MHz, 1MHz SPACING, RF MODE



TWO-TONE IMD vs. OUTPUT FREQUENCY
f_{CLK} = 1000MHz, 1MHz SPACING, RF MODE



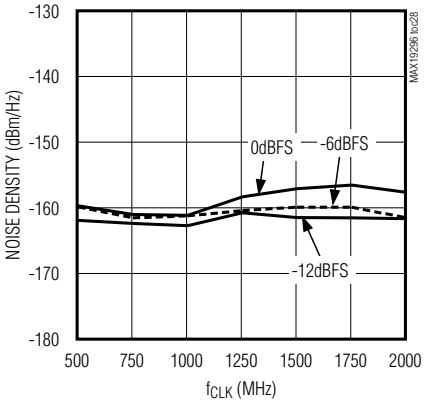
CLK FEEDTHROUGH vs. CLK FREQUENCY
f_{OUT} = 200MHz, A_{OUT} = -1dBFS, NRZ MODE



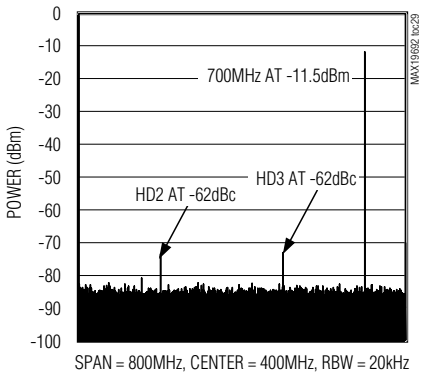
Typical Operating Characteristics (continued)

($AV_{DD3.3}$ = 3.3V, $AV_{DD1.8}$ = DV_{DD} = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, CAL on, transformer-coupled differential output, I_{OUT} = 20mA, T_A = +25°C, unless otherwise noted.)

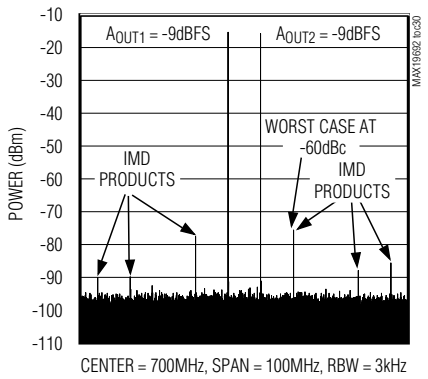
OUTPUT NOISE DENSITY vs. CLK FREQUENCY
f_{OUT} = 200MHz, NRZ MODE



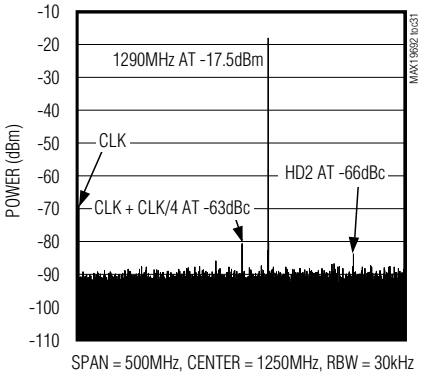
SFDR SPECTRAL PLOT
f_{CLK} = 1600MHz, f_{OUT} = 700MHz, A_{OUT} = -3dBFS, NRZ MODE



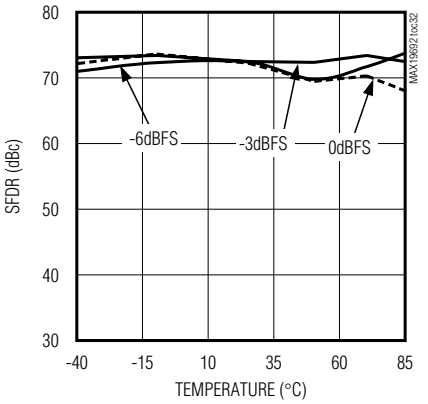
TWO-TONE IMD SPECTRAL PLOT
f_{CLK} = 1600MHz, f_{OUT} = 695MHz, f_{OUT2} = 705MHz



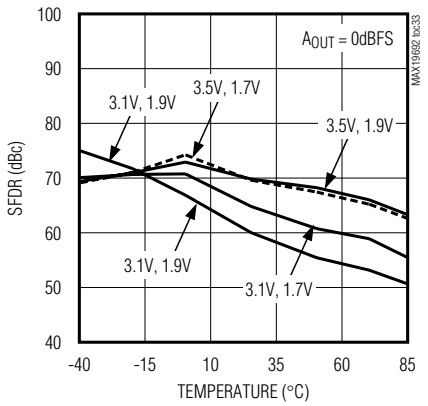
SFDR SPECTRAL PLOT, 3rd NYQUIST ZONE
f_{CLK} = 1000MHz, f_{OUT} = 1290MHz, A_{OUT} = -3dBFS, RF MODE



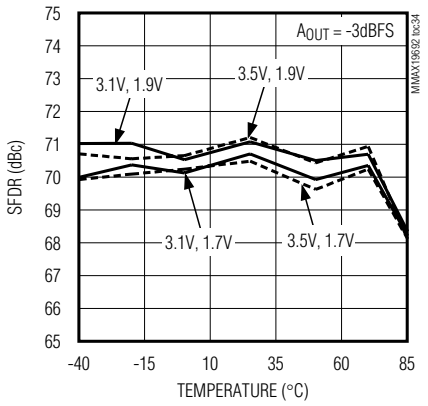
SFDR vs. TEMPERATURE
f_{CLK} = 1000MHz, f_{OUT} = 200MHz, NRZ MODE



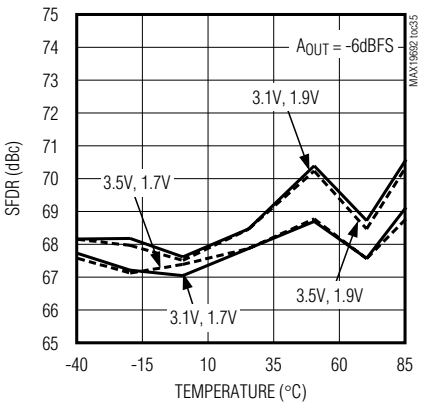
SFDR vs. TEMPERATURE ($AV_{DD3.3}$, 1.8V SUPPLIES)
f_{CLK} = 2000MHz, f_{OUT} = 400MHz, NRZ MODE



SFDR vs. TEMPERATURE ($AV_{DD3.3}$, 1.8V SUPPLIES)
f_{CLK} = 2000MHz, f_{OUT} = 400MHz, NRZ MODE



SFDR vs. TEMPERATURE ($AV_{DD3.3}$, 1.8V SUPPLIES)
f_{CLK} = 2000MHz, f_{OUT} = 400MHz, NRZ MODE

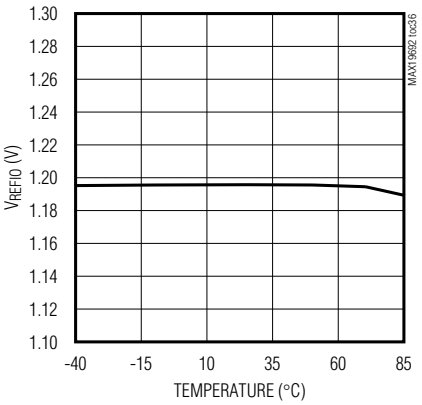


12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

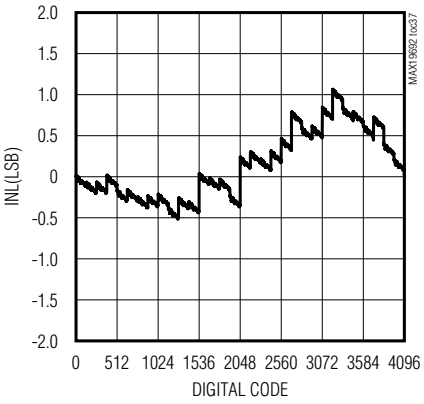
Typical Operating Characteristics (continued)

($AV_{DD3.3}$ = 3.3V, $AV_{DD1.8}$ = DV_{DD} = AV_{CLK} = 1.8V, R_{REFRES} = 500Ω, R_{SET} = 2kΩ, V_{REFIO} = external 1.25V, CAL on, transformer-coupled differential output, I_{OUT} = 20mA, T_A = +25°C, unless otherwise noted.)

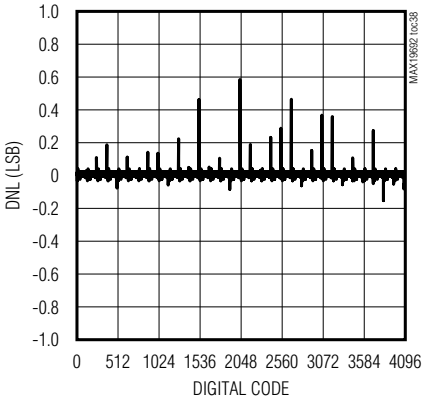
INTERNAL REFERENCE (REFIO) VOLTAGE vs. TEMPERATURE



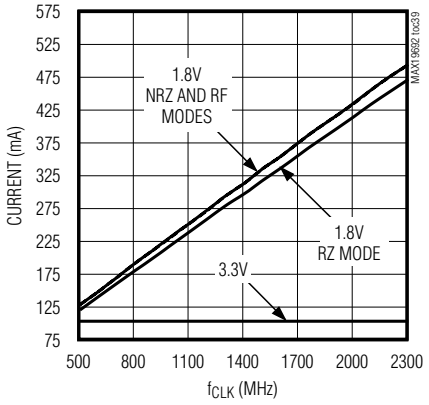
INTEGRAL NONLINEARITY vs. DIGITAL CODE



DIFFERENTIAL NONLINEARITY vs. DIGITAL CODE



SUPPLY CURRENT vs. CLK FREQUENCY f_{OUT} = 100MHz, A_{OUT} = 0dBFS, NRZ MODE



Pin Description

PIN	NAME	FUNCTION
A1	REFIO	Reference Input/Output. Output pin for the internal 1.2V-bandgap reference. REFIO has a 10kΩ series resistance and can be driven using an external reference. Connect a 1µF capacitor between REFIO and DACREF.
A2	FSADJ	Full-Scale Adjust Input. Sets the full-scale output current of the DAC. For a 20mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF.
A3	DACREF	Current-Set Resistor Return Path. For a 20mA full-scale output current, connect a 2kΩ resistor between FSADJ and DACREF. DACREF is internally connected to AGND. **DO NOT CONNECT TO EXTERNAL GROUND.**
A4, A5, A7, A9	$AV_{DD3.3}$	Analog 3.3V Supply Voltage. Accepts a 3.1V to 3.5V supply voltage range. Connect 47nF bypass capacitors between each $AV_{DD3.3}$ pin and AGND.
A6	OUTP	Positive Terminal of Differential DAC Output. OUTP has a calibrated internal 25Ω resistor to $AV_{DD3.3}$.
A8	OUTN	Negative Terminal of Differential DAC Output. OUTN has a calibrated internal 25Ω resistor to $AV_{DD3.3}$.
A10, B10, C2, C3, C10, E1–E4, E10–E13, F13	$V_{DD1.8}$	Analog 1.8V Supply Voltage. Accepts a 1.7V to 1.9V supply voltage range. Connect 47nF bypass capacitors between each $V_{DD1.8}$ pin and GND.
A11, A13, B5–B9, B11, C4–C9, C11, D1–D11, D13, E5–E9, G13, M13	GND	Ground. Connect to ground plane with minimum inductance.
A12, B12, C12, D12	AV_{CLK}	Clock 1.8V Supply Voltage. Accepts a 1.7V to 1.9V supply voltage range. Connect 47nF bypass capacitors between AV_{CLK} and GND.
B1	CREF	Noise Bypass Pin. A 1µF capacitor between the CREF and DACREF band limits the phase noise of the MAX19692.
B2	REFRES	Calibration Reference Resistor Input. Connect a 500Ω resistor between REFRES and $AV_{DD3.3}$. The internal analog output resistors are calibrated to this external resistor.
B3	RZ	Return-to-Zero (RZ) Mode-Select Input. RZ = 0 (and RF = 0): Normal DAC (NRZ) operation (default). RZ = 1 (and RF = 0): Return-to-zero (RZ) DAC operation. RZ is a 3.3V CMOS logic input with an internal pulldown resistor.
B4	RF	Radio Frequency (RF) Mode-Select Input. RF = 0: NRZ or RZ DAC operation. RF = 1 (and RZ = 0): RF DAC operation. RF is a 3.3V CMOS logic input with internal pulldown resistor.
C13	CLKP	LVDS-Compatible Converter Clock Input. There is an internal 100Ω termination resistor between CLKP and CLKN.
B13	CLKN	LVDS-Compatible Converter Clock Input. There is an internal 100Ω termination resistor between CLKP and CLKN.
C1	CAL	DAC Output Resistance Calibration Input. Calibration of the internal output resistors is initiated by a rising edge on CAL. CAL = 1: Output resistors are calibrated. CAL = 0: Output resistors are uncalibrated. CAL is a 3.3V CMOS input with an internal pulldown resistor. Leakage current is less than ±15µA.

12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

Pin Description (continued)

PIN	NAME	FUNCTION
F6–F3, F1, F2, H6–H1	DAP11–DAP0	Positive Terminals of A-Channel LVDS Data Inputs. DAP11 is MSB. Offset binary format.
G6–G3, G1, G2, J6–J1	DAN11–DAN0	Negative Terminals of A-Channel LVDS Data Inputs
K1–K4, M1–M4, K5, M5, K6, M6	DBP11–DBP0	Positive Terminals of B-Channel LVDS Data Inputs. DBP11 is MSB. Offset binary format.
L1–L4, N1–N4, L5, N5, L6, N6	DBN11–DBN0	Negative Terminals of B-Channel LVDS Data Inputs
M7, K7, M8, K8, M9–M12, K9, K10, K11, L12	DCP11–DCP0	Positive Terminals of C-Channel LVDS Data Inputs. DCP11 is MSB. Offset binary format.
N7, L7, N8, L8, N9–N12, L9, L10, L11, K12	DCN11–DCN0	Negative Terminals of C-Channel LVDS Data Inputs
G7, J7, J12–J8, G12–G8	DDP11–DDP0	Positive Terminals of D-Channel LVDS Data Inputs. DDP11 is MSB. Offset binary format.
F7, H7, H12–H8, F12–F8	DDN11–DDN0	Negative Terminals of D-Channel LVDS Data Inputs
J13	DATACLKP	Positive Terminal of LVDS Data Output Clock
H13	DATACLKN	Negative Terminal of LVDS Data Output Clock
K13	DELAY	Data Clock Delay Mode Input. Adjusts the delay of the output data clock. DELAY = 0: No delay added. DELAY = 1: Add delay of 1/2 input data period (2 DAC clock cycles). DELAY is a 3.3V CMOS input with an internal pulldown resistor.
L13	CLKDIV	Data Clock Divide Mode Input. CLKDIV = 1: Data clock rate = input data rate / 2 (f_{CLK} / 8). CLKDIV = 0: Data clock rate = input data rate / 4 (f_{CLK} / 16). CLKDIV is a 3.3V CMOS input with an internal pulldown resistor.
N13	N.C.	No Connection. This pin should be left unconnected.

Detailed Description

The MAX19692 is a high-performance, high-speed, 12-bit current-steering DAC with an integrated 50Ω differential output termination. The DAC is capable of operating with clock speeds up to 2.3GHz. The converter consists of an edge-triggered 4:1 input data multiplexer followed by a current-steering circuit. This circuit is capable of generating differential full-scale currents in the 8mA to 20mA range. Internal 25Ω resistors on each output, in combination with an external termination, convert the differential current into a voltage. The internal resistors are terminated to the 3.3V analog supply, $AV_{DD3.3}$. The internal termination resistors can be calibrated to an external 500Ω precision resistor. A calibration cycle can be run every time the converter is powered up, or at any other time. An integrated 1.2V-bandgap reference, control amplifier, and user-selectable external resistor determine the data converter's full-scale range. The converter features selectable frequency response to allow application-dependent optimization of output power and gain flatness. Three responses can be selected: non-return-to-zero (NRZ), return-to-zero (RZ), or radio frequency (RF).

Reference Input/Output

The MAX19692 supports operation with the on-chip 1.2V-bandgap reference or an external reference voltage source. REFIO serves as the input for an external, low-impedance reference source, and as the output if the DAC is operating with the internal reference. For stable operation with the internal reference, REFIO should be decoupled to DACREF with a 1µF capacitor. REFIO must be buffered with an external amplifier if heavier loading is required, due to its 10kΩ series resistance.

The MAX19692's reference circuit (Figure 1) employs a control amplifier, designed to regulate the full-scale current I_{OUT} for the differential current outputs of the DAC. The output current can be calculated as follows:

$$I_{OUT} = 32 \times I_{REF} \times 4095/4096$$

where I_{REF} is the reference output current ($I_{REF} = V_{REFIO} / R_{SET}$) and I_{OUT} is the full-scale output current of the DAC. Located between FSADJ and DACREF, R_{SET} is typically set to 2kΩ, which results in a full-scale current of 20mA if the internal reference is used.

12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

Analog Outputs

The MAX19692 is a differential current-steering DAC with built-in self-calibrated output termination resistors to optimize performance. The outputs are terminated to $AV_{DD3.3}$, and are calibrated to provide a 50Ω differential output resistance. In addition to the signal current, a constant 10mA current sink is connected to each DAC output. Typically, the outputs should be used with a 50Ω transformer. If the transformer is center tapped, it is recommended that the center tap be connected to $AV_{DD3.3}$. If the transformer is not center tapped, bias tees or RF chokes can be used to pull up the outputs. Figure 2 shows an equivalent circuit of the internal output structure of the MAX19692.

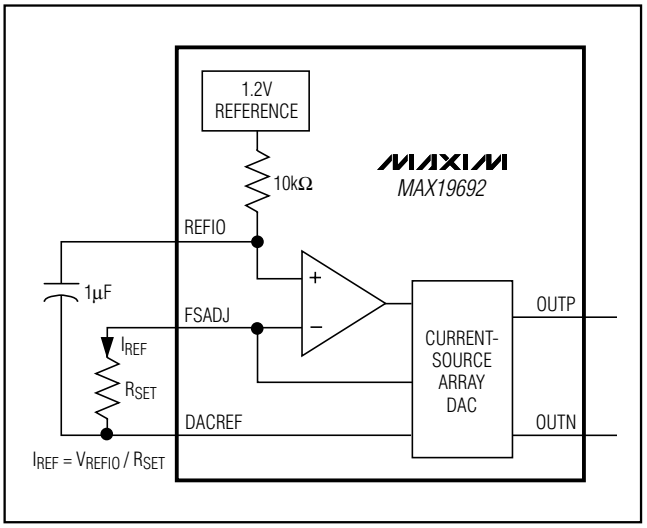


Figure 1. Reference Architecture, Internal Reference Configuration

The termination resistors, R_T, are calibrated to 23.5Ω. $R_M = R_{M1} + R_{M2} + R_{M3}$ is resistance associated with the DAC output traces and bond wires, and is not calibrated. The output resistance is equal to $2R_T + 2R_M$, and is nominally 50Ω. The MAX19692 is normally used with an external differential 50Ω load, R_L. For this case, the peak differential output voltage is calculated as:

$$V_{OUT} = I_{OUT} \times \frac{R_L R_T}{R_L + 2R_M + 2R_T}$$

where I_{OUT} is the full-scale current, which is typically set to 20mA. With R_L = 50Ω, R_T = 23.5Ω, and R_M = 1.5Ω, V_{OUT} = 0.235V is found. This corresponds to an output power of -2.6dBm. As shown in Figure 2, the output circuit has some resistive, capacitive, and inductive elements. These elements limit the output bandwidth to 2GHz with a resistive differential 50Ω load.

Output Resistor Calibration

The integrated termination resistors, R_T, must be calibrated to have an accurately known DAC output resistance and an accurately known DAC output voltage.

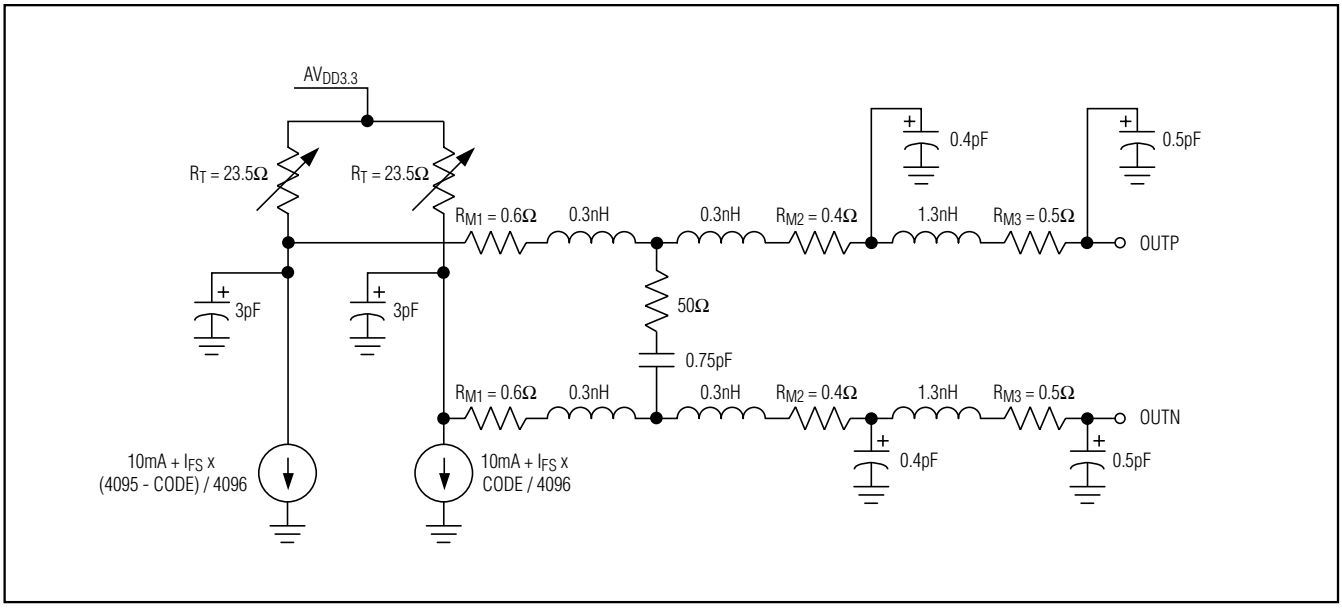


Figure 2. Equivalent Output Circuit

12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

The termination resistors are calibrated to the external reference resistor, R_{REFRES}, which should be connected between REFRES (pin B2) and $AV_{DD3.3}$. R_{REFRES} is nominally 500Ω. A plot showing the typical relation between the DAC output resistance and R_{REFRES} is shown in Figure 3.

The calibration cycle is initiated with a rising edge on the CAL pin. The CAL pin must be asserted after the supply voltages and the reference voltage have reached steady state. Input data should not be switching while calibration is running. The duration of the calibration cycle is shorter than 65,536 DAC clock cycles—which is less than 65.6µs if the converter is operated with a 1GHz clock rate. The CAL pin must be held high for the output resistors to remain calibrated. If the clock is stopped, or if power is cycled, a new calibration cycle must be run.

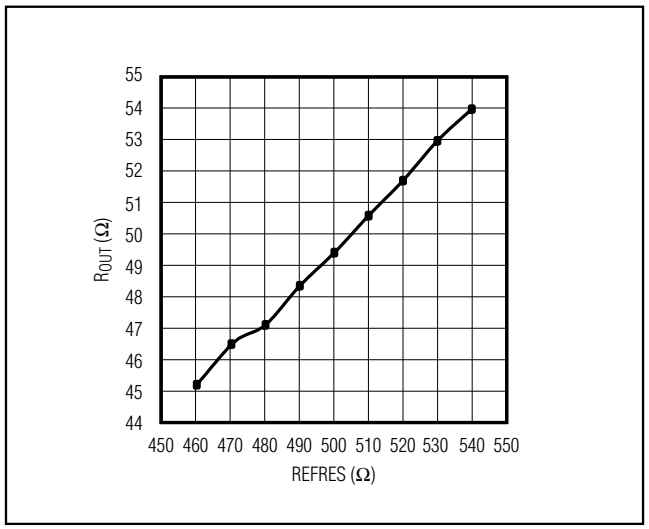


Figure 3. Output Resistance vs. REFRES Resistor

DAC Impulse/Frequency Response Selection

The MAX19692 has three impulse/frequency response modes. These are set with the RZ and RF input pins as described in Table 1.

The impulse responses of the three operating modes are shown in Figure 4. The sample period is equal to T. The default operating mode of the MAX19692 is NRZ mode. The sinc (sine(x)/x) response has zeros at every multiple of the DAC update frequency $f_{CLK} = 1/T$. Using this impulse response, the frequency response of the DAC has the familiar sinc shape:

$$A_{NRZ} = A_0\left[\frac{\sin(\pi f_{OUT}T)}{\pi f_{OUT}T}\right]$$

where f_{OUT} is the DAC output frequency, $T = 1/f_{CLK}$ is the period of the DAC clock, and A_0 is the peak low-frequency output amplitude.

In RZ mode, the DAC output has a 50% duty cycle. The DAC output stays at midscale for the remaining 50% of the clock cycle. The resulting frequency response is:

$$A_{RZ} = \frac{A_0}{2}\left[\frac{\sin(\pi f_{OUT}T/2)}{\pi f_{OUT}T/2}\right]$$

Table 1. RZ and RF Input Truth Table

RZ	RF	FREQUENCY RESPONSE MODE
0	0	NRZ
1	0	RZ
0	1	RF
1	1	Do not use

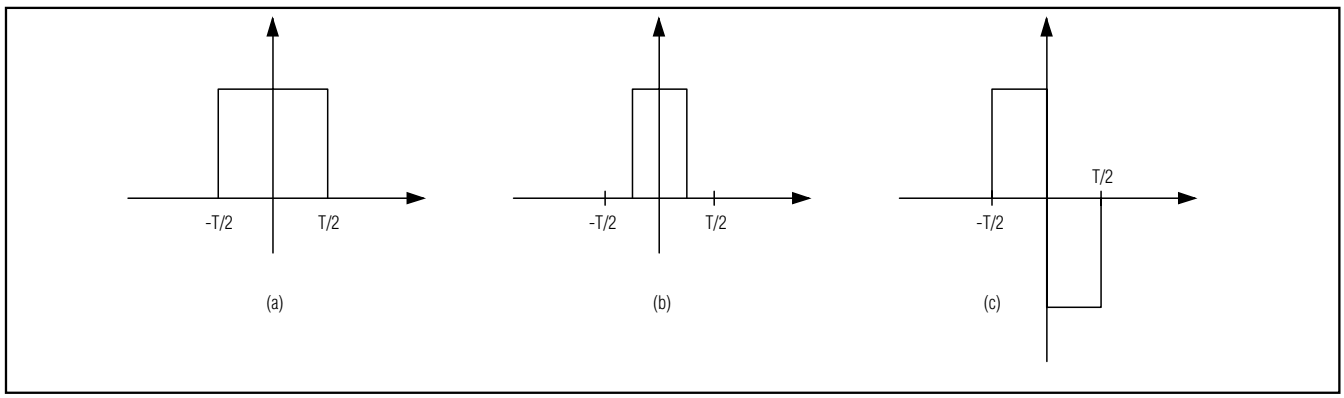


Figure 4. Impulse Responses in (a) NRZ Mode, (b) RZ Mode, and (c) RF Mode

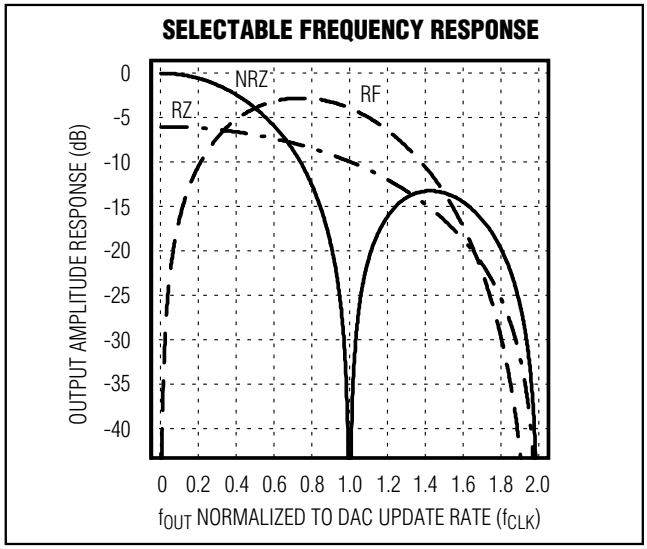


Figure 5. Amplitude Responses for NRZ Mode (Solid Line), RZ Mode (Dash-Dot Line), and RF Mode (Dashed Line). Excludes output bandwidth limitation.

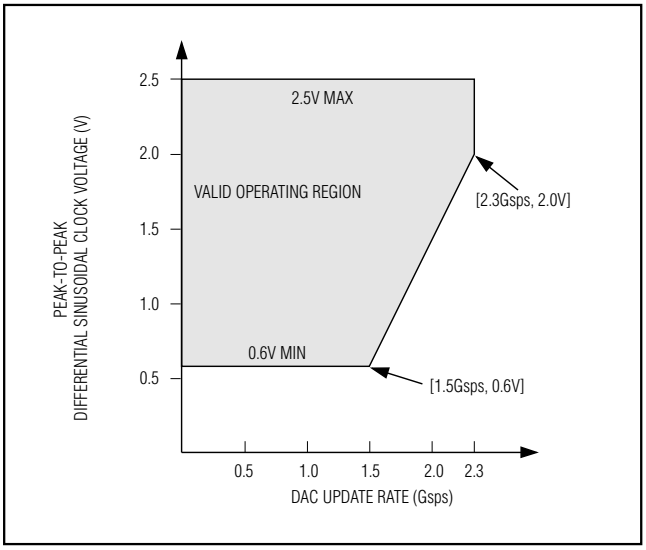


Figure 6. Recommended Clock Amplitude

This frequency response is flatter than the NRZ response in the three first Nyquist zones, particularly in the 2nd and 3rd Nyquist zones—making this DAC usable for outputting wideband signals in the 2nd and 3rd Nyquist zones.

The third mode of operation is the RF mode. In this mode, the DAC output response is inverted in the second half of the clock cycle, resulting in a doublet pulse at the output of the DAC in every clock cycle. The resulting DAC frequency response is:

$$A_{RF} = A_0 \left[\frac{\sin(\pi f_{OUT} T / 2)}{\pi f_{OUT} T / 2} \times \sin(\pi f_{OUT} T / 2) \right]$$

The RF mode increases the DAC output power in the second and third Nyquist zones and attenuates it in the first Nyquist zone.

The frequency responses for the three modes of operation are plotted in Figure 5.

NRZ mode provides the highest power in the first Nyquist zone. RZ mode provides the flattest frequency response in the first and third Nyquist zones, and RF mode provides superior output power in the second and third Nyquist zones, as well as the flattest gain in the second Nyquist zone.

Clock Inputs

The MAX19692 features a flexible differential clock input (CLKP, CLKN) operating from a separate supply (AV_{CLK}) to achieve the best possible jitter performance. The two clock inputs can be driven from a single-ended or a differential clock source. A sine wave or a square wave can be used. For single-ended operation, CLKP should be driven by a logic source, while CLKN should be bypassed to GND with a 0.1µF capacitor.

Driving the clocks differentially is recommended for optimum jitter performance. Choose a clock amplitude that is as large as possible (without the clock voltage at the CLKN and CLKP pins going more than 200mV below ground or above the AV_{CLK} supply voltage) to minimize jitter. This results in the most accurate duty cycle—and hence the most accurate gain in RZ and RF modes. For an AC-coupled, differential sine-wave clock, the clock amplitude should not be higher than 2.5V peak-to-peak (12dBm if terminated in 50Ω). The typical performance plots in this data sheet have generally been measured using a 10dBm ($2V_{P-P}$) clock amplitude.

The MAX19692 can be used with a sinusoidal clock amplitude as low as $0.6V_{P-P}$ below 1.5Gsps. For higher update rates, the clock amplitude should stay within the operating region specified in Figure 6.

The CLKP and CLKN pins are internally biased to 0.6V with resistors. This allows the user to AC-couple clock sources directly to the device without external resistors to define the DC level.

12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

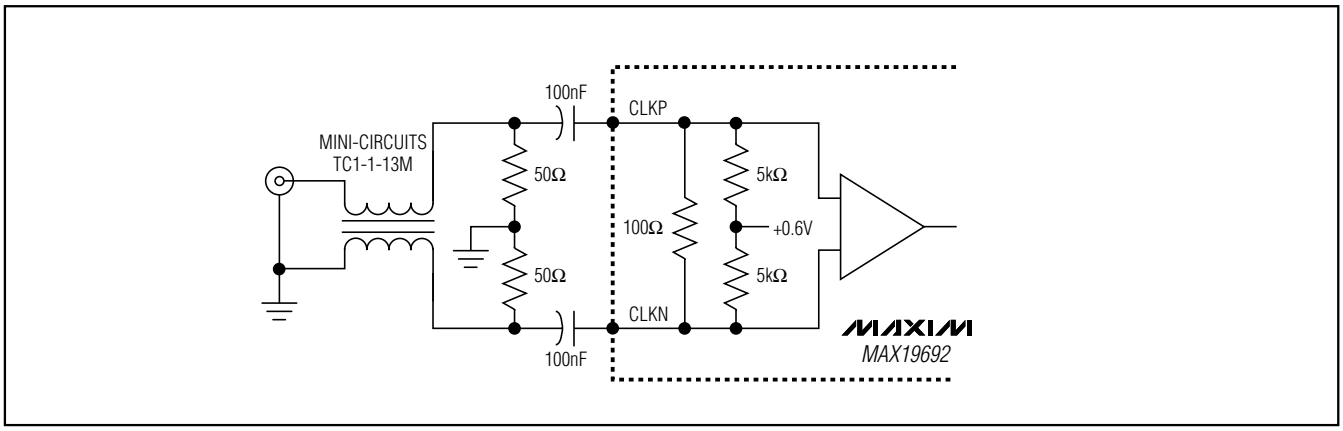


Figure 7. Typical Clock Application Circuit

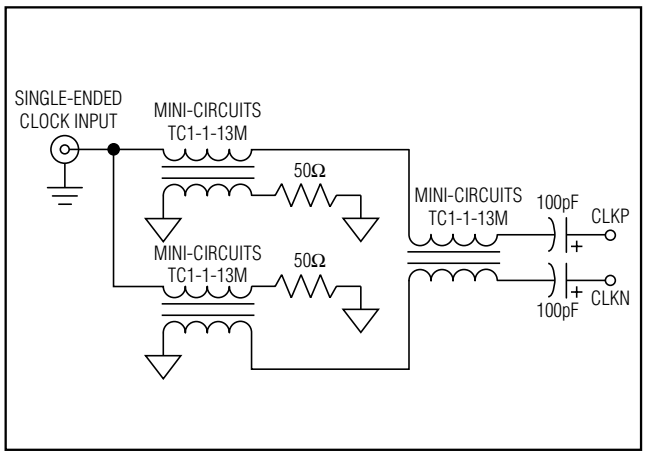


Figure 8. Clock Application Circuit with Improved Symmetry

The MAX19692 has an internal 100Ω termination resistor between CLKP and CLKN. An extra 100Ω differential termination resistor should be added if using a 50Ω clock source. See Figure 7 for a convenient and quick way to apply a differential signal created from a single-ended source and a wideband transformer.

The clock circuit in Figure 7 has some amplitude asymmetry at update rates above 1Gsps, due to transformer loss. This may cause performance degradation for some operating conditions. A clock interface circuit with improved symmetry using three balun transformers is shown in Figure 8. This clock interface circuit provides symmetric and balanced clock signals for frequencies up to the maximum update rate of the MAX19692.

An equivalent circuit model for the clock inputs is shown in Figure 9.

Clock Duty Cycle

The duty cycle of the converter clock should be close to 50%. If an AC-coupled sine-wave clock is used, the clock duty cycle is automatically close to 50%. If a square-wave clock is used, this is not necessarily the case.

Keeping the clock duty cycle close to 50% is particularly important when operating in RZ and RF modes.

When operating in RZ mode, clock duty-cycle deviation from 50% distorts the converter's frequency response. A clock duty cycle above 50% increases the converter's output power at low frequencies, and lowers the frequency of the zero in the frequency response function—effectively producing a frequency response between that of NRZ and RZ modes.

When operating in RF mode, a clock duty cycle higher or lower than 50% increases the output amplitude at low frequencies in the first Nyquist zone and slightly lowers the output amplitude in the second and third Nyquist zones.

Data Inputs

Data inputs (DAP[11:0], DAN[11:0], DBP[11:0], DBN[11:0], DCP[11:0], DCN[11:0], DDP[11:0], DDN[11:0]) have LVDS receivers followed by edge-triggered flip flops. Four 12-bit buses accept data in offset binary format. The LVDS inputs feature on-chip termination with differential 100Ω resistors. A 1.25V common-mode level with a ±400mV differential swing can be applied to these inputs. See Figure 10 for an equivalent circuit of the LVDS inputs.

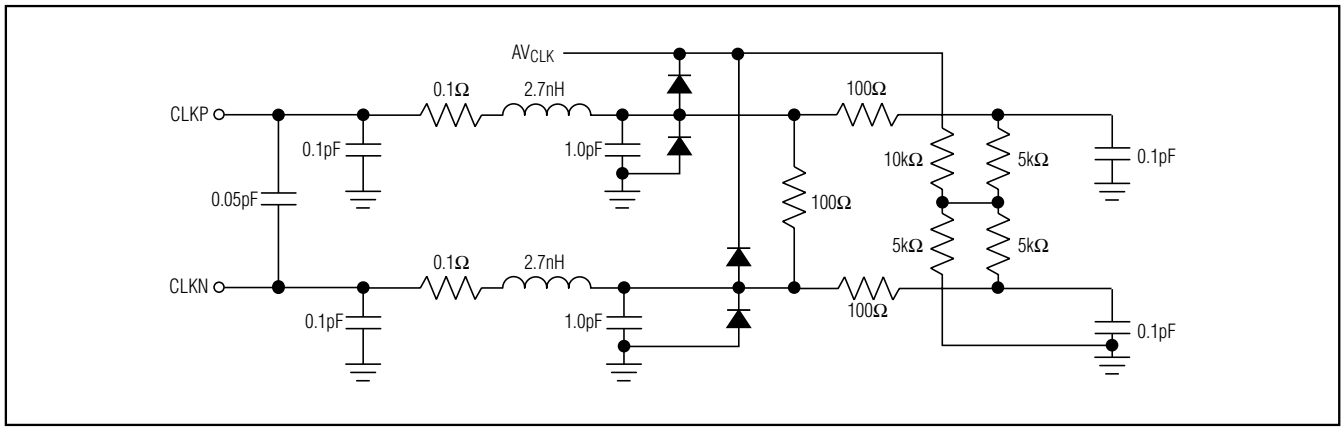


Figure 9. Clock Input Equivalent Circuit

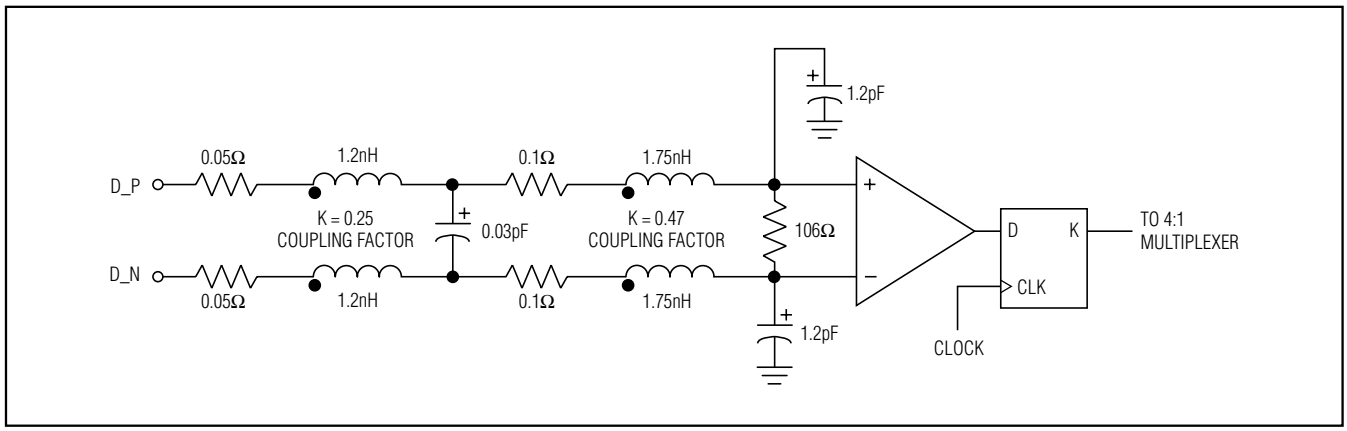


Figure 10. LVDS Input Equivalent Circuit

Data-Timing Relationships

The timing of the LVDS inputs is defined with respect to the LVDS output DATACLK (DATACLKP - DATACLKN). The LVDS data inputs are latched at 1/4 the input clock frequency. The DATACLK output frequency is divided by another factor of 4 (CLKDIV = 0) or by 2 (CLKDIV = 1).

Define the 0° point of DATACLK as the rising edge.

For the case of CLKDIV = 1, data are latched at 0° and 180° of DATACLK, and setup and hold times must be satisfied for both these points in time.

For the case of CLKDIV = 0, data are latched at 0°, 90°, 180°, and 270° of DATACLK. Setup and hold times must be satisfied for all four of these points in time.

A delay set by the DELAY pin can skew DATACLK by 1/2 period of the input data period, as shown in Figure 11. This eases interfacing to an FPGA where the clock to Q delay of the LVDS outputs is not adjustable. The clock driving the data input register is not delayed with the DELAY pin. The setup and hold times are always referred to the case when DELAY = 0. Data-timing relationships are shown in Figure 12.

12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

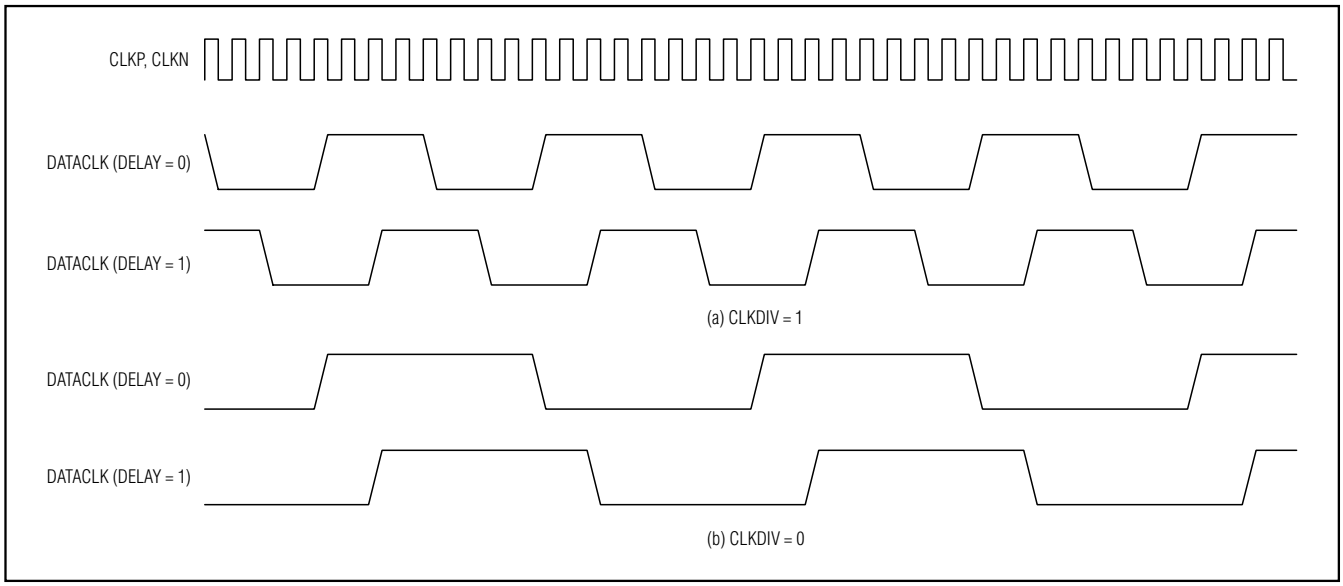


Figure 11. Effect of Setting DELAY = 1 on Data Clock Output

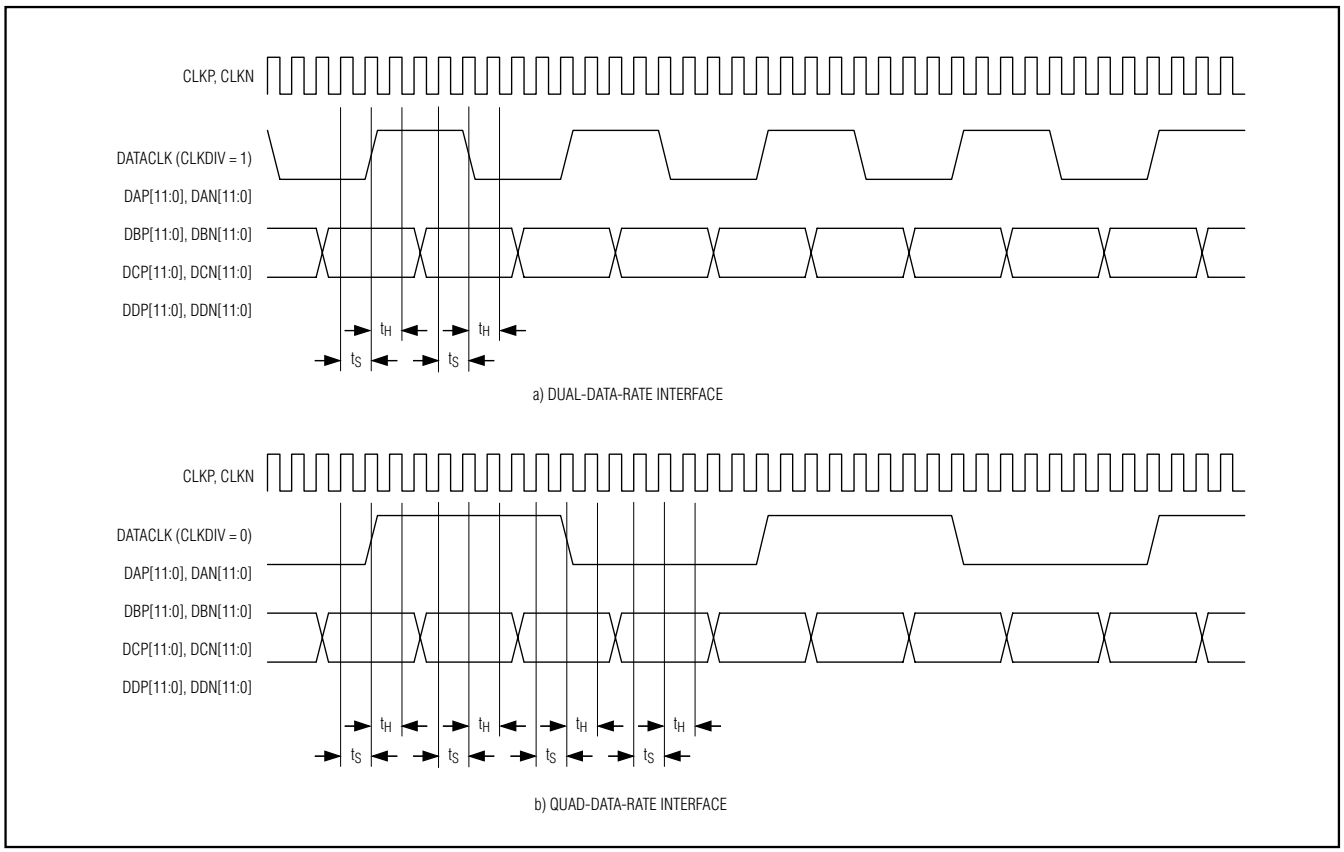


Figure 12. Setup (t_S) and Hold Time (t_H) for Data Input Interface

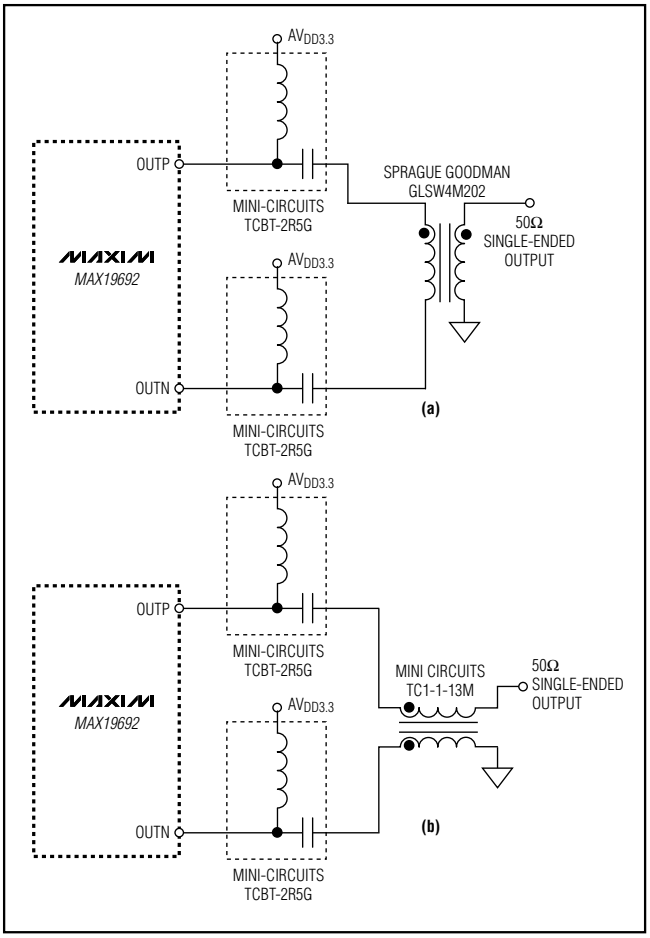


Figure 13. Possible Output Circuits for MAX19692

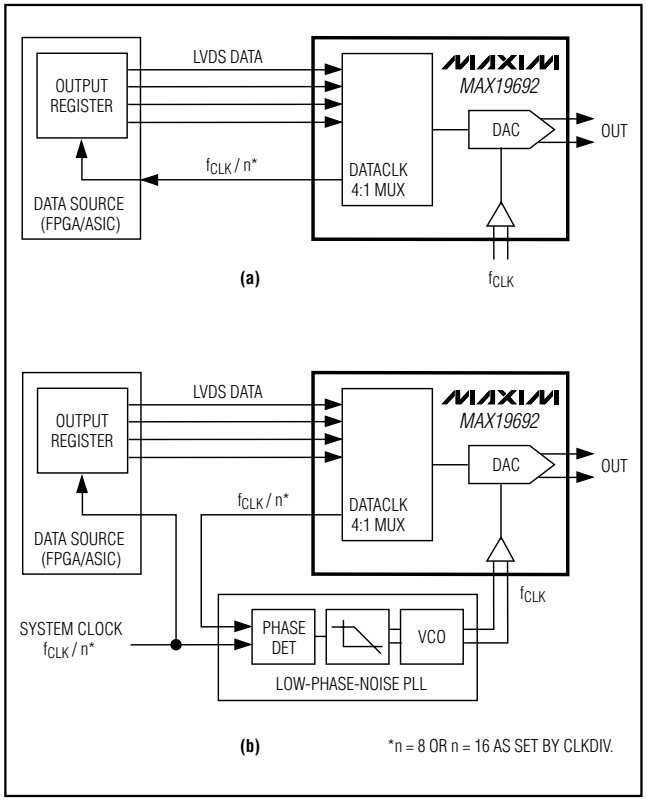


Figure 14. Data Source to DAC Interfacing

Applications Information

Differential Coupling Using RF Transformers

The differential voltage existing between OUTP and OUTN can be converted to a single-ended voltage using a transformer or a differential amplifier configuration. Using a differential transformer-coupled output, in which the output power is limited to -2.6dBm, can optimize the dynamic performance. It is recommended that the DAC outputs are pulled up to 3.3V. The use of bias tees, as shown in Figure 13, is recommended for optimal performance. RF chokes can be used rather than bias tees if an isolation transformer is used. Not pulling up the outputs to 3.3V is also possible, but may result in some degradation of dynamic performance in some applications. Two output circuits are shown in Figure 13. The circuit shown in Figure 13(a) has less than 3dB loss (in addition to the sinc attenuation built into the DAC) from approximately 4MHz to 700MHz. The circuit shown in Figure 13(b)—that is used on the MAX19692 evaluation kit—has less than 3dB loss at frequencies up to approximately 1150MHz. To achieve the maximum bandwidth, it is important to minimize the inductance in the ground lead on the secondary side of the transformers. It is recommended to use a very short trace and multiple vias for the connection to the ground plane.

Data Synchronization

The DAC clock is running at four times the data rate of the data interface to the MAX19692. An LVDS level data clock output (DATACLKP, DATACLKN) is provided to help the user synchronize the data source and the DAC. The output data clock frequency can be set to 1/2 the input data rate or 1/4 the input data rate. When the DAC is running at full speed, this allows the data clock to be interfaced directly to FPGAs without using an external clock divider. For example, if the DAC is updating at 2.3Gsps, the input data rate is 575Mwps. If the DAC is interfaced to an FPGA, one could run the data clock at 1/4 the data input rate; hence the data output clock frequency would be 143.75MHz.

12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

If the system clock is running at the DAC update rate, the scheme in Figure 14(a) can be used. In this case, the system is clocked using the data clock output from the DAC. The delays of the data and the clock depend upon line lengths and loading. Hence, clock deskewing using a phase-locked loop may be necessary to make this system work properly at speed. When CLKDIV = 0, the data clock output can be phase-shifted by 45° using the DELAY pin. When CLKDIV = 1, the data clock output can be phase-shifted by 90° using the DELAY pin.

An alternative solution is shown in Figure 14(b). In this case, the system clock distribution is running at the data clock rate. A low-jitter, low-phase-noise phase-locked loop is used to generate the high-speed DAC clock. Using the data clock for feedback into the PLL ensures synchronization between data and clock.

If more than one MAX19692 is used in a system, and the relative phases need to be defined, the divided data clock of each DAC should be phase locked to a system clock running at data-rate / 4 or data-rate / 2, which is equal to the input clock rate divided by 8 or 16.

Grounding, Bypassing, Power-Supply, and Board Layout Considerations

Grounding and power-supply decoupling can strongly influence the performance of the MAX19692. Unwanted digital crosstalk may couple through the input, reference, power supply, and ground connections, affecting dynamic performance. Proper grounding and power-supply decoupling guidelines for high-speed, high-frequency applications should be closely followed. This reduces EMI and internal crosstalk that can significantly affect the dynamic performance of the MAX19692.

Use of a multilayer PC board with separate ground and power-supply planes is required. It is recommended that the analog output and the clock input are run as controlled-impedance microstrip lines on the top layer of the board, directly above a ground plane, and that no vias are used for the clock input (CLKP, CLKN) and the analog output (OUTP, OUTN) signals. Depending on the length of the traces, and the operating condition, a low-loss dielectric material (such as ROGERS RO4003) as the top layer dielectric may be advisable. The data clock (DATACLKP, DATACLKN) must be routed so its coupling into the clock input and the DAC output is minimized.

Digital input signals should be run as controlled-impedance strip lines between ground planes. Digital signals should be kept as far away from sensitive analog inputs, reference input sense lines, common-mode inputs, and clock inputs as practical. It is particularly important to minimize coupling between digital signals and the clock to optimize dynamic performance for high output frequencies. A symmetric design of the clock input and analog output lines is critical to minimize distortion and optimize the DAC's dynamic performance.

Digital signal paths should be kept short and run lengths matched to avoid propagation delay and data-skew mismatches.

The MAX19692 supports three separate power-supply inputs for analog 3.3V ($AV_{DD3.3}$), switching ($V_{DD1.8}$), and clock (AV_{CLK}) circuits. Each $AV_{DD3.3}$, $V_{DD1.8}$, and AV_{CLK} input should at least be decoupled with a separate 47nF capacitor as close to the pin as possible and their opposite ends with the shortest possible connection to the corresponding ground plane, to minimize loop inductance. All three power-supply voltages should also be decoupled at the point they enter the PC board with tantalum or electrolytic capacitors. Ferrite beads with additional decoupling capacitors forming a pi-network could also improve performance.

The power-supply inputs $V_{DD1.8}$ and AV_{CLK} of the MAX19692 allow a 1.8V ±0.1V supply voltage range for update rates < 2.0Gsps. A range of 1.8V to 1.9V should be used for 2.0Gsps to 2.3Gsps. The analog power-supply input $AV_{DD3.3}$ allows a 3.3V ±0.2V supply voltage range. To optimize the dynamic performance of the MAX19692 over temperature at the highest update rates, it is important that the difference between $V_{DD1.8}$ and $AV_{DD3.3}$ is at least 1.4V. If $V_{DD1.8}$ is 1.9V and $AV_{DD3.3}$ is 3.1V, dynamic performance at these update rates will degrade at higher temperatures, as shown in the *Typical Operating Characteristics*.

The MAX19692 is packaged in a 169 CSBGA package with 0.8mm ball pitch **(package code: X16911-1)**, providing design flexibility, thermal efficiency, and a small footprint for the DAC.

Static Performance Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from either a best straight-line fit (closest approximation to the actual transfer curve) or end-point fit (a line drawn between the end points of the transfer function, once offset and gain errors have been nullified). For a DAC, the deviations are measured at every individual step. The MAX19692 INL is specified using the end-point method.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between an actual step height and the ideal value of 1 LSB. A DNL error specification greater than -1 LSB guarantees a monotonic transfer function.

Offset Error

The offset error is the difference between the ideal and the actual offset current. For a DAC, the offset point is the average value at the output for the two midscale digital input codes with respect to the full scale of the DAC. This error affects all codes by the same amount.

Gain Error

A gain error is the difference between the ideal and the actual full-scale output voltage on the transfer curve, after nullifying the offset error. This error alters the slope of the transfer function and corresponds to the same percentage error in each step.

Dynamic Performance Parameter Definitions

Settling Time

The settling time is the amount of time required from the start of a transition until the DAC output settles its new output value to within the specified accuracy.

Noise Spectral Density

The DAC output noise is the sum of the quantization noise and other noise sources. Noise spectral density is the noise power in a 1Hz bandwidth.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of the carrier frequency (maximum signal components) to the RMS value of the largest distortion component. SFDR is usually measured in dBc with respect to the carrier frequency amplitude or in dBFS with respect to the DAC's full-scale range. Depending on its test condition, SFDR is observed within a predefined window or to Nyquist.

Two-/Four-Tone Intermodulation Distortion (IMD)

The two-/four-tone IMD is the ratio expressed in dBc (or dBFS) of the worst 3rd-order (or higher) IMD products to any output tone.

12-Bit, 2.3Gsps, Multi-Nyquist DAC with Selectable Frequency Response

Pin Configuration

TOP VIEW

MAXIM

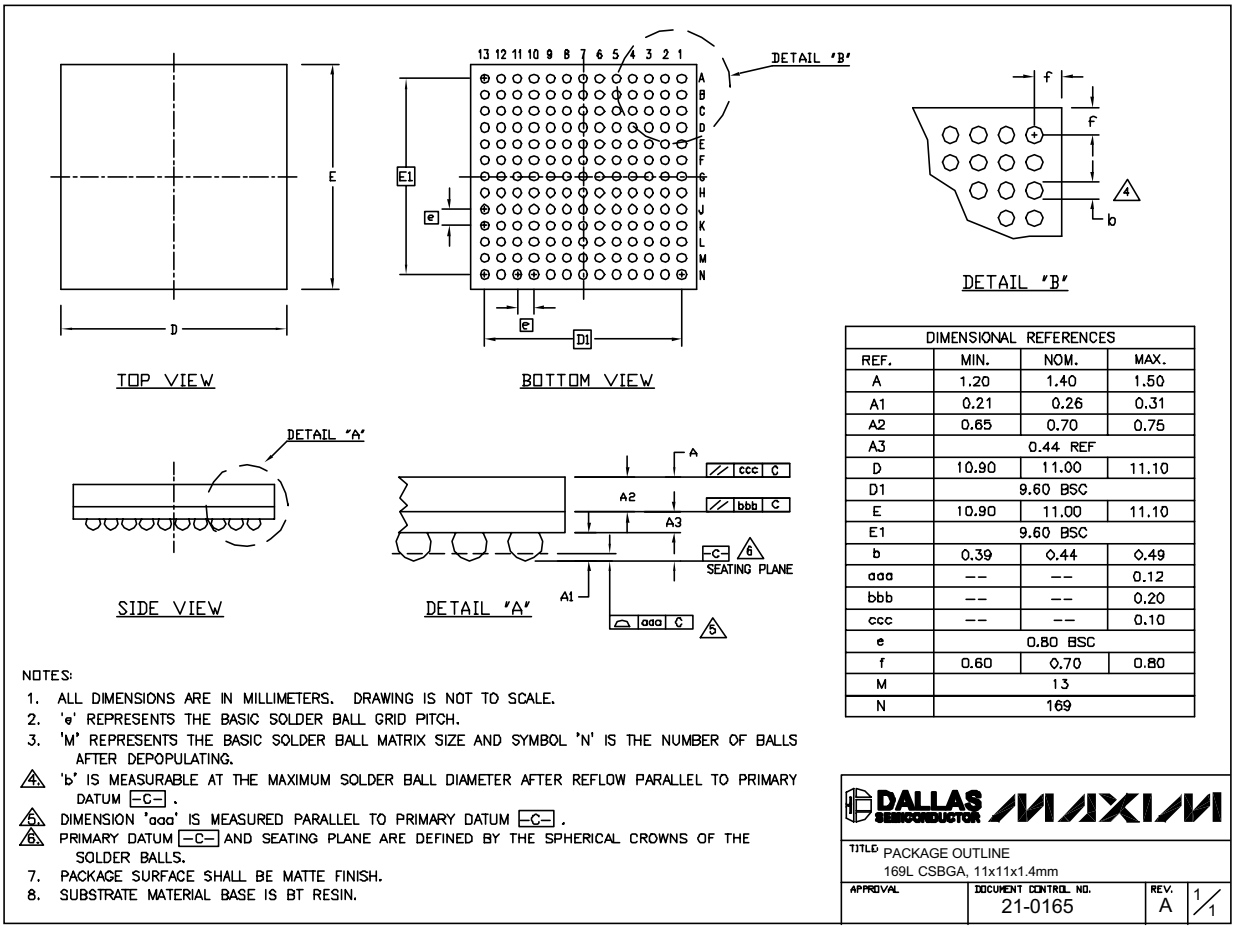
MAX19692

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	REFIO A1	FSADJ A2	DACREF A3	$AV_{DD3.3}$ A4	$AV_{DD3.3}$ A5	OUTP A6	$AV_{DD3.3}$ A7	OUTN A8	$AV_{DD3.3}$ A9	$V_{DD1.8}$ A10	GND A11	AV_{CLK} A12	GND A13
B	CREF B1	REFRES B2	RZ B3	RF B4	GND B5	GND B6	GND B7	GND B8	GND B9	$V_{DD1.8}$ B10	GND B11	AV_{CLK} B12	CLKN B13
C	CAL C1	$V_{DD1.8}$ C2	$V_{DD1.8}$ C3	GND C4	GND C5	GND C6	GND C7	GND C8	GND C9	$V_{DD1.8}$ C10	GND C11	AV_{CLK} C12	CLKP C13
D	GND D1	GND D2	GND D3	GND D4	GND D5	GND D6	GND D7	GND D8	GND D9	GND D10	GND D11	AV_{CLK} D12	GND D13
E	$V_{DD1.8}$ E1	$V_{DD1.8}$ E2	$V_{DD1.8}$ E3	$V_{DD1.8}$ E4	GND E5	GND E6	GND E7	GND E8	GND E9	$V_{DD1.8}$ E10	$V_{DD1.8}$ E11	$V_{DD1.8}$ E12	$V_{DD1.8}$ E13
F	DAP7 F1	DAP6 F2	DAP8 F3	DAP9 F4	DAP10 F5	DAP11 F6	DDN11 F7	DDN0 F8	DDN1 F9	DDN2 F10	DDN3 F11	DDN4 F12	$V_{DD1.8}$ F13
G	DAN7 G1	DAN6 G2	DAN8 G3	DAN9 G4	DAN10 G5	DAN11 G6	DDP11 G7	DDP0 G8	DDP1 G9	DDP2 G10	DDP3 G11	DDP4 G12	GND G13
H	DAP0 H1	DAP1 H2	DAP2 H3	DAP3 H4	DAP4 H5	DAP5 H6	DDN10 H7	DDN5 H8	DDN6 H9	DDN7 H10	DDN8 H11	DDN9 H12	DATACLKN H13
J	DAN0 J1	DAN1 J2	DAN2 J3	DAN3 J4	DAN4 J5	DAN5 J6	DDP10 J7	DDP5 J8	DDP6 J9	DDP7 J10	DDP8 J11	DDP9 J12	DATACLKP J13
K	DBP11 K1	DBP10 K2	DBP9 K3	DBP8 K4	DBP3 K5	DBP1 K6	DCP10 K7	DCP8 K8	DCP3 K9	DCP2 K10	DCP1 K11	DCN0 K12	DELAY K13
L	DBN11 L1	DBN10 L2	DBN9 L3	DBN8 L4	DBN3 L5	DBN1 L6	DCN10 L7	DCN8 L8	DCN3 L9	DCN2 L10	DCN1 L11	DCP0 L12	CLKDIV L13
M	DBP7 M1	DBP6 M2	DBP5 M3	DBP4 M4	DBP2 M5	DBP0 M6	DCP11 M7	DCP9 M8	DCP7 M9	DCP6 M10	DCP5 M11	DCP4 M12	GND M13
N	DBN7 N1	DBN6 N2	DBN5 N3	DBN4 N4	DBN2 N5	DBN0 N6	DCN11 N7	DCN9 N8	DCN7 N9	DCN6 N10	DCN5 N11	DCN4 N12	N.C. N13

The MAX19692 is packaged in an 11mm x 11mm, 169 CSBGA package (package code X16911-1). Ball pitch is 0.8mm.

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



DIMENSIONAL REFERENCES			
REF.	MIN.	NOM.	MAX.
A	1.20	1.40	1.50
A1	0.21	0.26	0.31
A2	0.65	0.70	0.75
A3		0.44 REF	
D	10.90	11.00	11.10
D1		9.60 BSC	
E	10.90	11.00	11.10
E1		9.60 BSC	
b	0.39	0.44	0.49
aaa	--	--	0.12
bbb	--	--	0.20
ccc	--	--	0.10
e		0.80 BSC	
f	0.60	0.70	0.80
M		13	
N		169	

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE
169L CSBGA, 11x11x1.4mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0165	A	1/1