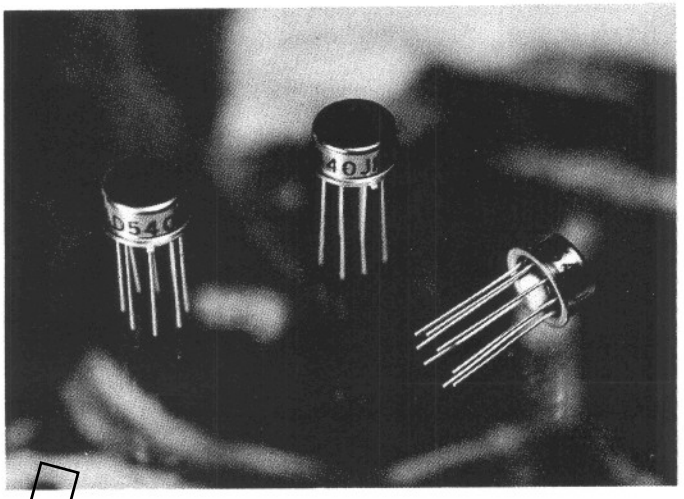
ANALOG DEVICES

High Accuracy, Low Cost, FET-Input Operational Amplifier

AD540

FEATURES

- Low Cost: $4.45 (100's, J)
- Low I_b: 25pA max (K)
- Low V_{os}: 20mV max (K)
- Low V_{os} Drift: 25μV/°C max (K)
- High Differential Input Voltage Capability: ±20V



PRODUCT DESCRIPTION

The AD540 is the lowest cost, high accuracy FET-input op amp available which provides the user with low bias currents, high overall performance, and accurately specified predictable operation. The device offers maximum bias currents as low as 25pA, offset voltages below 20mV, maximum offset voltage drift below 25μV/°C and a minimum gain of 50,000.

All devices are free from latchup and are short-circuit protected. No external compensation is required as the internal 6dB/octave roll-off provides stability in closed loop applications.

The AD540 is suggested for all FET-input amplifier requirements where low cost is of prime importance. Its performance is comparable to modular FET op amps, but its IC construction reduces the price significantly below that of modules.

All versions of the AD540 are supplied in the hermetically-sealed, 8-pin, TO-99 package. The AD540J and AD540K are specified for 0 to +70°C applications, while the AD540S is offered for operation over the full military temperature range of −55 to +125°C.

PRODUCT HIGHLIGHTS

1. The AD540 op amp meets specified input bias current and offset voltage values after full warm-up. Conventional high speed IC testing does not allow for self-heating of the chip due to internal power dissipation under operating conditions.
2. The bias currents of the AD540 are specified as a maximum for either input. Conventional IC FET op amps generally specify bias currents as the average of the two input currents.
3. Unlike many FET-input op amps, the AD540 allows a maximum differential input voltage of ±20VDC. Standard "bootstrapped" FET-input op amps permit maximum differential input voltages of only about ±3V.
4. Offset nulling of the AD540 is accomplished without affecting the operating current of the FET's and results in relatively small changes in temperature drift characteristics. The additional drift induced by nulling is only ±2.0μV/°C per millivolt of nulled offset, compared to several times this for other IC FET op amps.
5. The gain of the AD540 is measured with the offset voltage nulled. Nulling a FET-input op amp can cause the gain to decrease below its specified limit. The gain of the AD540 is fully guaranteed with the offset voltage both nulled and unnulled.
6. To maximize the reliability inherent in IC construction, every AD540 is stored for 40 hours at +150°C, temperature cycled from −65 to +125°C and receives a high impact shock test.

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SPECIFICATIONS (typical @ +25°C and V_S = ±15VDC unless otherwise specified)

MODEL	AD540J	AD540K	AD540S
OPEN LOOP GAIN (Note 1)			
V_{out} = ±10V, $R_L \geq 2k\Omega$	20,000 min	50,000 min	**
T_A = min to max	15,000 min	25,000 min	**
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±13V typ)	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±12V min (±14V typ)	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	6.0V/μsec	*	*
INPUT OFFSET VOLTAGE (Note 2)	50mV max	20mV max	**
vs. Temperature	75μV/°C max	25μV/°C max	50μV/°C max
vs. Supply, T_A = min to max	400μV/V max	300μV/V max	**
INPUT BIAS CURRENT			
Either Input (Note 3)	50pA max	25pA max	**
INPUT IMPEDANCE			
Differential	$10^{10}\Omega \| 2pF$	*	*
Common Mode	$10^{11}\Omega \| 2pF$	*	*
INPUT VOLTAGE RANGE			
Differential (Note 4)	±20V	*	*
Common Mode	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{in} = ±10V	70dB min	*	*
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	*
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE RANGE			
Operating, Rated Performance	0 to +70°C	*	−55 to +125°C
Storage	−65 to +150°C	*	*
PRICE			
(1–24)	$6.45	$8.95	$14.95
(25–99)	$5.70	$7.20	$11.95
(100–999)	$4.45	$5.95	$ 9.95

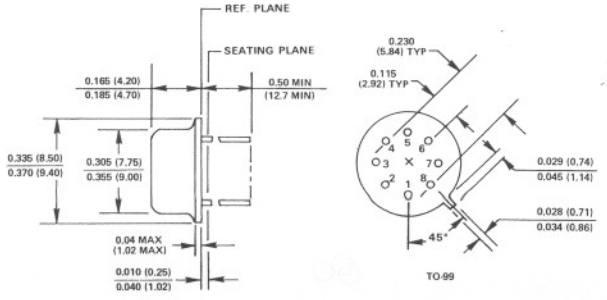
NOTE:
1. Open Loop Gain is specified with V_{os} both nulled and unnulled.
2. Input Offset Voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.
3. Bias Current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.
4. Defined as voltage between inputs, such that neither exceeds ±10V from ground.

* Specifications same as AD540J.
** Specifications same as AD540K.

Specifications and prices subject to change without notice.

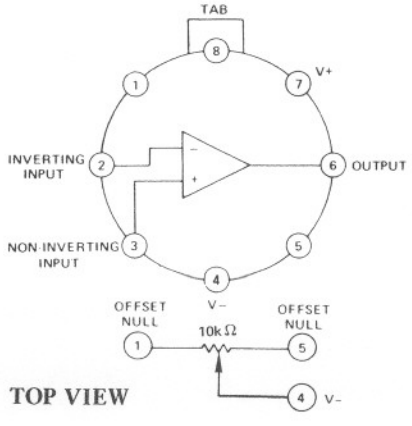
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TO-99

PIN CONFIGURATION



TOP VIEW

APPLYING THE AD540

The AD540 is especially designed for low cost applications involving the measurement of low level currents or small voltages from high impedance sources in which bias current can be a primary source of error. Input bias current contributes to error in two ways: (1) in current measuring configurations the bias current limits the resolution of a current signal; (2) the bias current produces a voltage offset which is proportional to the value of input resistance (in the case of an inverting configuration) or source impedance (when the non-inverting "buffer" connection is used). The AD540 FET-input operational amplifier is, therefore, of use where small currents are to be measured or where relatively low voltage drift is necessary despite large values of source resistance.

APPLICATIONS CONSIDERATIONS

BIAS CURRENTS. Most IC FET op amp manufacturers specify maximum bias currents as the value immediately after turn-on. Since FET bias currents double every 10°C and since most FET op amps have case temperature increases of 15°C to 20°C above ambient, initial "maximum" readings may be only ¼ of the true warmed-up value. Furthermore, most IC FET op amp manufacturers specify I_B as the average of both input currents, sometimes resulting in twice the maximum bias current appearing at the input being used. The total result is that 8X the expected bias current may appear at either input terminal in a warmed-up operating unit.

The AD540 specifies maximum bias current at either input after warm-up, thus giving the user the values he expected.

IMPROVING BIAS CURRENT BEYOND GUARANTEED VALUES. Bias currents can be substantially reduced in the AD540 by decreasing the junction temperature of the devices. One technique to accomplish this is to reduce the operating supply voltage. This procedure will decrease the power dissipation of the device, which will in turn result in a lower junction temperature and lower bias currents. The supply voltage effect on bias current is shown in Figure 1.

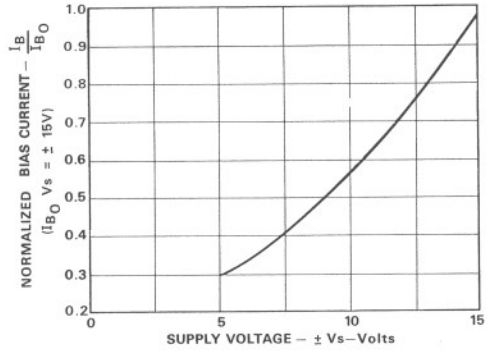


Figure 1. Normalized Bias Current vs. Supply Voltage

Operation of the AD540K at ±5V reduces the warmed-up bias current by 70% to a typical value of 8pA.

A second technique is the use of a suitable heat sink. Wakefield Engineering Series 200 heat sinks were selected to demonstrate this effect. The characteristic bias current vs. case temperature above ambient is shown in Figure 2. Bias current has been normalized with unity representing the 25°C free air reading. Note that the use of the Model 209 heat sink reduces warmed-up bias current by 60% to 10pA in the AD540K.

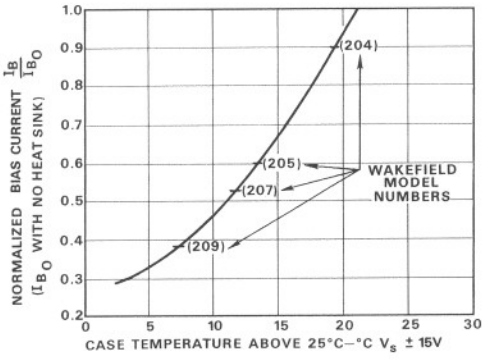


Figure 2. Normalized Bias Current vs. Case Temperature

Both of these techniques may be used together for obtaining lower bias currents. Remember that loading the output can also affect the power dissipation.

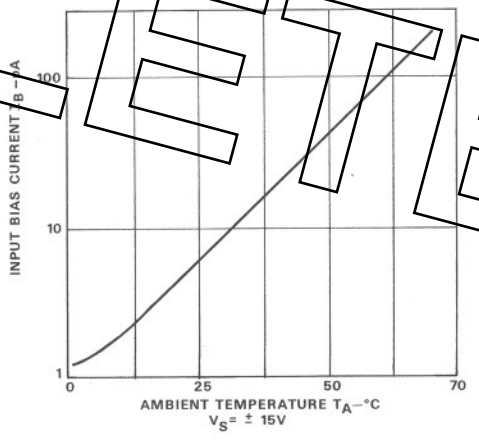


Figure 3. Input Bias Current vs. Temperature

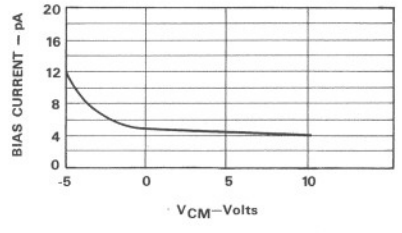


Figure 4. Bias Current vs. Common Mode Voltage.

INPUT CONSIDERATIONS. Unlike some FET-input operational amplifiers, the AD540 accommodates differential input voltages of up to ±20V....without any degradation in bias current. In certain time-dependent applications, such as charge amplifiers and integrators, large differential input voltages temporarily occur which may exceed the rated value of a typical FET op amp (approximately ±3V differential).

By utilizing un-bootstrapped FET's at the inputs, the AD540 assures the user of expected performance at large differential input voltages....without the use of protective diodes or resistors.

OFFSET VOLTAGE DRIFT. Most commercially available IC FET op amps are nulled by adjusting the FET operating currents, causing the offset voltage temperature coefficients to vary 3 to 6μV/°C per millivolt of offset nulled. Thus a conventional FET op amp with 20mV initial offset, when nulled may display an additional offset drift of 60 to 120μV/°C, in addition to its nulled value.

The AD540 achieves nulling without disturbing the operating currents of the FET's, thus allowing a substantial reduction in drift. Figure 5 graphically displays the offset drift performance of the AD540, nulled and unnulled. As can be seen, nulling the device can result in either positive or negative offset drifts given by the slope $\Delta V_{OS}/\Delta T$. The nulled curves represent the maximum changes in drift, indicating performance considerably better than many other IC FET op amps which null V_{OS} by varying the operating currents of the FET's.

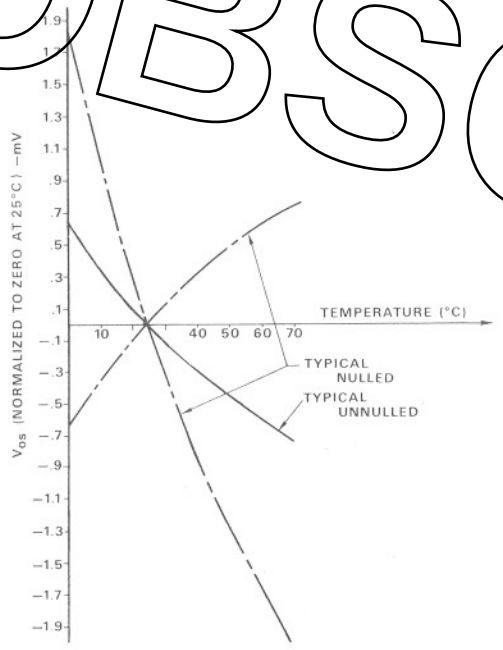


Figure 5. V_{OS} vs. Temperature

NOISE PERFORMANCE. The noise spectral density vs. frequency for the AD540 is given in Figure 6. The curve shows approximately 300nV/$\sqrt{Hz}$ at 10Hz, declining in a 1/f fashion (1/f for power, 1/$\sqrt{f}$ for voltage) to approximately 12nV/$\sqrt{Hz}$ at higher frequencies.

Current noise in the AD540 is approximately 0.001pA/$\sqrt{Hz}$ at low frequencies. Above 300Hz, the current noise generated by the op amp increases at a 3dB/octave rate, determined by $\omega e_n C_{in}$, where e_n = spectral noise density and C_{in} = input capacitance. In most practical applications, the current noise from source or feedback resistors will be larger than the low frequency current noise from the amplifier.

At high frequencies, the total circuit current noise is equal to $\omega e_n C$, where C is the sum of all input and feedback capacitors. In well-shielded circuits, C is usually 10 to 100pF, so that the $\omega e_n C$ can be a significant factor. Thus the user should attempt to minimize C.

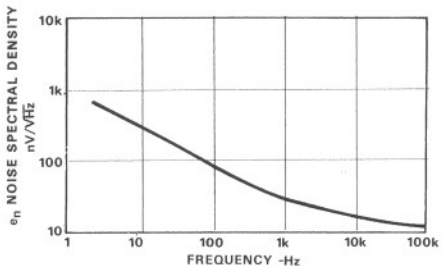


Figure 6. Noise Spectral Density vs. Frequency

DYNAMIC PERFORMANCE. The AD540 is internally compensated to achieve a −3dB bandwidth of 1MHz (see Figure 7). At unity gain the full power bandwidth is 50kHz minimum, and typically 100kHz. Slew rates are 3V/μsec minimum and 6V/μsec typical (see Figure 8 and Figure 9).

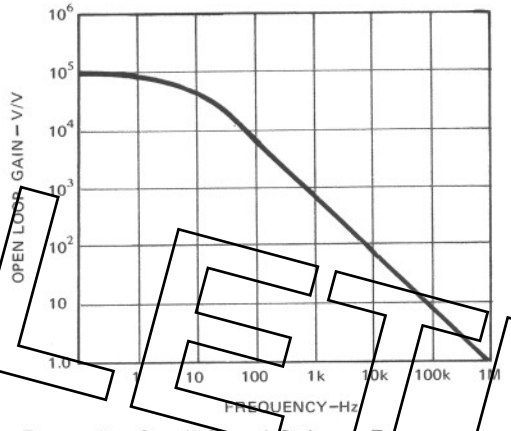


Figure 7. Small Signal Gain vs. Frequency

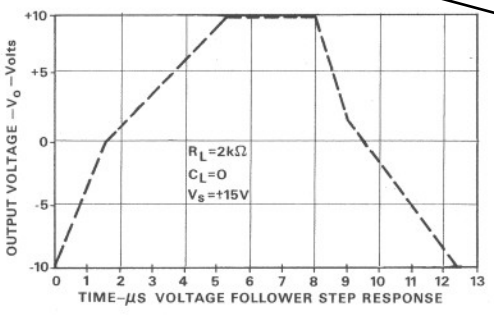


Figure 8. Voltage Follower Step Response

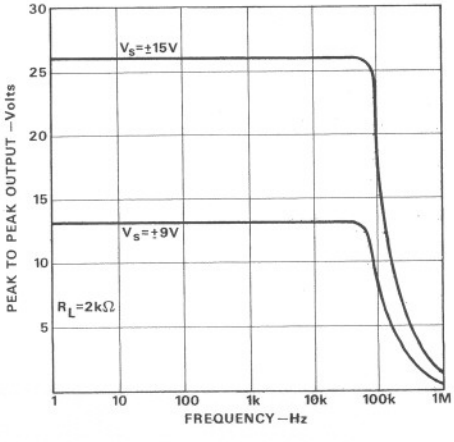


Figure 9. P-P Output vs. Frequency