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OptiPHY™ F155 Quad OC-3/STM-1 ATM/POS PHY

CX29704/2/1

Four-Channel CX29704, two-channel CX29702, one-channel CX29701 155Mbps ATM/POS PHY with Clock and Data Recovery

The CX2970x is an integrated circuit that implements four-channel ATM/Packet over SONET/SDH (POS) processing functions at 155.52 Mbps. The device contains both the PMD and TC sublayers and features a UTOPIA Level 2 interface to the ATM layer or, optionally, a POS PHY Level 2 interface to the link layer. This device also includes dedicated serial ports for the insertion and extraction of the DCC overhead bytes.

SONET/SDH Processing

In the transmit path, this device generates all section, line and path overhead bytes, in addition to implementing framing, scrambling and alarm indication functions. On the receive path, all framing, descrambling, alarm detection and pointer interpretations are performed. A serial interface inserts and extracts the section or line DCC bytes.

ATM Cell Processing

For ATM cell processing, the CX2970x performs all cell encapsulation, HEC calculation, cell delineation, payload scrambling/descrambling and idle cell insertion/filtering. Data is exchanged with a higher-layer device using a UTOPIA Level 2 interface.

POS Processing

In POS mode, the CX2970x performs all HDLC framing, scrambling/descrambling, interframe fills, FIFO management and stuffing/destuffing operations. Data is exchanged with higher-layer devices using a POS PHY Level 2 interface.

KEY FEATURES

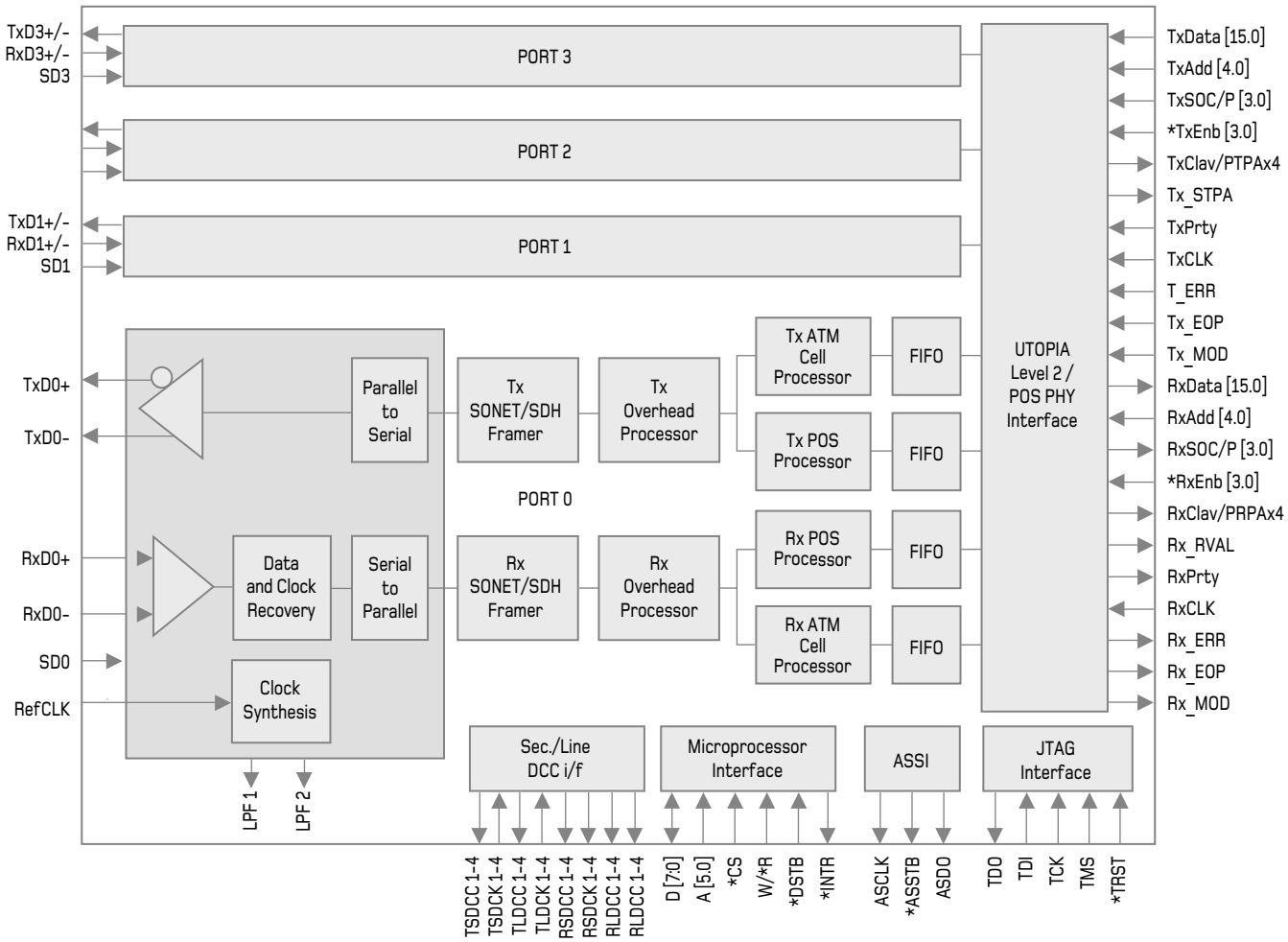
- Integrated clock and data recovery (CDR)
- Clock recovery conforms to GR-253-CORE jitter requirements
- Low-power, 3.3 V CMOS technology
- Synthesizes a 155 MHz Tx clock from a 19 MHz input
- UTOPIA Level 2 and POS Level 2 system interfaces

Line Interface

The CX2970x includes on-chip clock and data recovery (CDR) for 155.52 Mbps line rates. This CDR block also implements the serialize/deserialize functions. On the receive path, after recovery of the data and its associated clock, data is sent to the SONET/SDH framer via a parallel bus.

Higher-Layer Interface

The CX2970x supports several interfaces to higher-layer devices. The component supports a UTOPIA Level 2 interface for ATM cells and a POS PHY interface for PPP packets in POS mode. Up to eight CX2970x devices can be connected to a single higher-level device (multiport ATM-layer or POS-layer device), in various operation modes.



CX2970x Block Diagram

Product Features

- **Four fully configurable independent channels, supporting ATM or POS**
- **Fully integrated clock and data recovery module supporting a 155.52 Mbps data stream**
- **STS-3c/STM-1 data-stream processing with mapping functions of ATM cells or PPP packets into SONET/SDH payloads**
- **Full processing of SONET/SDH section, line and path overhead bytes with DCC overhead interface**
- **Access to all SONET/SDH overhead bytes via a microprocessor port**
- **UTOPIA Level 2 and POS PHY Level 2 interfaces to higher-layer devices**
- **Optional SONET/SDH frame scrambling/descrambling operation (1+X6+X7)**
- **Standard IEEE 1149.1 JTAG port**
- **Complies with SONET/SDH standards (Bellcore GR-253, ITU-G.707 and ANSI T1.105)**
- **Complies with PPP protocol over SONET/SDH (RFC 1619/1662 of the IETF)**
- **272-pin PBGA package**
- **3.3 V operation, with 5 V input tolerance**

Applications

- **Switches**
- **Routers**
- **DSLAMs**
- **Cellular base station infrastructure**

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